Description

The F0452 is an integrated dual-path RF front-end consisting of an RF switch and two gain stages with 6dB gain control used in the analog front-end receiver of an Active Antenna System (AAS). The F0452 supports frequencies from 2300MHz to 2700MHz.

The F0452 provides 34dB gain with +23dBm OIP3, +15dBm output P1dB, and 1.5dB noise figure at 2600MHz. Gain is reduced 6dB in a single step with a maximum settling time of 31ns. The device uses a single 3.3V supply and 130mA of I_{DD}.

The F0452 is offered in a 5 × 5 × 0.8 mm, 32-LGA package with 50Ω input and output amplifier impedances for ease of integration into the signal path.

Competitive Advantage

- High integration
- Low noise and high linearity
- On-chip matching and bias
- Extremely low current consumption

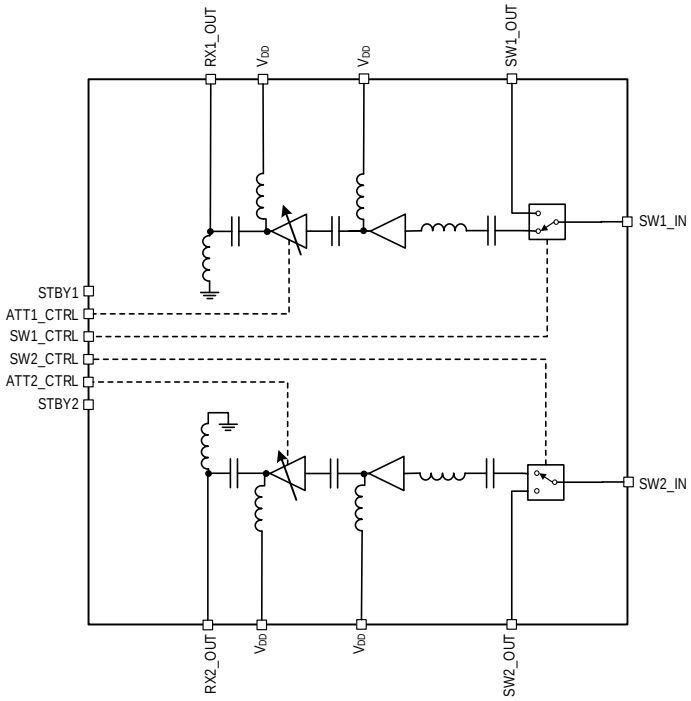
Typical Applications

- Multi-mode, Multi-carrier receivers
- 4.5G (LTE Advanced)
- 5G band 42

Features

- Gain at 2600MHz
  - 34dB typical in High Gain Mode
  - 28dB typical in Low Gain Mode
- 1.5dB NF at 2600MHz
- +23dBm OIP3 at 2600MHz
- OP1dB at 2600MHz
  - +15dBm in High Gain Mode
  - +14dBm in Low Gain Mode
- 50Ω single-ended input / output amplifier impedances
- I_{DD} = 130mA
- Independent Standby Mode for power savings
- Supply voltage: +3.15V to +3.45V
- 5 × 5 mm, 32-LGA package
- -40°C to +105°C exposed pad operating temperature range

Block Diagram



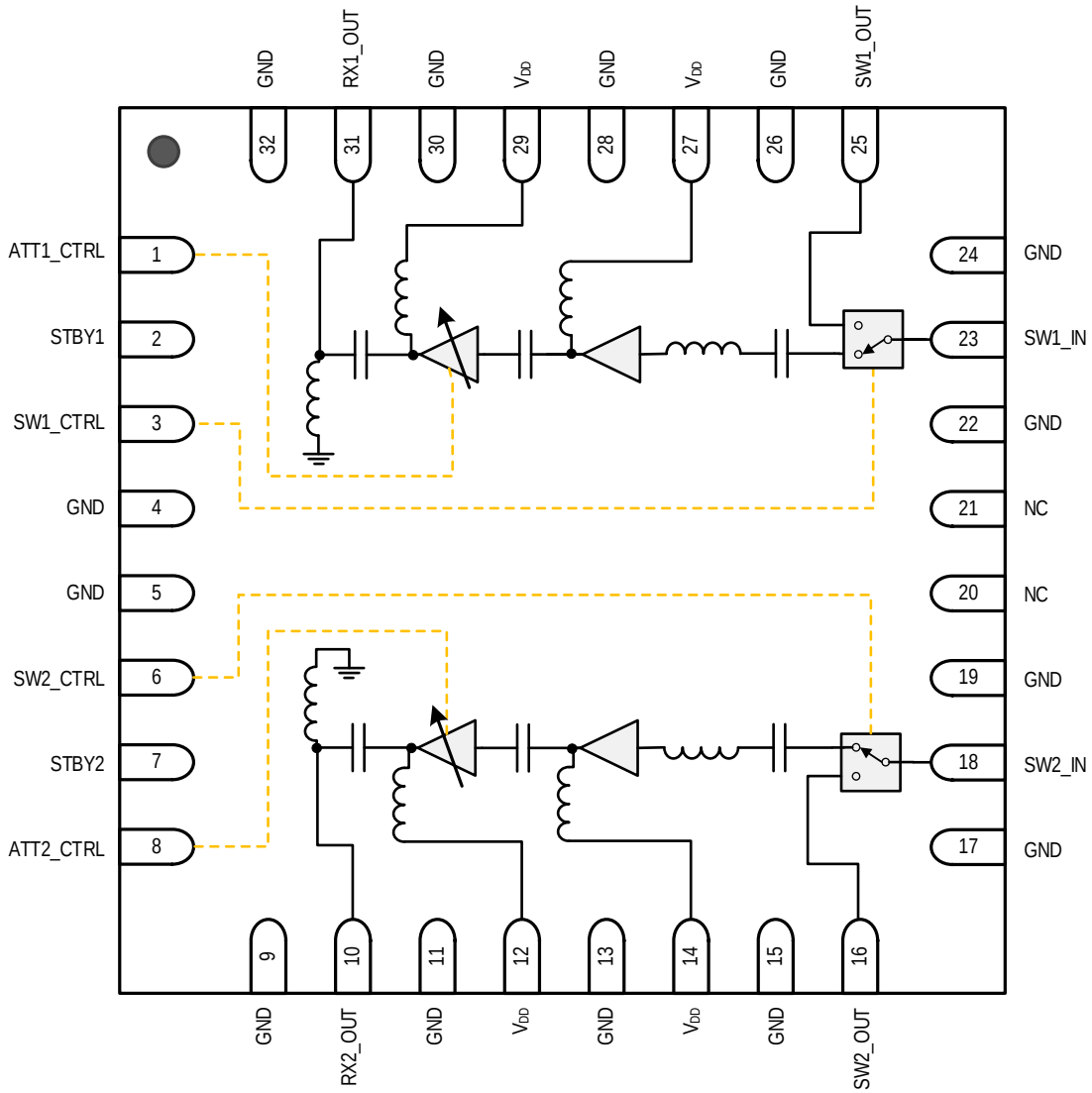
Contents

List of Figures

List of Tables

Pin Assignments

Figure 1. Pin Assignments for 5 × 5 × 0.8 mm 32-LGA – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1	ATT1_CTRL	1-bit 6dB gain control for path 1. (Low/open = no attenuation; High = 6dB attenuation). A 500kΩ pull-down resistor is connected between this input and GND.
2	STBY1	Standby (Low/open = path 1 power ON; High = path 1 power OFF). A 500kΩ pull-down resistor is connected between this input and GND.
3	SW1_CTRL	RF SWITCH 1 control (Low/open = select main RX PATH 1; High = termination). SW1_CTRL also puts path 1 into Standby Mode for minimum current consumption. A 500kΩ pull-down resistor is connected between this input and GND.
4, 5, 9, 11, 13, 15, 17, 19, 22, 24, 26, 28, 30, 32	GND	Ground these pins.
12, 14, 27, 29	VDD	Power supply. Bypass to GND with capacitors shown in the F0452 Application Circuit (see Figure 29) as close as possible to pin.
6	SW2_CTRL	RF SWITCH 2 control (Low/open = select main RX PATH 2; High = termination). SW2_CTRL also puts path 2 into Standby Mode for minimum current consumption. A 500kΩ pull-down resistor is connected between this input and GND.
7	STBY2	Standby (Low/open = path 2 power ON; High = path 2 power OFF). A 500kΩ pull-down resistor is connected between this input and GND.
8	ATT2_CTRL	1-bit 6dB gain control for path 2. (Low/open = no attenuation; High = 6dB attenuation). A 500kΩ pull-down resistor connects between this input and GND.
10	RX2_OUT	RF output path 2 matched to 50Ω. Use external DC block as close to the pin as possible.
16	SW2_OUT	RF2 switch output matched to 50Ω. Use external 50Ω terminating resistor with proper power rating as required for the application.
18	SW2_IN	RF2 switch input matched to 50Ω. Use external DC block as close to the pin as possible.
23	SW1_IN	RF1 switch input matched to 50Ω. Use external DC block as close to the pin as possible.
25	SW1_OUT	RF1 switch output matched to 50Ω. Use external 50Ω terminating resistor with proper power rating as required for the application
31	RX1_OUT	RF output path 1 matched to 50Ω. Use external DC block as close to the pin as possible.
20, 21	NC	Not internally connected.
	— EPAD	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the noted RF performance.

Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
V_{DD} to GND	V_{DD}	-0.3	+3.6	V
STBY1, STBY2, ATT1_CTRL, ATT2_CTRL, SW1_CTRL, SW2_CTRL to GND	V_{CTRL}	-0.3	V_{DD} + 0.25	V
SW1_IN, SW2_IN, RX1_OUT, RX2_OUT, SW1_OUT, SW2_OUT to GND Externally Applied DC Voltage	V_{SW}	-50	50	mV
Tx Mode CW Average Input Power +7.5dB PAR at SW1_IN, SW2_IN ports, 10s, 89% Duty Cycle 50Ω, T_{EPAD} = 105°C [a], V_{DD} = +3.3V	P_{ABS_TX}	+31	+33 [b]	dBm
Rx Mode Average Input Power +7.5dB PAR at SW1_IN, SW2_IN ports, 1 hour single event, 50% Duty Cycle 50Ω, T_{EPAD} = 105°C [a], V_{DD} = +3.3V	P_{ABS_RX}		+8	dBm
Storage Temperature Range	T_{ST}	-65	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}		+260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}		1500 (Class 1C)	V
Electrostatic Discharge – CDM (JEDEC JS-002-2014) ALL pins except pins 16, 18, 23, 25	V_{ESDCDM}		500 (Class C2a)	V
Electrostatic Discharge – CDM (JEDEC JS-002-2014) Pins 16, 18, 23, 25	V_{ESDCDM}		125 (Class C0b)	V

[a] T_{EPAD} = Temperature of the exposed paddle.

[b] RF input exposures greater than +31dBm and up to +33dBm for multiple extended periods will affect device reliability and lifetime if the maximum recommended input junction temperature is exceeded.

Recommended Operating Conditions

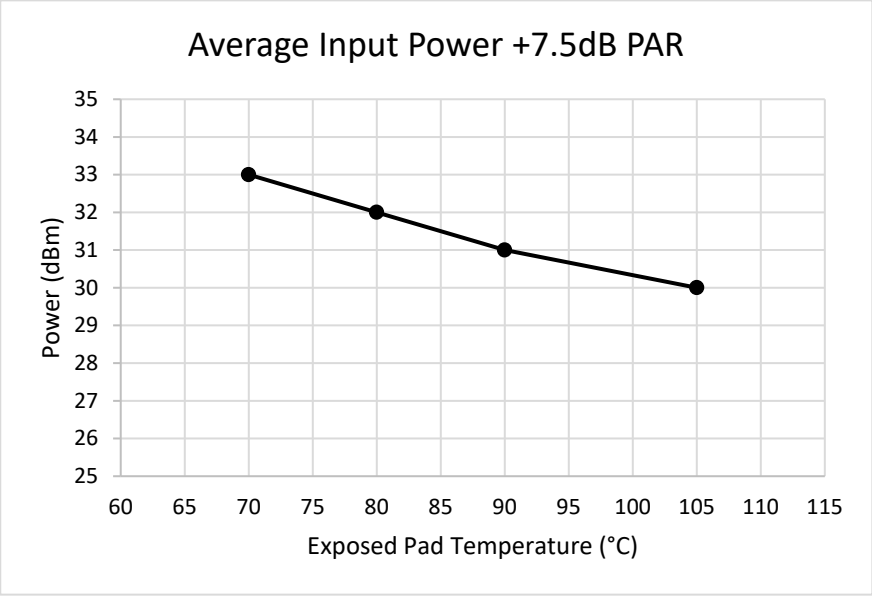
Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Power Supply Voltage	V_{DD}		3.15	3.3	3.45	V
Operating Temperature Range	T_{EPAD}	Exposed Paddle	-40		+105	°C
RF Frequency Range	f_{RF}		2300		2700	MHz
Tx Mode CW Average Input Power, +7.5dB PAR, Full Life Time [a] 50Ω, V_{DD} = +3.3V	P_{MAX_TX}	89% Duty Cycle			+30[b]	dBm
Rx Mode CW Average Input Power, +7.5dB PAR, Full Life Time [a] 50Ω, V_{DD} = +3.3V	P_{MAX_RX}	89% Duty Cycle			-25	dBm
Port Impedance (SW1_IN, SW2_IN, RX1_OUT, RX2_OUT)	Z_{RF}			50		Ω
Junction Temperature	T_J				+125	°C

[a] Assumes device environmental temperature cycling within the specified exposed pad operating temperature range of -40°C and 105°C and a maximum junction temperature of 125°C.

[b] Operation beyond the maximum recommended operating input power level should be limited and have reduced exposed pad temperatures to maintain device reliability per foundry guidelines (see Figure 2). Electrical characteristics and lifetime are not guaranteed for RF input power levels beyond what is specified in this table.

Figure 2. Typical TX Input Power and Reduced Exposed Pad Temperature Profile [c]



[c] Profile represents estimates to maintain maximum junction temperature ≤ 125°C using Renesas specific evaluation board and test environment.

Electrical Characteristics

Table 4. Electrical Characteristics

See F0452 Application Circuit in Figure 29. Specifications apply when operated as an Rx RF amplifier with V_{DD} = +3.3V, T_{EPAD} = +25°C, STBY = LOW, RX output power = -10dBm, $Z_S = Z_L$ = 50Ω, and EVKit trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input High Threshold	V_{IH}		*1.17*[a]		Lower of (V_{DD}, 3.3)	V
Logic Input Low Threshold	V_{IL}		-0.3		*0.55*	V
Logic Current	I_{IH}, I_{IL}	For each control pin	*-10*		*10*	µA
DC Current	I_{DD}	2 paths in Rx Mode		130	*180*	mA
		1 path in Rx Mode 1 path in Tx Mode		70	*100*	
		1 path in Rx Mode 1 path in Standby Mode		67		
		1 path in Tx Mode 1 path in Standby Mode		5		
		2 paths in Standby Mode		5		
Gain Step	G_{STEP}			6		dB
Gain Step Absolute Error	G_{STEP_ERR}	Relative to maximum gain, over-voltage, and temperature		±0.5		dB
Relative Phase Gain Step	G_{STEP_PH}			28		deg
Gain Step Settling Time [b]	G_{STEP_SET}	50% control logic to RF output within ±0.1dB of final value		20	31	ns
Gain Step Phase Settling Time [b]	G_{STEP_PHSET}	50% control logic to RF output within ±1 degree of final value		16	30	ns
Power ON Switching Time [b]	SW_{ON}	To Rx Mode from Tx Mode 50% control logic to RF output settled to within ±0.1dB of final value			5.6	µs
Power OFF Switching Time [b]	SW_{OFF}	To Tx Mode from Rx Mode 50% control logic to RF input settled within ±0.1dB of final value			0.5	µs

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Power ON from Standby Mode [b]	$SW_{ON\_STANDBY}$	To Rx Mode from Standby Mode 50% STBY to RF output settled within ±0.1dB of final value			1	µs
Power OFF to Standby Mode [b]	$SW_{OFF\_STANDBY}$	To Standby Mode from Rx Mode 50% STBY to gain below -25dB from max gain			1	µs

[a] Items in the Minimum/Maximum columns in ***bold italics*** are confirmed by test. Items in the Minimum/Maximum columns NOT in bold italics are confirmed by design characterization.

[b] f_{RF} = 2600MHz. Assumes the control signal is clean and no external RC circuitry is required on the pin. Adding RC circuitry increases switching time. Timing tests performed with a control logic signal of +3.3V and a rise/fall time ≤ 30ns.

Electrical Characteristics

Table 5. Electrical Characteristics: RX Path in Rx Mode Cascaded Performance

See the F0452 Application Circuit in Figure 29. Specifications apply when operated as an Rx RF amplifier with V_{DD} = +3.3V, f_{RF} = 2600MHz, T_{EPAD} = +25°C, STBY = LOW, RX output power = -10dBm, Z_S = Z_L = 50Ω, and EVKit trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Input Return Loss	RL_{IN}	Measured at SW1_IN, SW2_IN High/Low Gain Mode, f_{RF} = 2400MHz		12[a]		dB
		Measured at SW1_IN, SW2_IN High/Low Gain Mode, f_{RF} = 2600MHz		20		
		Measured at SW1_IN, SW2_IN High/Low Gain Mode, f_{RF} = 2300MHz to 2700MHz	6			
Output Return Loss	RL_{OUT}	Measured at RX1_OUT, RX2_OUT, High/Low Gain Modes, f_{RF} = 2300MHz to 2700MHz	7			dB
Reverse Isolation, RX1_OUT to SW1_IN, or RX2_OUT to SW2_IN	ISO_{REV}	f_{RF} = 2300MHz to 2700MHz	50	58		dB
Gain	G_{HG}	High Gain Mode	***32***	34	***37***	dB
	G_{HG_TEMP}	T_{EPAD} = -40 to 105°C	31		38	
Gain Attenuated	G_{LG}	Low Gain Mode	25.5	28	31.5	dB
Gain Ripple	G_{RIPPLE}	f_{RF} = 2300MHz to 2700MHz (Difference between maximum and minimum gain in each 100MHz subrange within the specified frequency range)		±0.75		dB
Noise Figure	NF	Measured at antenna port ideally matched to LNA		1.5	1.7	dB
		T_{EPAD} = 105°C			2.3	
		Low Gain Mode		1.5		

[a] Items in Minimum/Maximum columns in ***bold italics*** are confirmed by test. Items in Minimum/Maximum columns NOT in bold italics are confirmed by design characterization.

[b] Specification reflects use of an external termination resistor at SW1_OUT, SW2_OUT with a RL > 22dB.

[c] Performance can be further improved with tuning at the SW1_OUT and SW2_OUT ports.

Electrical Characteristics

Table 6. Electrical Characteristics: RX Path in Rx Mode Cascaded Performance and TX Performance

See the F0452 Application Circuit in Figure 29. Specifications apply when operated as an Rx RF amplifier with V_{DD} = +3.3V, f_{RF} = 2600MHz, T_{EPAD} = +25°C, STBY = LOW, RX output power = -10dBm, Z_S = Z_L = 50Ω, and EVKit trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Output Third-Order Intercept Point	$OIP3_1$	Pout = 0dBm/tone 5MHz tone separation		23[a]		dBm
	$OIP3_2$	Pout = 0dBm/tone 5MHz tone separation T_{EPAD} = -40 to 105°C	20			
	$OIP3_3$	Pout = 0dBm/tone 5MHz tone separation Low Gain Mode		23		
	$OIP3_4$	Pout = 0dBm/tone 5MHz tone separation Low Gain Mode T_{EPAD} = -40 to 105°C	18			
Output 1dB Compression	$OP1dB_1$	High Gain Mode [b]	13	15		dBm
	$OP1dB_2$	High Gain Mode T_{EPAD} = -40 to 105°C	11			
	$OP1dB_3$	Low Gain Mode		14		
	$OP1dB_4$	Low Gain Mode T_{EPAD} = -40 to 105°C	10			
Channel Isolation	ISO_{CH}	$RFISO_1 = \left(\frac{RX1\_OUT}{RX2\_OUT}\right)_{dB}$ with -60 ≤ SW1_IN ≤ -30dBm $RFISO_2 = \left(\frac{RX2\_OUT}{RX1\_OUT}\right)_{dB}$ with -60 ≤ SW2_IN ≤ -30dBm	40	50		dB
RF Switch Isolation	ISO_{SW}	Tx Mode Measured at SW_IN to RX_OUT of the same channel	55	65		dB

[a] Items in Minimum/Maximum columns in ***bold italics*** are confirmed by test. Items in Minimum/Maximum columns NOT in bold italics are confirmed by design characterization.

[b] In the OP1dB calculation formula, "G" denotes the gain of each part instance at the frequency of interest and appropriate High / Low gain state.

Thermal Characteristics

Table 7. Thermal Characteristics

Parameter	Symbol	Value	Units
Junction-to-Ambient Thermal Resistance	θ_{JA}	43	°C/W
Junction-to-Case Thermal Resistance (Case is defined as the exposed paddle)	θ_{JC_BOT}	11.7	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL3	

Typical Operating Conditions

Unless otherwise noted:

- V_{DD} = +3.3V
- T_{EPAD} = 25°C
- $Z_L = Z_S$ = 50Ω single-ended with matching networks
- STBY = Low or open
- SW_CTRL = Low or open
- Gain Setting = High Gain Mode
- $P_{IN} \leq$ -30dBm
- All temperatures are referenced to the exposed paddle
- Evaluation kit traces and connector losses are de-embedded

Typical Performance Characteristics: Part 1

Figure 3. Rx Mode Gain (High Gain)

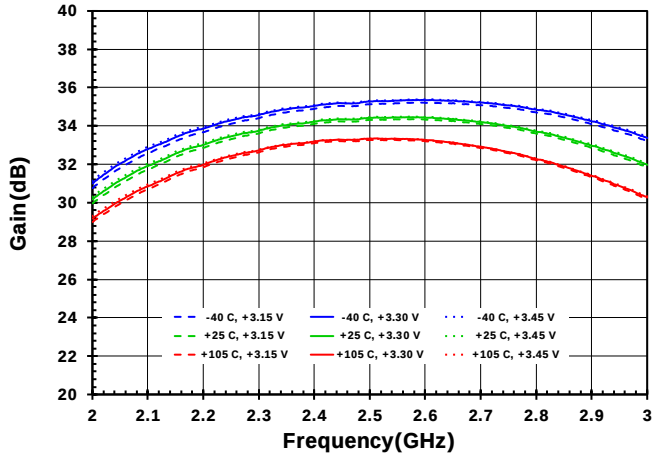


Figure 4. Rx Mode Gain (Low Gain)

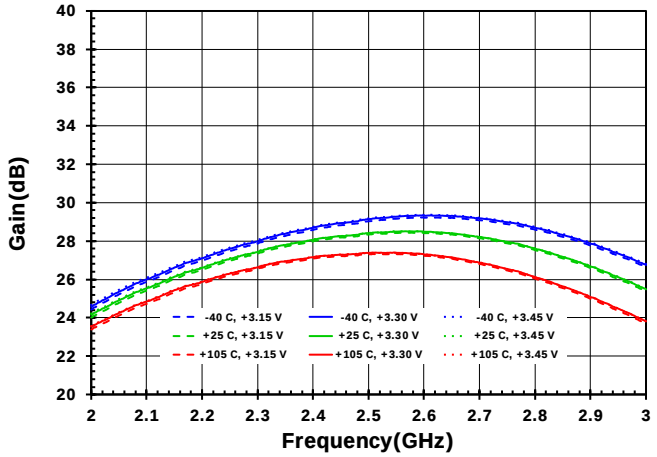


Figure 5. Rx Mode Channel Isolation (High Gain)

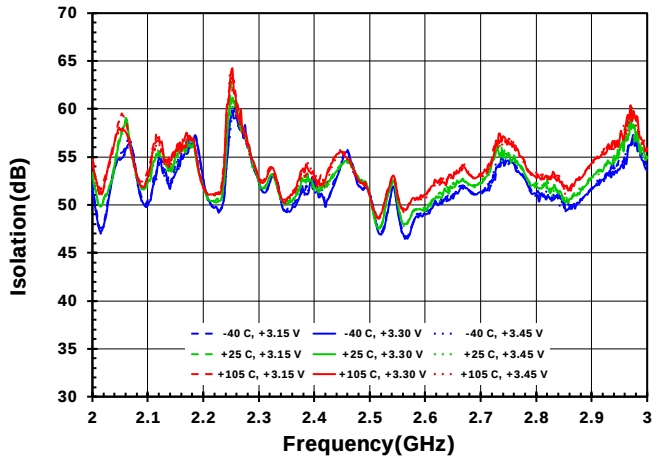


Figure 6. Rx Mode Channel Isolation (Low Gain)

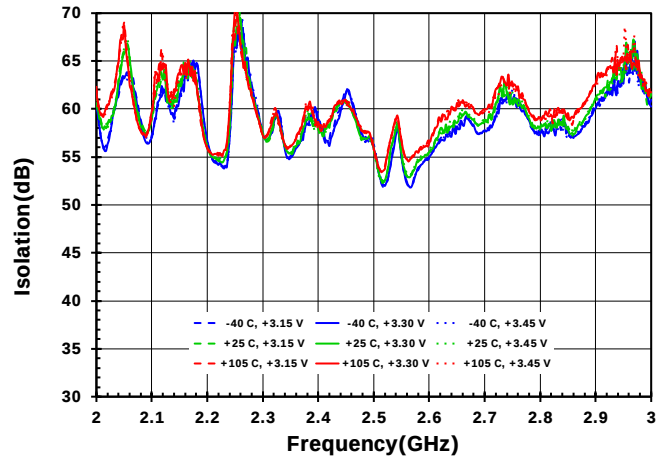


Figure 7. Rx Mode Input Return Loss (High Gain)

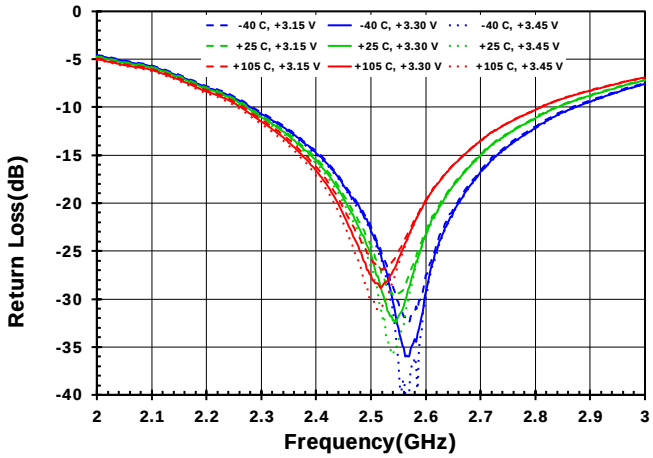
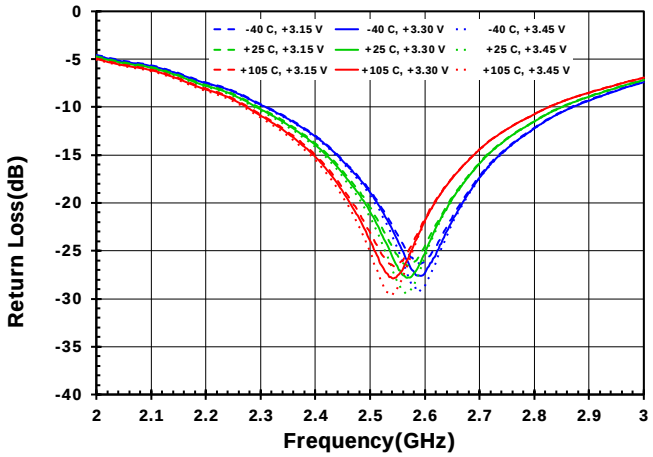


Figure 8. Rx Mode Input Return Loss (Low Gain)



Typical Performance Characteristics: Part 2

Figure 9. Rx Mode Output Return Loss (High Gain)

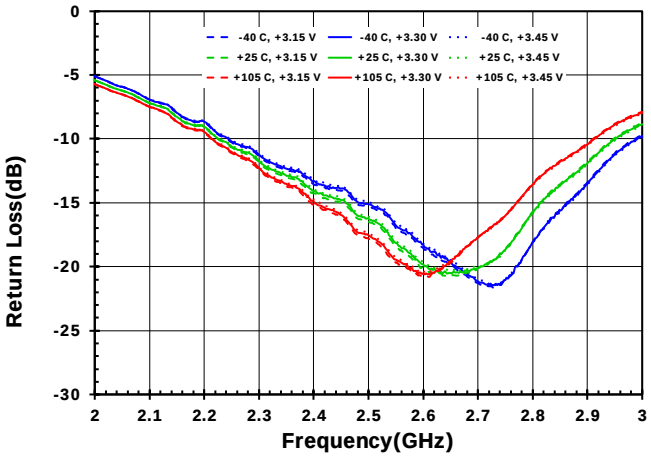


Figure 10. Rx Mode Output Return Loss (Low Gain)

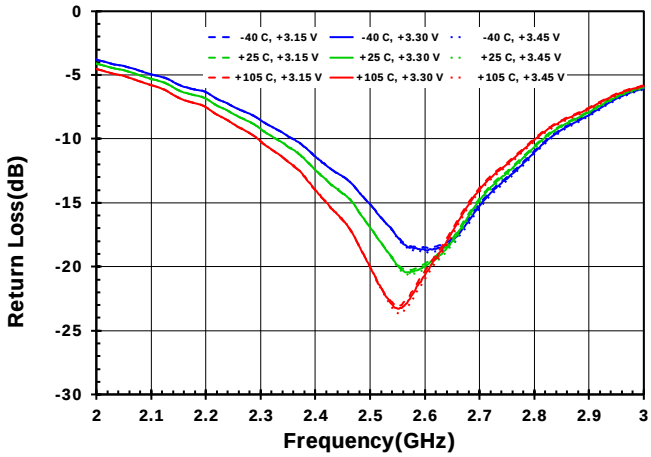


Figure 11. Rx Mode OP1dB vs. Frequency (High Gain)

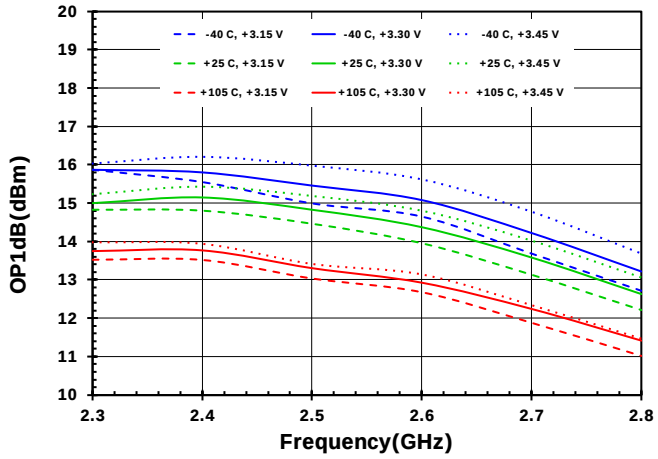


Figure 12. Rx Mode OP1dB vs. Frequency (Low Gain)

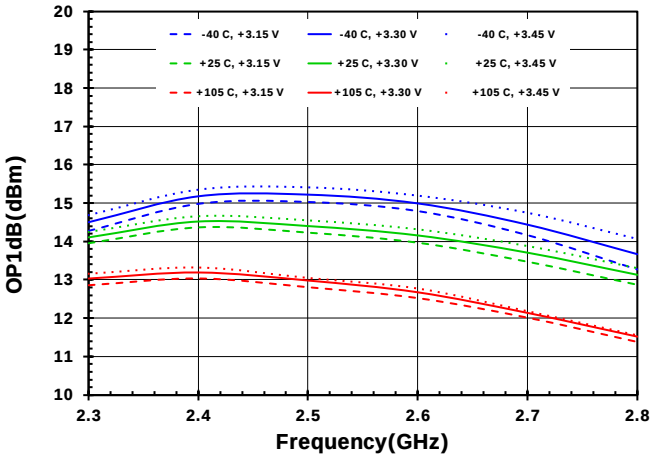


Figure 13. Rx Mode OIP3 vs. Frequency (High Gain)

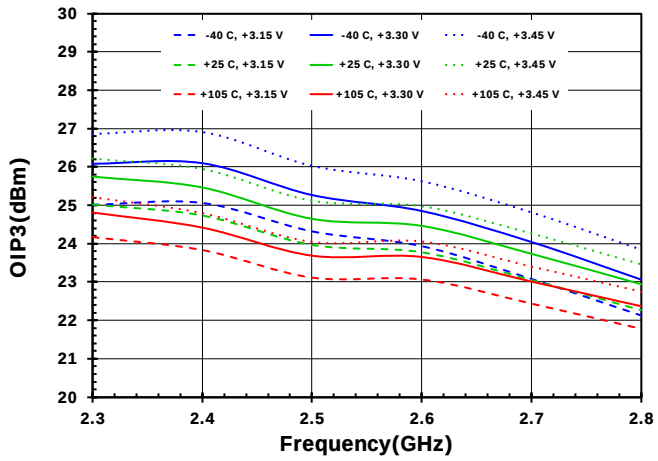
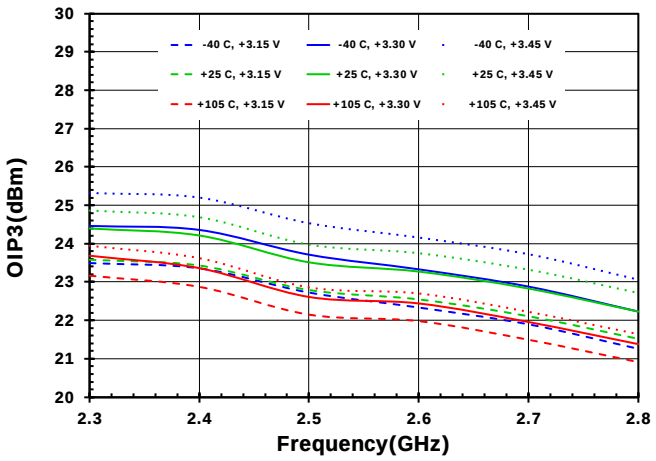


Figure 14. Rx Mode OIP3 vs. Frequency (Low Gain)



Typical Performance Characteristics: Part 3

Figure 15. Tx Mode Switch Isolation (SW_IN to RX_OUT)

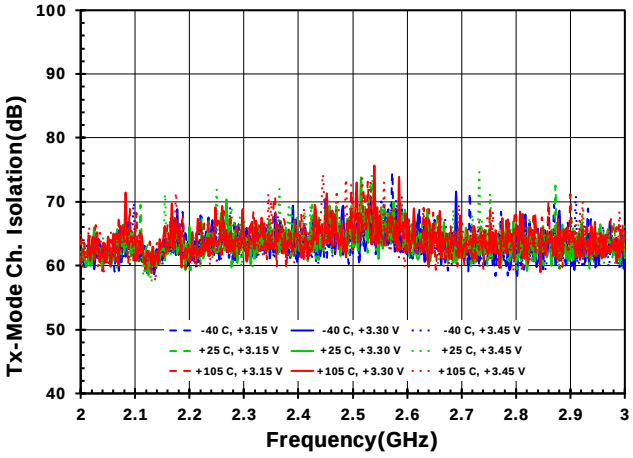


Figure 16. Tx Mode Channel Isolation (Switch Inputs)

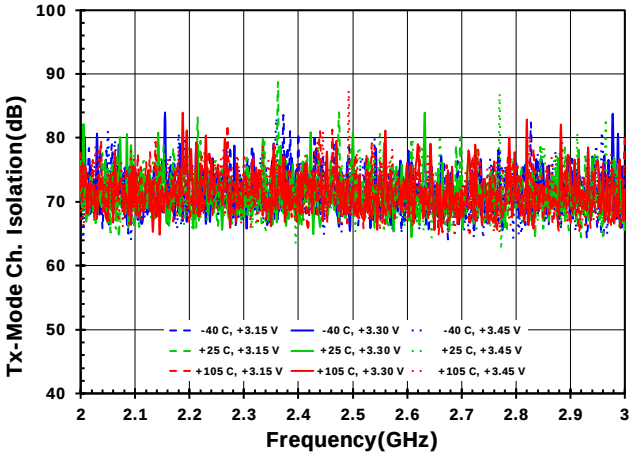


Figure 17. Tx Mode Input Return Loss

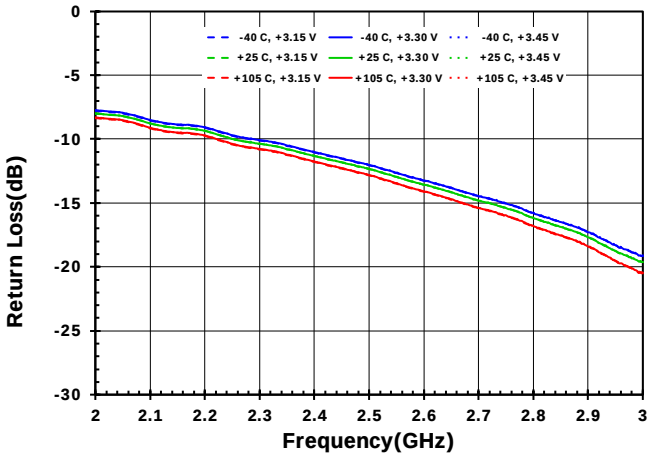


Figure 18. Stability Factor

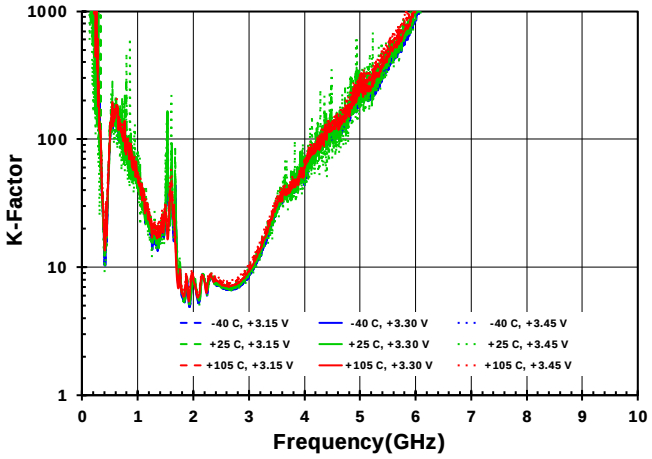


Figure 19. Rx Mode Noise Figure (High Gain)

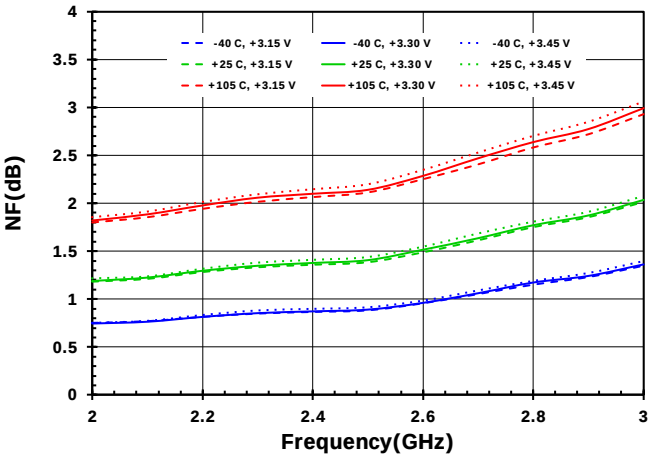
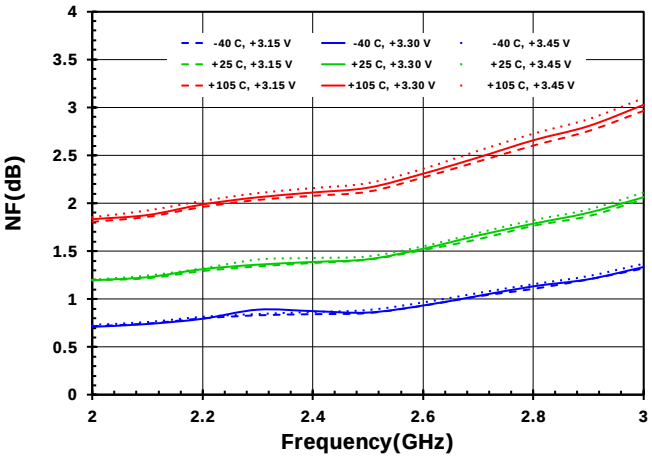


Figure 20. Rx Mode Noise Figure (Low Gain)



Typical Performance Characteristics: Part 4

Figure 21. Switching Time from TX to RX Mode

Figure 22. Switching Time from RX to TX Mode

Figure 23. Standby to RX Mode Transient Time

Figure 24. RX Mode to Standby Transient Time

Figure 25. 6dB Gain Reduction Transient Time

Figure 26. 6dB Gain Increase Transient Time

Programming

Table 8. Gain Step Truth Table

ATT1_CTRL, ATT2_CTRL	Attenuation Setting
Low or NC	0dB
High	6dB

Table 9. Standby and RF Switch Truth Table

In TX Mode, the amplifiers are OFF but the bias will remain ON for fast turn-on recovery time.

STBY	SW_CTRL	MODE	Amplifier State
Low or NC	Low or NC	RX	ON
Low or NC	High	TX	OFF
High	High or Low or NC	STANDBY	OFF

Evaluation Kit Picture

Figure 27. Evaluation Kit: Top View

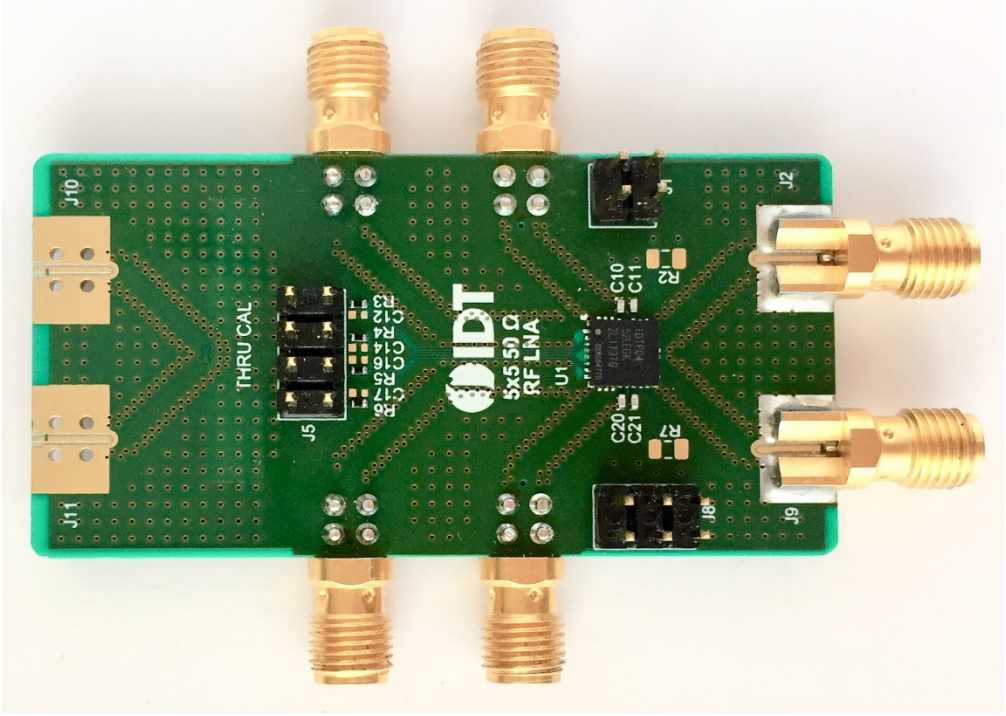
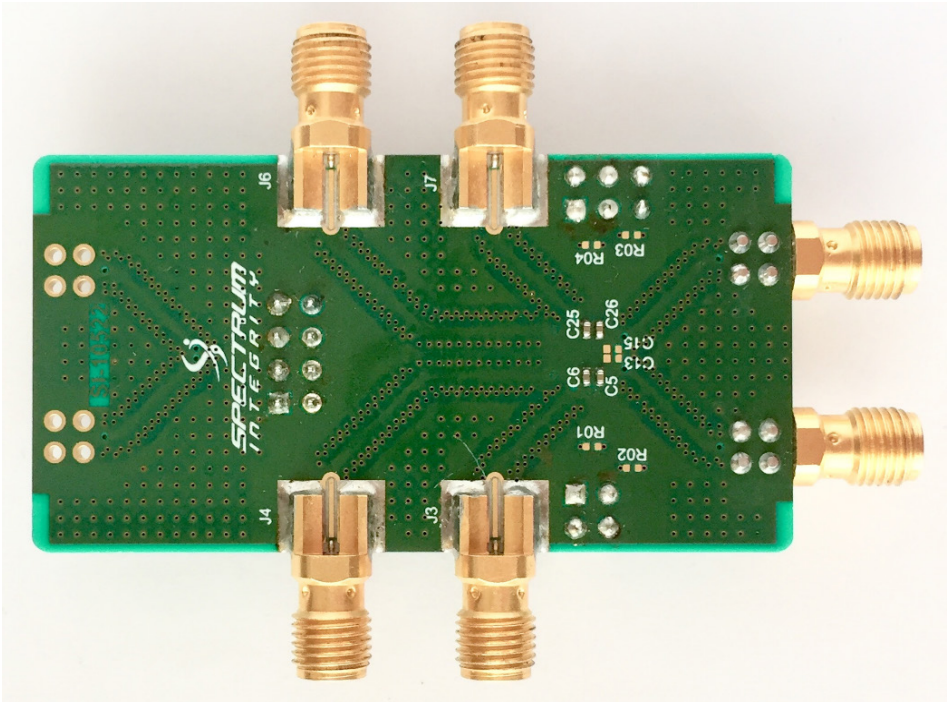


Figure 28. Evaluation Kit: Bottom View



Evaluation Kit / Applications Circuit

Figure 29. Electrical Schematic

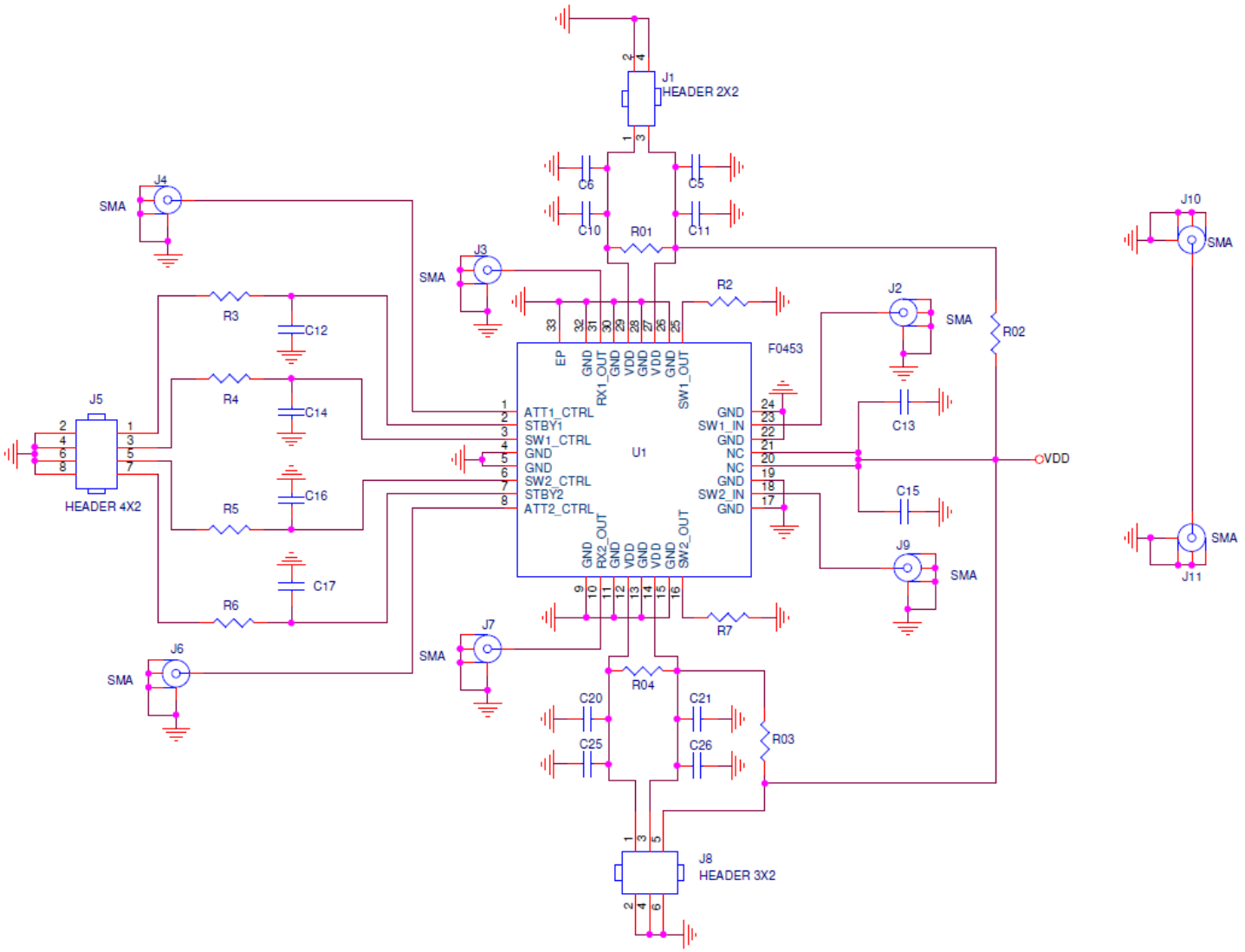


Table 10. Bill of Material (BOM)

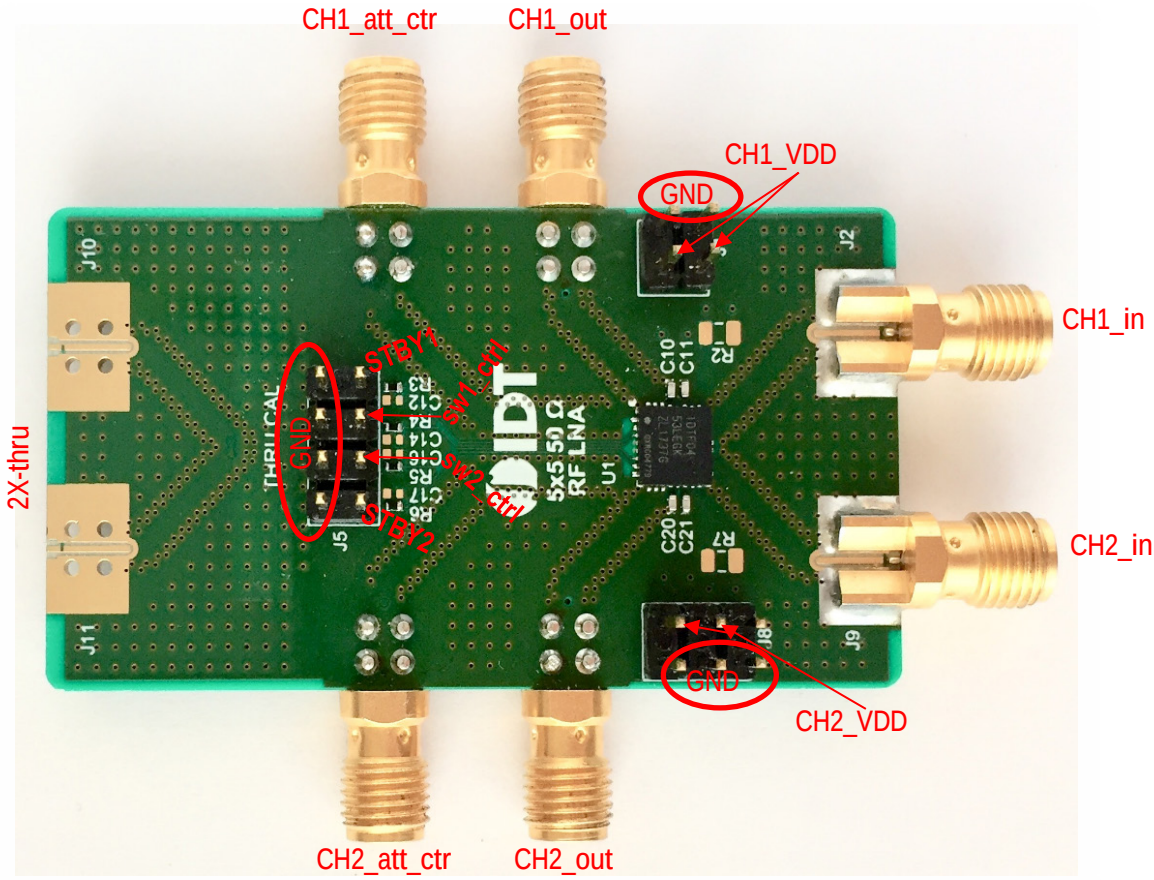
Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
R3, R4, R5, R6	4	0Ω Jumper 1/10W	ERJ2GE0R00X	Panasonic
R2, R7	2	50Ω termination (0805)	PCAN0805E49R9BST5	VISHAY
C10, C11, C20, C21	4	Cap 8pF (0402)	GRM1555C1H8R0DA01D	Murata
C5, C6, C25, C26	4	Cap 1µF, 10V, X5R (0402)	GRM155R61A105KE15D	Murata
J5	1	2x4 Pin Header	67996_108HLF	Digi-Key/Amphenol FCI
J1	1	2x2 Pin Header	67996-104HLF	Digi-Key/Amphenol FCI
J8	1	2x3 Pin Header	67996-106HLF	Digi-Key/Amphenol FCI
J2, J3, J4, J6, J7, J9, J10, J11	8	SMA Edge Mount	142-0761-881	Cinch Connectivity
C12, C13, C14, C15, C16, C17		Do not install		
U1	1	Dual Path RF Switch with LNA and DVGA 5X5 QFN	F0452ZL LEG32K	Renesas (IDT)
SI 10522	1	Printed Circuit Board	F0452 EVKIT SI10522	

Evaluation Kit Operation

Power Supply Setup

Set up a power supply in the voltage range of 3.15V to 3.45V with the power supply output disabled. The voltage is applied by wiring to Pin 1 and 3 of header J1 for CH1_VDD, and wiring to Pin 1 and 3 of header J8 for CH2_VDD, as displayed in Figure 30.

Figure 30. Connections of Evaluation Board



Standby (STBY) Pin

The Evaluation Board can control the F0452 for standby operation. On header J5, the standby pins are pin 2 for CH1 and pin 8 for CH2 as shown in Figure 30. Ground (logic LOW) pins are available to make a connection with a jumper. VDD (logic HIGH) could be wired either from CH1_VDD of header J1 or CH2_VDD of header J8.

To place channel 1 in the normal operation mode (on), use one of the following options:

- Keep STBY1 open by making no connection on pin 2 of J5
- Apply a logic LOW signal to STBY1 by making a connection between pin 1 and pin 2 of J5

To place channel 1 in the standby mode (off), apply a logic HIGH signal to the STBY1 by making a connection between pin 2 of J5 and pin 1 (or pin 3) of J1.

To place channel 2 in the normal operation mode (on), use one of the following options:

- Keep STBY2 open by making no connection on pin 8 of J5
- Apply a logic LOW signal to STBY2 by making a connection between pin 7 and pin 8 of J5

To place channel 2 in the standby mode (off), apply a logic HIGH signal to the STBY2 by making a connection between pin 8 of J5 and pin 1 (or pin 3) of J8.

Gain Step Control Setup

To get 6dB gain attenuation for channel 1, make a connection of SMA Connector J4, marked as “CH1_att_ctr” in Figure 30, to logic HIGH (see Table 8). In contrast, if J4 is open or logic LOW the minimum attenuation is obtained for channel 1.

To get 6dB gain attenuation for channel 2, make a connection of SMA Connector J6, marked as “CH2_att_ctr” in Figure 30, to logic HIGH. In contrast, if J6 is open or logic LOW the minimum attenuation is obtained for channel 2.

Switch Control Pin

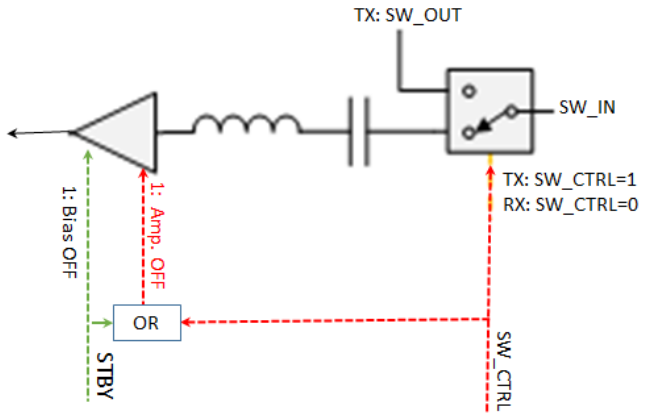
To switch channel 1 into TX throw, make a connection of pin 4 of J5, marked as “sw1_ctr” in Figure 30, to logic HIGH (see Table 9). In contrast, if pin 4 of J5 is open or logic LOW the result is to switch channel 1 into RX throw.

To switch channel 2 into TX throw, make a connection of pin 6 of J5, marked as “sw2_ctr” in Figure 30, to logic HIGH. In contrast, if pin 6 of J5 is open or logic LOW the result is to switch channel 2 into RX throw.

Mode Control Setup

There are three operation modes as displayed in Table 9Error! Reference source not found.. Based on each mode, set up the standby pin and switch control pin as described in Standby (STBY) Pin and in Switch Control Pin. The standby and switch control logic are displayed in the following figure.

Figure 31. Standby and Switch Control Logics



Power-On Procedure

Set up the voltage supplies and Evaluation Board as described in Power Supply Setup with the Standby (STBY) Pin set for open or logic LOW, then enable the power supply.

Power-Off Procedure

Disable the power supply.

Application Information

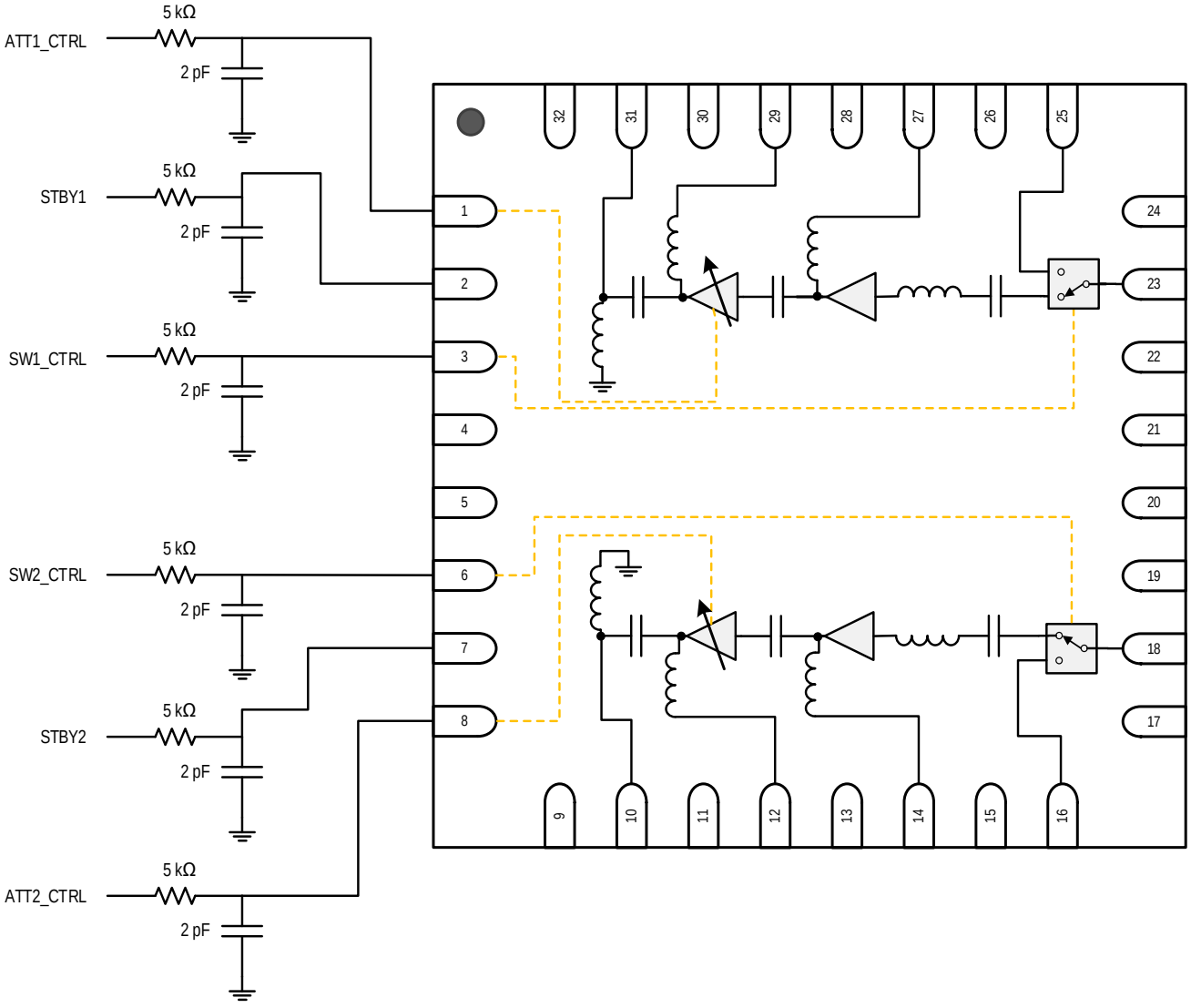
Power Supplies

A common V_{DD} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade the noise figure, and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V / 20µs. In addition, all control pins should remain at 0V (±0.3V) while the supply voltage ramps up or while it returns to zero.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 1, 2, 3, 6, 7, and 8 displayed in Figure 32.

Figure 32. Control Pin Interface Schematic



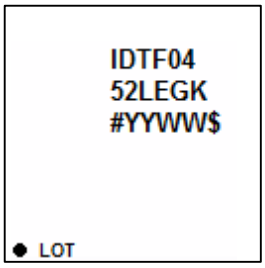
Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see package links in Ordering Information). The package information is the most current data available and is subject to change without revision of this document.

Ordering Information

Part Number	Package Description	MSL Rating	Carrier Type	Temp. Range
F0452LEGK	5.0 × 5.0 × 0.8 mm 32-LGA	MSL3	Tray	-40° to +105°C
F0452LEGK8	5.0 × 5.0 × 0.8 mm 32-LGA	MSL3	Reel	-40° to +105°C
F0452EVBK	Evaluation Board			

Marking Diagram



- Lines 1 and 2 indicate the part number
- Line 3 indicates the following:
  - "#" denotes stepping
  - "YY" is the last two digits of the year; "WW" is the work week number when the part was assembled.
  - "$" denotes the mark code.

Revision History

Revision Date	Description of Change
July 13, 2021	• Updated the maximum value of V_{IL} specification in Table 4. • Completed other minor changes
January 23, 2019	Initial release.