F5268

26GHz 8-Channel, Half-Duplex Transceiver IC

The F5268 is an 8-channel half-duplex transceiver (TRX) silicon integrated circuit (IC) designed using a SiGe BiCMOS process for dual-polarization 5G phased-array applications at the n258 band. The core IC has highly flexible gain and phase control on each channel to achieve fine beam steering and gain compensation between radiating channels.

The F5268 includes a standard SPI protocol that operates up to 95MHz with fast beam switching and fast beam-state loading. Up to 16 devices can be supported on the same SPI bus using dedicated address pins. Each device uses a 2.5V analog supply and a 2.5V-3.3V programmable PA supply to provide TX power modes. The digital core and SPI use a 1.8V supply generated by an on-chip LDO.

Competitive Advantage

- High integration and minimal footprint
- High TX linear output power for 5G NR waveforms
- Low RX noise figure across the frequency band
- Low power consumption
- Fast and flexible beam state programming and loading with high beam state memory count
- Fast TDD switching

Applications

- 5G Single/Dual-Polarization Phased-Array Antenna System, Beam Steering, and similar applications

Features

- 24.25 to 27.5 GHz operation (5G NR n258)
- 8 radiation channels
- 100ns typical TX/RX mode switching time
- 20ns typical gain and phase settling time
- 1.2°/1.7° typical TX/RX RMS phase error
- 0.18dB/0.13dB typical TX/RX RMS gain step error
- 30.5dB gain attenuation range
- Integrated PTAT, PTAT2, and Bandgap generator
- Internal temperature sensor and power detector
- 4-bit chip address (hard-wired/programmable)
- Up to 95MHz SPI control
- 2048 on-chip programmable beam states
- Analog supply voltage: +2.4V to +2.6V
- Dedicated PA supply voltage: selectable between +2.4V to +2.6V and +3.0V to +3.3V
- 5.1 × 5.1 × 0.8 mm, 118-FCCSP package
- -40°C to +95°C operating temperature range

Typical Application Diagram

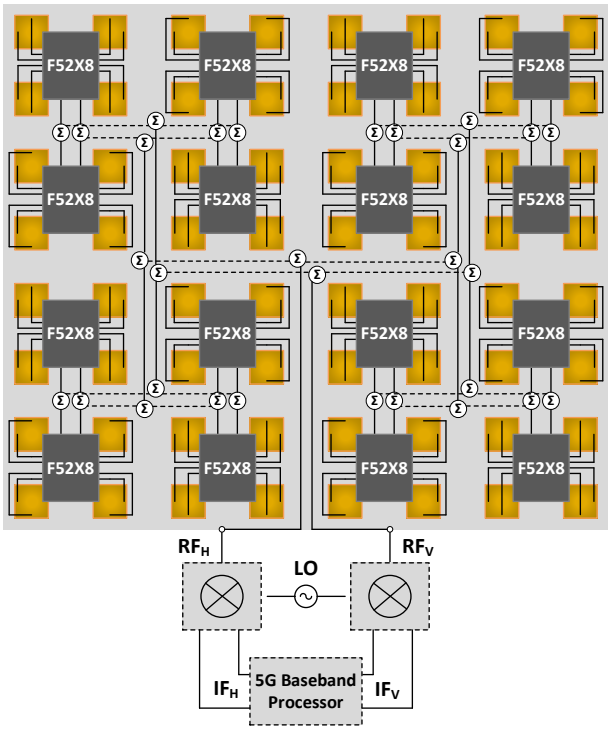

Figure 1. Typical 5G Dual-Polarization Phased-Array Antenna System

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1. Overview

1.1 Block Diagram

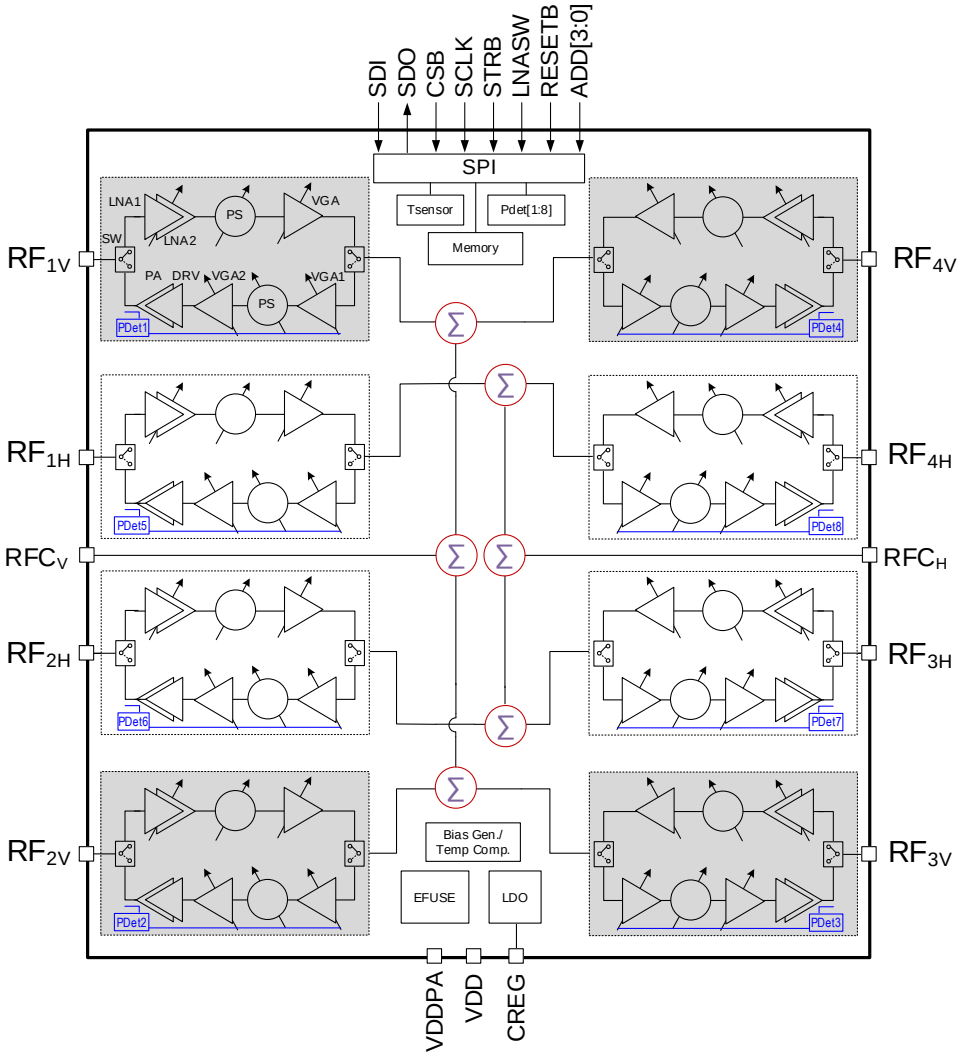


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments

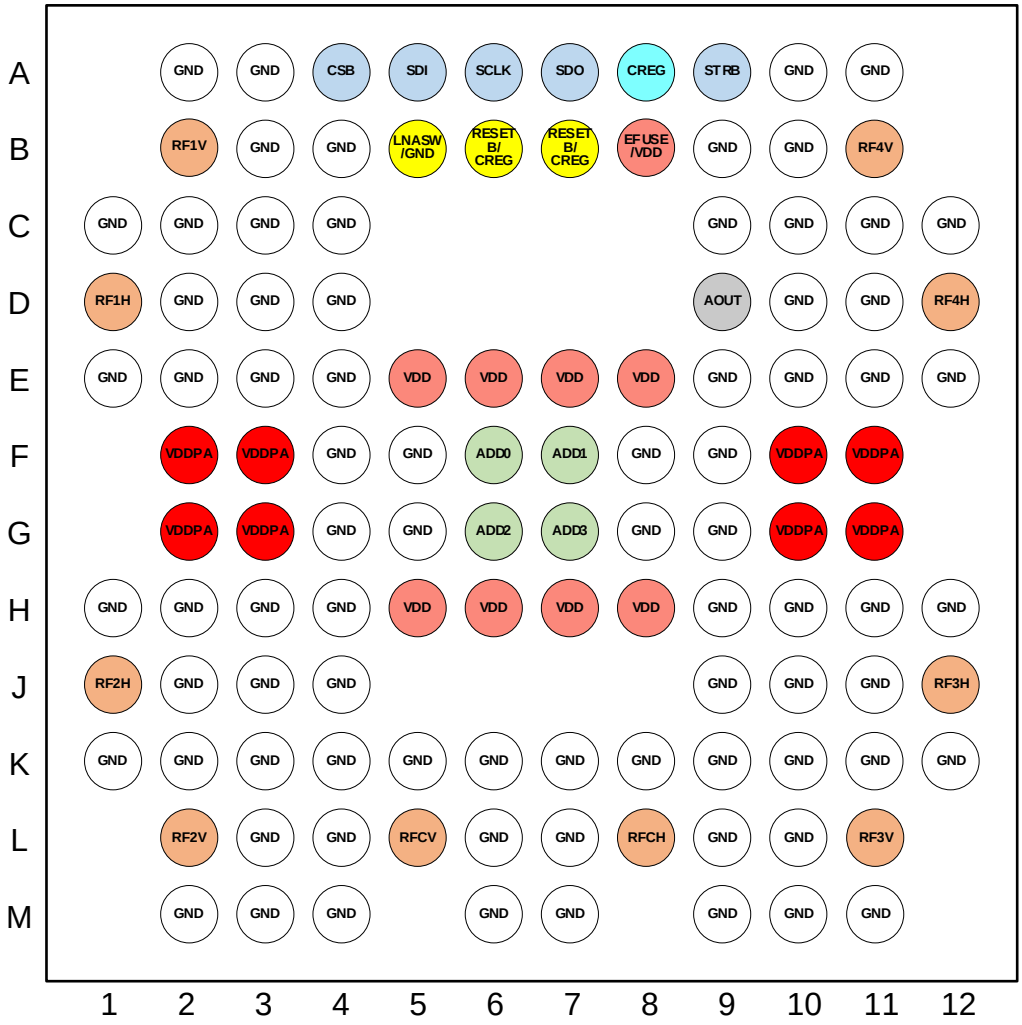


Figure 3. Pin Assignments – Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Type	Description
A4	CSB	Digital Input (PU)[1]	Chip select. 1.8V logic compatible.
A5	SDI	Digital Input (PD)	SPI data input. 1.8V logic compatible.
A6	SCLK	Digital Input (PD)	SPI clock. 1.8V logic compatible.
A7	SDO	Digital Output	SPI data output. 1.8V logic compatible.
A8	CREG	Analog Output	Internal 1.8V digital power supply node (generated by an internal LDO). Require an external capacitor (10µF) to ground.
A9	STRB	Digital Input (PD)	Digitally programmable strobe pin.
B2	RF1V	RF Input/Output	Vertical polarization channel 1.

Pin Number	Pin Name	Type	Description
B5	LNASW/ GND	Digital Input (PD)	RX Linearity mode direct control. 0 = set gain attenuation, 1 = max gain. Gain attenuation adjustable through register control setting. Should be connected to ground if not used.
B6, B7	RESETB/ CREG	Digital Input (PU)	Chip reset. 1 = operation mode, 0 = reset digital/memory to power-on reset default. Connected to CREG if not used.
B8	EFUSE/ VDD	Analog Input	EFUSE programming supply voltage pin for write operation (internal use only). For read operation, connect to VDD.
B11	RF4V	RF Input/Output	Vertical polarization channel 4.
D1	RF1H	RF Input/Output	Horizontal polarization channel 1.
D9	AOUT	Analog Output	Analog DC voltage test port for power detector or temperature sensor measurement. Output selection is controlled through a register setting. This pin can be grounded or left floating if not used.
D12	RF4H	RF Input/Output	Horizontal polarization channel 4.
E5, E6, E7, E8, H5, H6, H7, H8	VDD	Analog Input	2.5V analog power supply.
F2, F3, F10, F11, G2, G3, G10, G11	VDDPA	Analog Input	2.5V/3.3V analog power supply for PA.
F6	ADD0	Digital Input (PU)	Chip address bit 0.
F7	ADD1	Digital Input (PU)	Chip address bit 1.
G6	ADD2	Digital Input (PU)	Chip address bit 2.
G7	ADD3	Digital Input (PU)	Chip address bit 3.
J1	RF2H	RF Input/Output	Horizontal polarization channel 2.
J12	RF3H	RF Input/Output	Horizontal polarization channel 3.
L2	RF2V	RF Input/Output	Vertical polarization channel 2.
L5	RFCV	RF Input/Output	Vertical polarization common port.
L8	RFCH	RF Input/Output	Horizontal polarization common port.
L11	RF3V	RF Input/Output	Vertical polarization channel 3.
A2, A3, A10, A11, B3, B4, B9, B10, C1, C2, C3, C4, C9, C10, C11, C12, D2, D3, D4, D10, D11, E1, E2, E3, E4, E9, E10, E11, E12, F4, F5, F8, F9, G4, G5, G8, G9, H1, H2, H3, H4, H9, H10, H11, H12, J2, J3, J4, J9, J10, J11, K1, K2, K3, K4, K5, K6, K7, K8, K9, K10, K11, K12, L3, L4, L6, L7, L9, L10, M2, M3, M4, M6, M7, M9, M10, M11	GND	Ground	Ground pins.

1. Pull-up (PU) and pull-down (PD) resistors, if applicable, are indicated in parentheses.

3. Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F5268 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions can affect device reliability.

Parameter	Symbol	Condition	Minimum	Maximum	Unit
Analog Supply Voltage	V_{DD}	-	-0.3	+3.0	V
PA Supply Voltage	V_{DDPA}	-	-0.3	+3.3	V
CSB, SDI, SCLK, STRB, LNASW, RESETB, ADD0, ADD1, ADD2, ADD3	V_{CTL}	-	-0.3	+2.1	V
TX Mode RF Common Port Input Power	P_{ABS_TX}	CW, 10s single event V_{DD} = +2.5V, V_{DDPA} = +2.5V and +3.3V, T_{AMB} = +95°C	-	+15	dBm
RX Mode RF Channel Input Power	P_{ABS_RX}	CW, No damage for at least 2 hours V_{DD} = +2.5V, V_{DDPA} = +2.5V and +3.3V, T_{AMB} = +95°C	-	+10	dBm
Maximum Junction Temperature	T_J	-	-	150	°C
Power Dissipation	P_D	-	-	7	W
Storage Temperature Range	T_{ST}	-	-40	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}	-	-	+220	°C

3.2 ESD Ratings

ESD Model/Test	Symbol	Rating	Unit
Human Body Model (Tested per JS-001-2012)	V_{HBM}	2500	V
Charged Device Model (Tested per JESD-C101)	V_{CDM}	250	V

3.3 Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Analog Supply Voltage	V_{DD}	-	+2.4	+2.5	+2.6	V
PA Supply Voltage	V_{DDPA}	Default power mode	+2.4	+2.5	+2.6	V
		High power mode	+3.0	-	+3.3	
Operating Temperature Range[1]	T_{AMB}	Ambient temperature	-40	-	+95	°C
Operating Junction Temperature	T_J	-	-	-	+125	°C
RF Frequency Range	f_{RF}	-	24.25	-	27.5	GHz
RF Pin Impedance	Z_{RF}	-	-	50	-	Ω

1. The operating temperature does not reflect the junction temperature.

3.4 Electrical Characteristics – General

See the F5268 Application Circuit (see Figure 1). Specifications apply when operated with V_{DD} = V_{DDPA} = +2.5V, T_{AMB} = +25°C, f_{RF} = 26GHz, Z_S = Z_L = 50Ω, and with EVB trace and connector losses de-embedded unless otherwise noted.

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Unit
Logic Input High Voltage	V_{IH}	-		***1.6*** [1]	-	1.8	V
Logic Input Low Voltage	V_{IL}	-		0	-	***0.3***	V
Logic Input Current	I_{IH}, I_{IL}	For each input control pin		***-50***	-	***50***	µA
Logic Output High Voltage [2]	V_{OH}	I_{OH} = -2mA		***1.35***	-	-	V
Logic Output Low Voltage [2]	V_{OL}	I_{OL} = 2mA		-	-	***0.45***	V
Analog Supply Current	I_{VDD}	All channels OFF Internal reference OFF		-	4.2	***7.5***	mA
		All channels OFF Internal reference ON		-	4.8	***8.5***	
		All 8 RX channels ON All 8 TX channels OFF		-	472	***565***	
		All 8 RX channels OFF All 8 TX channels ON	No RF input	-	536	***650***	
			At Pout = 10dBm/CH	-	617	-	
			At Pout = 13dBm/CH	-	627	-	
			At Pout = 20dBm/CH	-	745	-	
PA Supply Current	I_{VDDPA}	All 8 channels OFF Internal reference OFF		-	0.1	-	mA
		All 8 channels OFF Internal reference ON		-	0.1	-	
		All 8 RX channels ON All 8 TX channels OFF		-	0.1	-	
		All 8 RX channels OFF All 8 TX channels ON	No RF input	-	437	***640***	
			At Pout = 10dBm/CH	-	589	-	
			At Pout = 13dBm/CH	-	726	-	
			At Pout = 20dBm/CH	-	1551	-	
TDD Switching Time	SW	RF Switch transition between TX and RX states		-	100	-	ns
		From Standby state		-	100	-	

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain Settling Time	G_{ST}	97% settling time	-	20	-	ns
Phase Settling Time	PH_{ST}	97% settling time	-	20	-	ns
Phase Control Range	PH_{RANGE}	-	-	360	-	deg
Phase Control Resolution	PH_{RES}	6-bit control	-	5.6	-	deg
Temperature Sensor Accuracy	TEMP	After calibration [3]	-5	-	5	°C
SPI Clock Rate	SPI_{CLK}	-	-	-	***65*** / 95 [4]	MHz

1. Items in minimum/maximum columns in ***bold italics*** are confirmed by test. Items in minimum/maximum columns NOT in bold italics are confirmed by design characterization.
2. V_{OH} and V_{OL} parameters are simulated with an estimated load resistance of 1.7kΩ and load capacitance of 8pF.
3. For calibration procedure, refer to section 5.1.
4. SPI write operations are rated up to 95MHz clock speed. Other SPI transactions, including read operation, are rated up to 65MHz clock speed.

3.5 Electrical Characteristics – TX

See the F5268 Application Circuit (see Figure 1). Specifications apply when operated with V_{DD} = V_{DDPA} = +2.5V, T_{AMB} = +25°C, f_{RF} = 26GHz, Z_S = Z_L = 50Ω, in TX mode, and with EVB trace and connector losses de-embedded unless otherwise noted. Minimum and maximum performance over all process corners guaranteed through tuned internal current source by bias register setting change.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	Maximum gain setting	-	31	-	dB
Noise Figure	NF	Maximum gain setting	-	21.1	-	dB
Output P1dB	OP1dB	Maximum gain setting	-	19.4	-	dBm
Output IP3	OIP3	Pout ≈ 10dBm/tone 100MHz / 400MHz spacing Maximum gain setting	-	28 / 30	-	dBm
3GPP-Compliant Linear Output Power	Linear P_{OUT}	5G-NR 400MHz 64QAM CP-OFDM, 120kHz sub-carrier spacing, Output power with 3% EVM	-	13	-	dBm
		5G-NR 400MHz 64QAM CP-OFDM, 120kHz sub-carrier spacing, Output power with 5% EVM	-	14	-	
Adjacent Channel Leakage Ratio	ACLR	5G-NR 400MHz 64QAM CP-OFDM, 120kHz sub-carrier spacing, At 3% EVM P_{OUT}	-	34	-	dBc
RMS Phase Error	PH_{ERR}	Maximum gain setting	-	1.2	-	deg
RMS Gain Error due to Phase Setting	G_{ERR}	Maximum gain setting	-	0.35	-	dB
Gain Control Range	G_{ATT_RANGE}	Monotonic vs. control code	-	30.5	-	dB
Gain Control Resolution	G_{RES}	6-bit control, Gain mode = 1	-	0.5	-	dB

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
RMS Gain Step Error	G_{ERR}		-	0.18	-	dB
Gain Flatness	G_{FLAT}	1GHz range at the center	-	0.5	-	dB
		1GHz range at band edges	-	1.8	-	
Input Return Loss	RL_{IN}	Over VT	-	16.4	-	dB
Output Return Loss	RL_{OUT}	Over VT	4.5	8.8	-	dB
Power Detector Dynamic Range	PD_{RANGE}	Over VT	-5		18	dBm
Power Detector Accuracy	PD_{ACC}	Average power versus process and voltage. Output Return Loss ≥ 3dB.	-	±1.2	-	dB
Reverse Isolation	ISO_{REV}	Maximum gain setting	-	43.6	-	dB
Channel-to-Channel Isolation	ISO_{CH}	Adjacent channels Maximum gain setting	-	40	-	dB

3.6 Electrical Characteristics – RX

See the F5268 Application Circuit (see Figure 1). Specifications apply when operated with V_{DD} = V_{DDPA} = +2.5V, T_{AMB} = +25°C, f_{RF} = 26GHz, Z_S = Z_L = 50Ω, in RX mode, and with EVB trace and connector losses de-embedded unless otherwise noted. Minimum and maximum performance over all process corners guaranteed through tuned internal current source by bias register setting change.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Single Path Gain [1]	G	Maximum gain setting	-	19.2	-	dB
		Linearity Mode 1 [2]	-	16	-	
		Linearity Mode 2	-	12.5	-	
Noise Figure	NF	Maximum gain setting	-	4.8	-	dB
		Linearity Mode 1	-	4.9	-	
		Linearity Mode 2	-	5.6	-	
Input P1dB	IP1dB	Maximum gain setting	-	-29.9	-	dBm
		Linearity Mode 1	-	-28.5	-	
		Linearity Mode 2	-	-25.6	-	

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Input IP3	IIP3	Maximum gain setting Pin = -43dBm/tone, 100MHz / 400MHz spacing	-	-21.8 / -20.7	-	dBm
		Linearity Mode 1 Pin = -43dBm/tone, 100MHz spacing	-	-20.1	-	
		Linearity Mode 2 Pin = -43dBm/tone, 100MHz spacing	-	-17.2	-	
RMS Phase Error	PH_{ERR}		-	1.7	-	deg
RMS Gain Error due to Phase Setting	G_{ERR}		-	0.42	-	dB
Gain Control Range	G_{ATT_RANGE}	Monotonic vs. control code	-	15.5	-	dB
Gain Control Resolution	G_{RES}	5-bit control, Gain mode = 0	-	0.5	-	dB
RMS Gain Step Error	G_{ERR}		-	0.13	-	dB
Gain Flatness	G_{FLAT}	1GHz range at the center	-	0.6	-	dB
		1GHz range at band edges	-	2	-	
Input Return Loss	RL_{IN}	Over VT	8.8	17.3	-	dB
Output Return Loss	RL_{OUT}	Over VT	-	14.6	-	dB
Reverse Isolation	ISO_{REV}	Over VT	-	43.8	-	dB
Channel-to-Channel Isolation	ISO_{CH}	Adjacent channels Maximum gain setting	-	40	-	dB

1. Single path gain (SPG) is the S21 measured between RF_n and RFC ports. For electronic gain (EG), 6dB division loss should be added to the SPG (EG = SPG + 6dB).
2. Refer to section 5.3 for more information regarding Linearity Modes.

3.7 Package Thermal Characteristics

Parameter	Symbol	Value	Unit
Junction to Ambient Thermal Resistance [1]	θ_{JA}	13	°C/W
Junction to Case Thermal Resistance (Case is defined as the top of silicon exposure)	θ_{JC}	2.5	°C/W
Moisture Sensitivity Rating (Per J-STD-020)	-	MSL 3	-

1. Assuming 5 × 5 × 12.7 mm heatsink with 16 fins and 3m/s airflow in JEDEC chamber.

4. Typical Performance Graphs

Unless stated otherwise, V_{DD} = V_{DDPA} = +2.5V, T_{AMB} = 25°C, f_{RF} = 26GHz, and Z_L = Z_S = 50Ω single-ended with internal matching networks on all RF ports. EVB trace and connector losses are de-embedded. Small signal parameters measured with P_{IN_TX} = -25dBm; P_{IN_RX} = -40dBm. All temperatures are referenced to the ambient.

4.1 TX Mode Performance

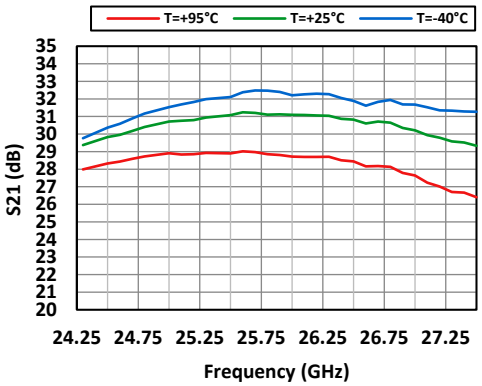


Figure 4. TX Gain

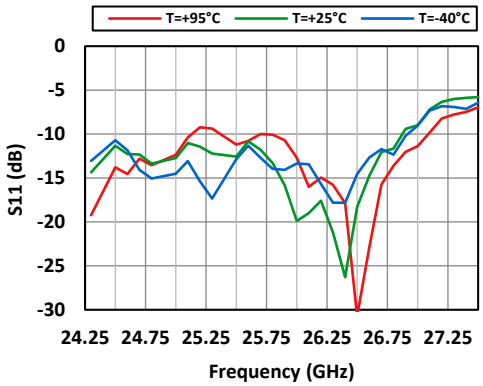


Figure 5. TX Input Return Loss

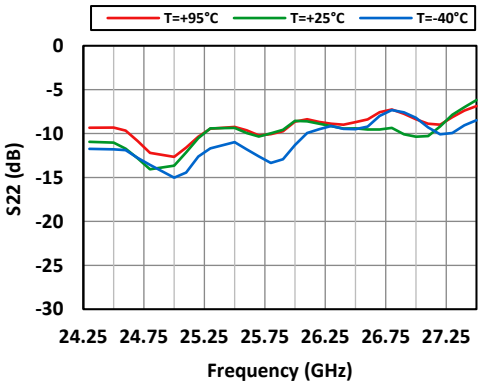


Figure 6. TX Output Return Loss

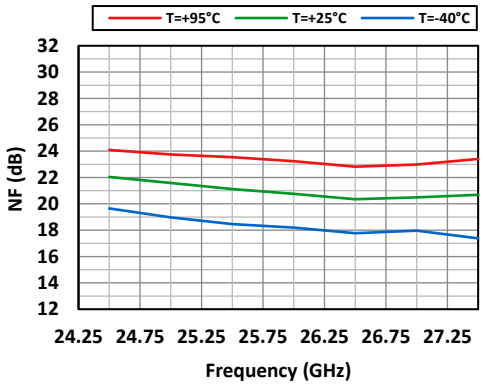


Figure 7. TX Noise Figure

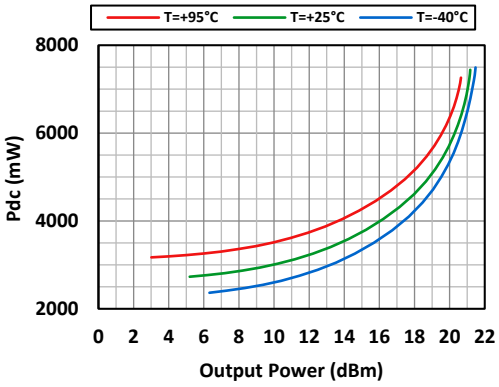


Figure 8. TX DC Power Consumption (Combined VDD and VDDPA), 26GHz Continuous-Wave Signal

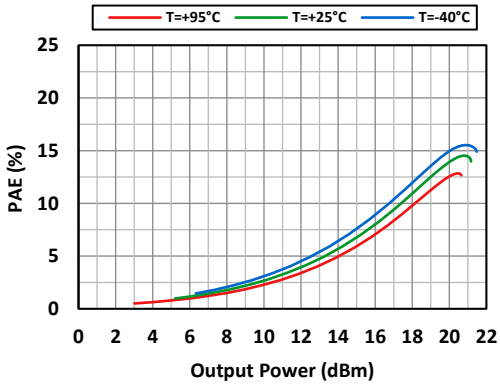


Figure 9. TX PAE, 26GHz Continuous-Wave Signal

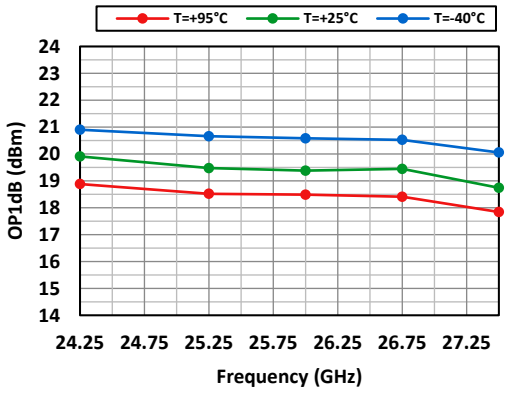


Figure 10. TX OP1dB

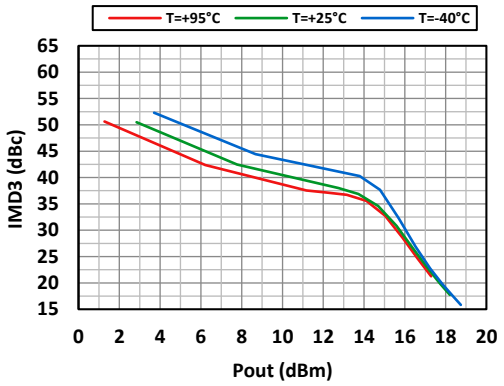


Figure 11. TX IMD3 at 26GHz, 100MHz Spacing

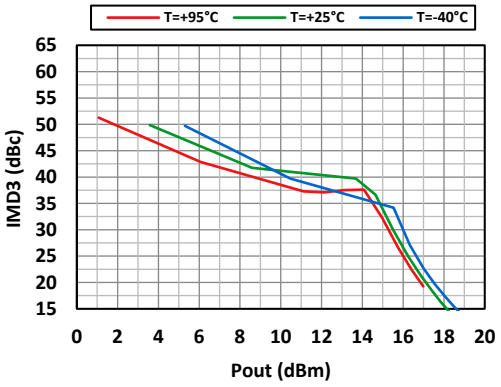


Figure 12. TX IMD3 at 26GHz, 400MHz Spacing

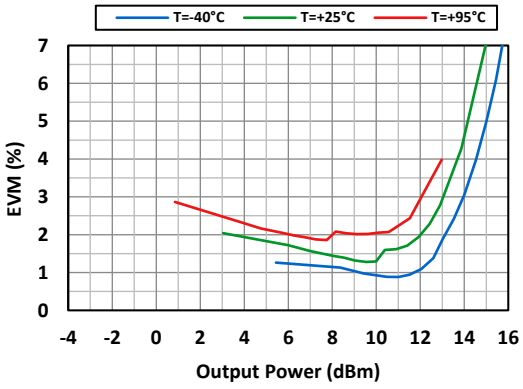


Figure 13. TX EVM at 26GHz (400MHz 64QAM 5G NR)

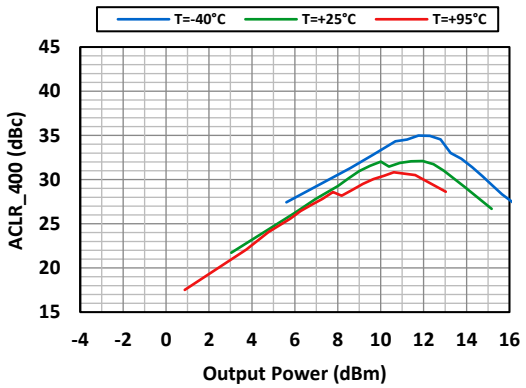


Figure 14. TX ACLR at 26GHz (400MHz 64QAM 5G NR)

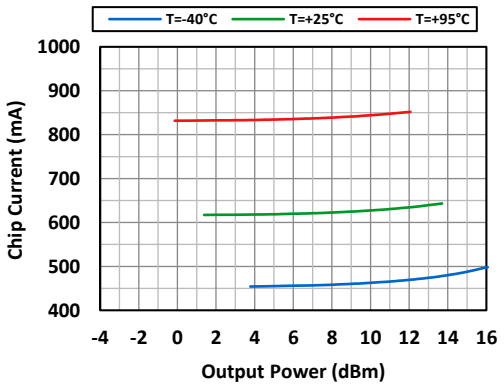


Figure 15. TX VDD Current at 26GHz (400MHz 64QAM 5G NR)

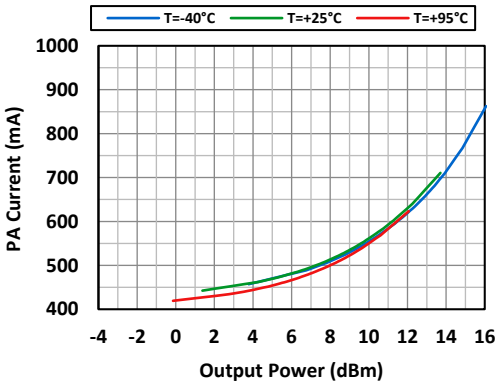


Figure 16. TX VDDPA Current at 26GHz (400MHz 64QAM 5G NR)

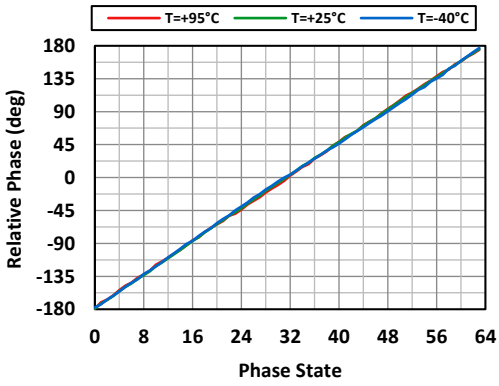


Figure 17. TX Phase Control at 26GHz

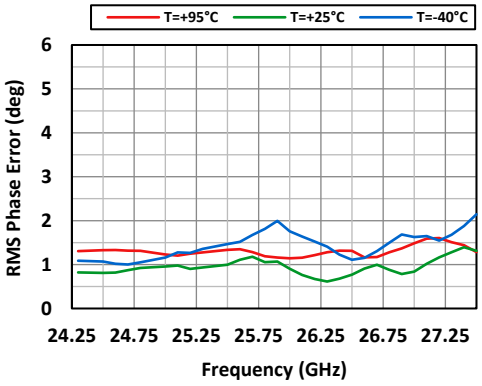


Figure 18. TX Phase Control: RMS Phase Error vs Frequency

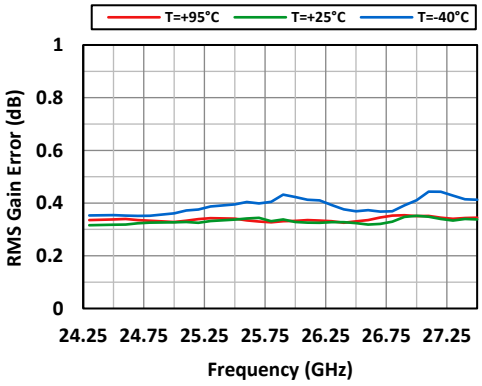


Figure 19. TX Phase Control: RMS Gain Error vs Frequency

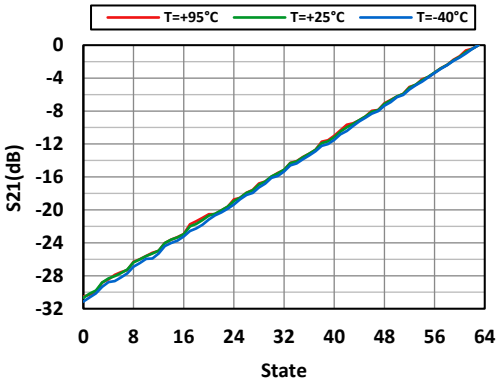


Figure 20. TX Gain Control at 26GHz

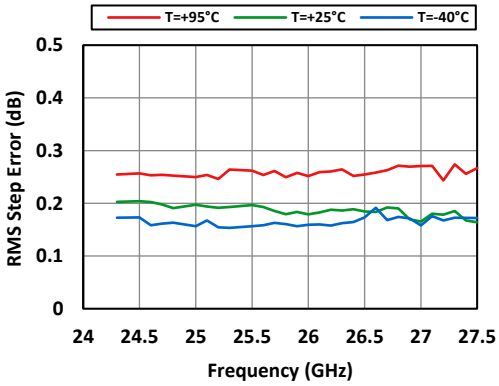


Figure 21. TX Gain Control: RMS Gain Step Error vs Frequency

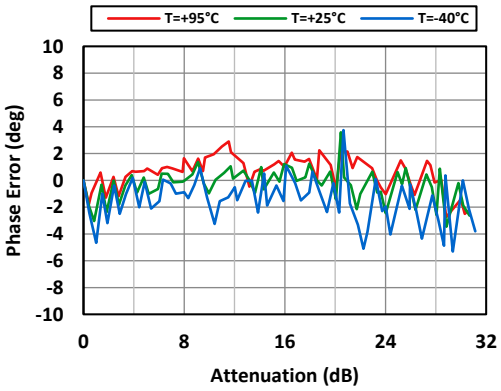


Figure 22. TX Gain Control at 26GHz: Phase Variation

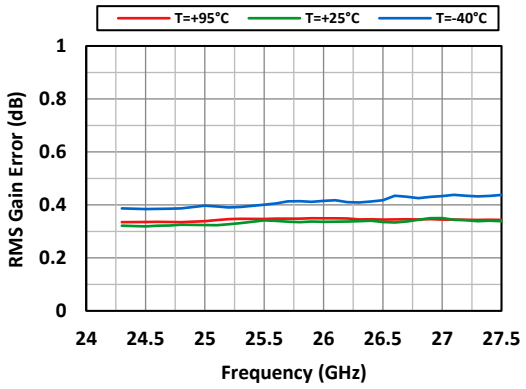


Figure 23. TX Phase Control: RMS Gain Error vs Frequency

4.2 RX Mode Performance

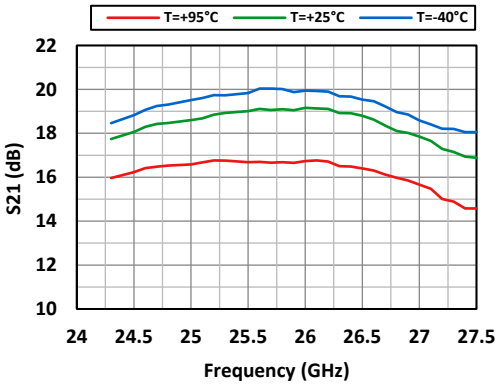


Figure 24. RX Single-Path Gain

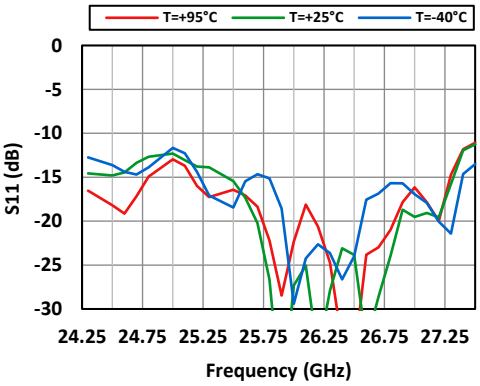


Figure 25. RX Input Return Loss

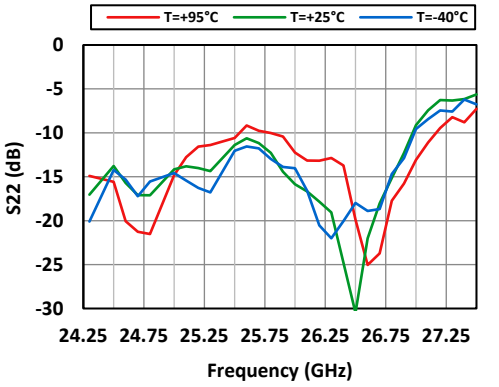


Figure 26. RX Output Return Loss

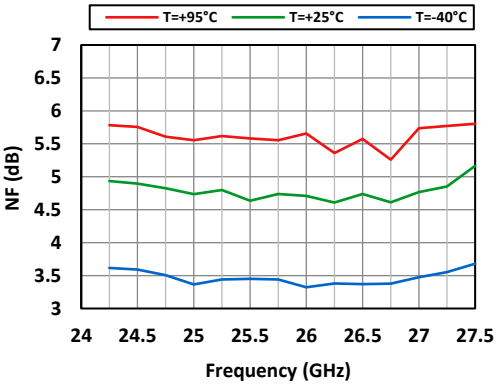


Figure 27. RX Noise Figure

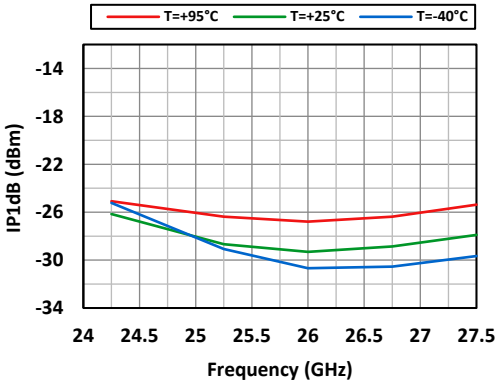


Figure 28. RX IP1dB

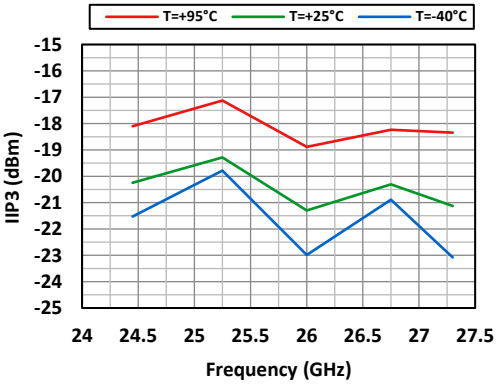


Figure 29. RX IIP3, 100MHz Spacing, -43dBm/Tone

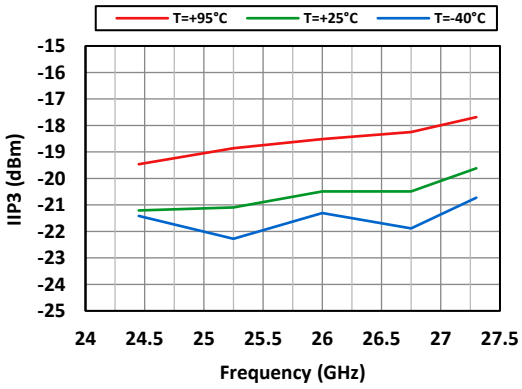


Figure 30. RX IIP3, 400MHz Spacing, -43dBm/Tone

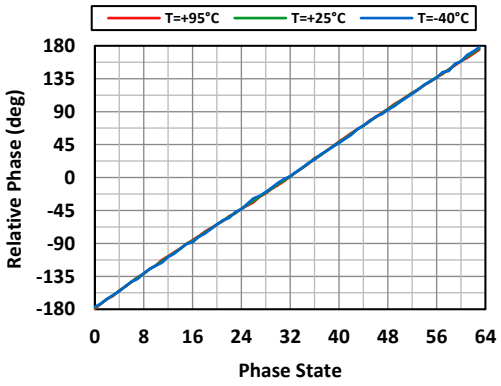


Figure 31. RX Phase Control at 26GHz

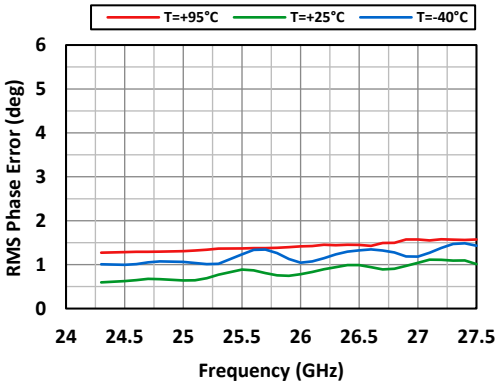


Figure 32. RX Phase Control: RMS Phase Error vs Frequency

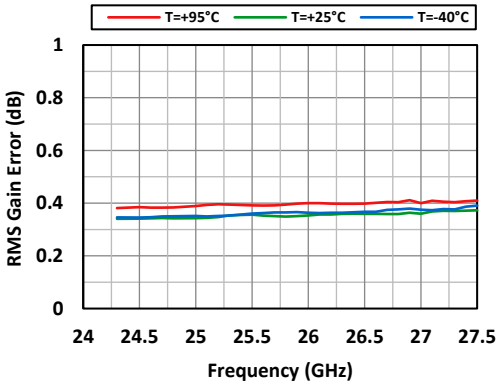


Figure 33. RX Phase Control: RMS Gain Error vs Frequency

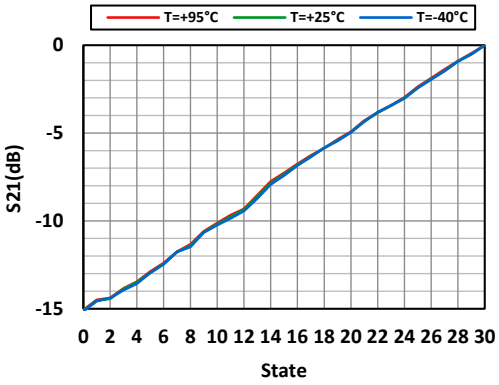


Figure 34. RX Gain Control at 26GHz (High Gain Mode)

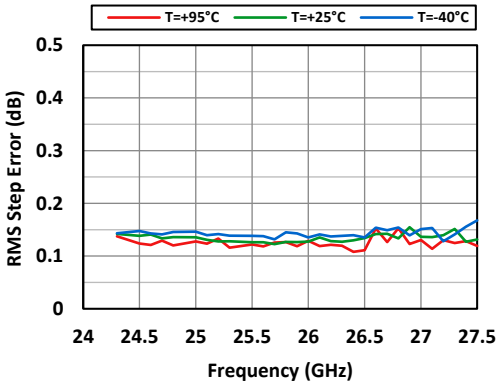


Figure 35. RX Gain Control at 26GHz (High Gain Mode): RMS Gain Step Error vs Frequency

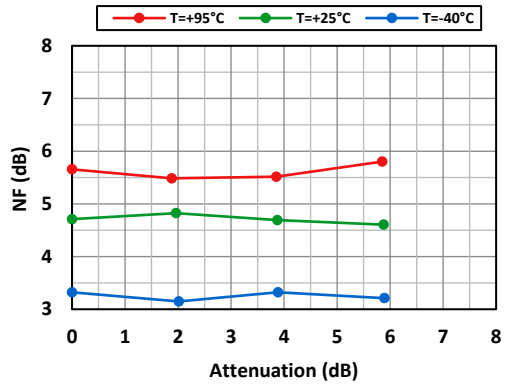


Figure 36. RX Gain Control at 26GHz (High Gain Mode): Noise Figure vs Gain Attenuation

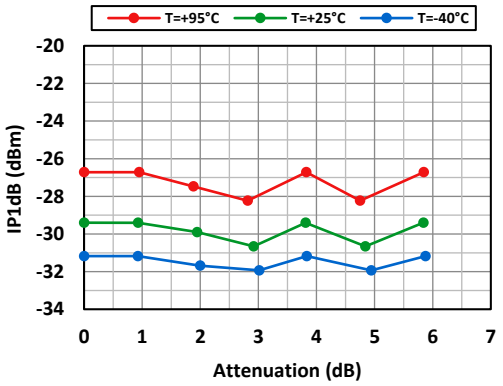


Figure 37. RX Gain Control at 26GHz (High Gain Mode): IP1dB vs Gain Attenuation

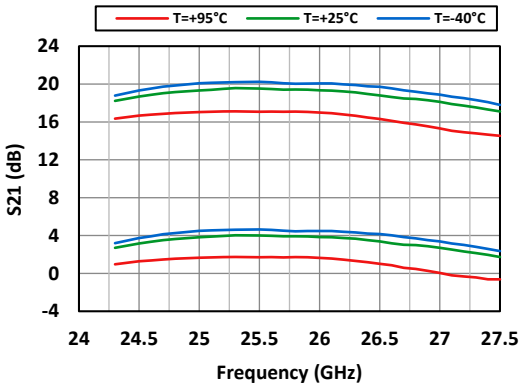


Figure 38. RX High Gain Mode and Low Gain Mode Operation

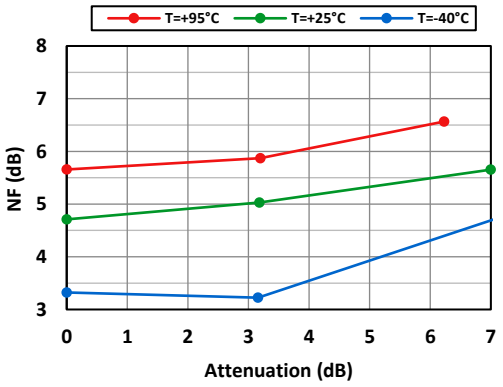


Figure 39. RX Linearity Mode at 26GHz: Noise Figure

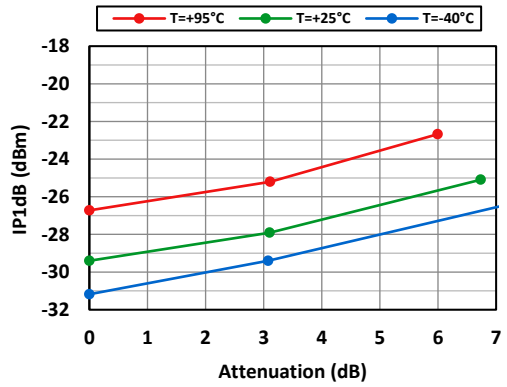


Figure 40. RX Linearity Mode at 26GHz: IP1dB

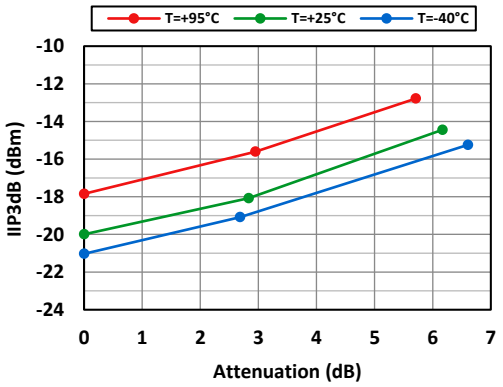


Figure 41. RX Linearity Mode at 26GHz: IIP3, 400MHz Spacing, -43dBm/Tone

5. Functional Description

The F5268 has integrated temperature sensors and power detectors for each TX channel. Selection of the output signal for each sensor is controlled through the SPI interface. These signals can be read through SPI interface using the on-chip ADC. The F5268 can also output an analog signal representation of the temperature sensor or power detector measurements through the AOUT pin. However, the use of the AOUT pin is not suggested for panel implementation or operation. The pin can be grounded or left floating when not used.

5.1 Power Detector and Temperature Sensor

The on-chip temperature sensors provide a measurement range of -40°C to 95°C with an accuracy of ±5°C after calibration. Complete the procedure outlined in “Procedure to Read the Core Temperature Sensor” to operate and access the measurement data through the SPI interface. Note that Register# corresponds to its offset address value in decimal. For the full register information, see “Register Information”.

Calibration needs to be performed at one known temperature only to find the value of $Offset$ for every chip.

$$T_{Sens} = 0.7715 \times Sensor + Offset$$

For example, with the chip in standby mode where the master bias is enabled but all RF channels are OFF, at a known ambient temperature (T_{Amb}), T_{Sens} is approximately T_{Amb}. The value of $Sensor$ is then read from the chip to calculate $Offset$. A typical value for $Offset$ is -263. A lower estimation accuracy of ±25°C is expected if this value is used for all chips without any calibration.

The on-chip power detectors measure the TX output power of each channel. The power detector operates over a wide power range and with modulated signals. Estimation accuracy is within ±0.6dB at room temperature and reduces to ±1.2dB across -40°C to 95°C. Complete the procedures outlined in “Procedure for H-Polarization TX Power Detector Readout” and “Procedure for V-Polarization TX Power Detector Readout” to operate and access the measurement data through the SPI interface. Note that Register# corresponds to its offset address value in decimal. For the full register information, see “Register Information.”

$$P_{TX} = 20 + 1.005 \times 10Log_{10}\left(\frac{Sensor}{1023}\right)$$

5.1.1. Procedure to Read the Core Temperature Sensor

The following example explains how to read values from the core temperature sensor:

1. Enable the temperature sensor and select the core sensor: write 1100h to Register#6.
2. Run the ADC on Temperature Sensor: write 0001h to Register#11 and write 0285h to Register#13.
3. Fetch the temperature sensor result: read bits [9:0] of Register#112.
4. Turn of the ADC and oscillator: write 0204h to Register#13.
5. Disable all temperature sensors: write 0000h to Register#6.

5.1.2. Procedure for H-Polarization TX Power Detector Readout

The following example explains how to read values from the power detectors in TX horizontal channels:

1. Turn on the power detector bias: write 0632h to Register#7.
2. Enable all power detectors for H-polarization channels: write 00F0h to Register#6.
3. Run the ADC on Power Detectors: write F0F0h to Register#12 and write 0285h to Register#13.
4. Fetch the result for horizontal channel 1 (PD_H1): read bits [9:0] of Register#100.
5. Fetch the result for horizontal channel 2 (PD_H2): read bits [9:0] of Register#101.
6. Fetch the result for horizontal channel 3 (PD_H3): read bits [9:0] of Register#102.
7. Fetch the result for horizontal channel 4 (PD_H4): read bits [9:0] of Register#103.
8. Turn off the ADC and oscillator: write 0204h to Register#13.

9. Turn off the power detector bias: write 0630h to Register#7.

5.1.3. Procedure for V-Polarization TX Power Detector Readout

The following example explains how to read values from the power detectors in TX vertical channels:

1. Turn on the power detector bias: write 0632h to Register#7.
2. Enable all power detectors for H-polarization channels: write 000Fh to Register#6.
3. Run the ADC on Power Detectors: write 0F0Fh to Register#12 and write 0285h to Register#13.
4. Fetch the result for vertical channel 1 (PD_V1): read bits [9:0] of Register#96.
5. Fetch the result for vertical channel 2 (PD_V2): read bits [9:0] of Register#97.
6. Fetch the result for vertical channel 3 (PD_V3): read bits [9:0] of Register#98.
7. Fetch the result for vertical channel 4 (PD_V4): read bits [9:0] of Register#99.
8. Turn off the ADC and oscillator: write 0204h to Register#13.
9. Turn off the power detector bias: write 0630h to Register#7.

5.2 Look-Up Table (LUT)

The LUT is used for Fast Beam Steering Mode, which allows fast programming to a specific beam state at the chip or system level. The F5268 has two dedicated LUTs, VLUT and HLUT, for vertical and horizontal polarization respectively, with 1024 beam states each. A single LUT address points to four 16-bit register locations (equivalent to four channels) that contain programmable phase and gain settings. The phase and gain settings for 1 LUT entry constitute a beam state. Each beam state can be either TX or RX, and once selected, LUT data will be loaded simultaneously to all four channels. There is no provision to load to selected channels. Latch capability is also implemented in the protocol such that the LUT information can be buffered to be loaded to channels later. For more information, see “Programming.”

Table 1. Example LUT Entry

LUT Address	Channel	Name	Bit	Field
0x00	00b = 1	CH1_PS	15:8	CH1 Phase Shifter Control
		CH1_VGA	7:0	CH1 VGA Gain Control
	01b = 2	CH2_PS	15:8	CH2 Phase Shifter Control
		CH2_VGA	7:0	CH2 VGA Gain Control
	10b = 3	CH3_PS	15:8	CH3 Phase Shifter Control
		CH3_VGA	7:0	CH3 VGA Gain Control
	11b = 4	CH4_PS	15:8	CH4 Phase Shifter Control
		CH4_VGA	7:0	CH4 VGA Gain Control

5.3 Linearity Modes

The device includes linearity modes that reduce the RX channel gain through single-gain steps. Gain reduction is performed at the input stage of the RX channel to further improve RX channel input-referred linearity. Mode setting and control are configured by RX_LinMode_ExtPinEN and RX_LinMode bits of RXV_LNA (0x21) and RXH_LNA (0x31) registers for vertical and horizontal polarization respectively (for linearity mode settings, see Table 2). The LNASW pin (ball B5) can be used to toggle between maximum gain mode and linearity mode if enabled through the RX_LinMode_ExtPinEN bit (see section 6.2).

Table 2. Linearity Modes

Modes	RX_LinMode	Attenuation (dB)
Maximum Gain Mode	0	0
Linearity Mode 1	1 or 2 (either LNA1 or LNA2 attenuation)	3
Linearity Mode 2	3 (both LNA1 and LNA2 attenuation)	6

6. Control Mode

6.1 Strobe Pin Control

The external STRB pin (pin A9) acts as an asynchronous request, which can change configuration of all the chips in the panel with a single pulse. By setting the register bits CTRL_CFG.STROBE_PROG (or CTRL_CFG[6:4]), the STRB pin can be configured to function as a latch control pin, a V/H TRX toggle pin, or a V/H LUT increment pin for fast beam scanning control. To avoid interfering with regular SPI operation, this strobe function is executed only when the CSB signal is high.

Table 3. STRB Pin Function Setting

CTRL_CFG.STROBE_PROG Bits	Strobe Function
000	Latch mode
001	V TRX toggle
010	H TRX toggle
011	H and V TRX toggle
100	V LUT increment (enabled RX/TX)
101	H LUT increment (enabled RX/TX)
110	H and V LUT increment (enabled RX/TX)

6.1.1. Latch Mode

In this mode, when a strobe pulse is inserted, all the buffers are latched to their respective channel registers at the strobe pulse's positive edge. As a use-case example, suppose the device is currently operating in TXH mode and it is desired to switch to RXH mode at a future time. The RXH related settings in all the devices can be loaded to the buffers in advance. A single strobe pulse can then reconfigure all the chips when the TRX switching is desired.

6.1.2. TRX Toggle

In TRX toggle mode, if any of the buffers for registers 0x0 to 0x2 differ from their registers, the strobe pulse will latch the buffers to their registers. Thus, the desired program mode, TRX mode, and the effective pointer registers become effective. The subsequent strobe pulse then toggles the TRX bit in CTRL_CFG and HLUT/VLUT registers and it becomes effective immediately. If the buffers are already the same as their respective registers, however, TRX toggle will happen in the first strobe pulse.

6.1.3. LUT Increment for Fast Beam Scanning

Similar to the TRX toggle mode, if any of the three buffers differ from their registers, the first strobe pulse will latch the buffers to their registers. In subsequent strobe pulses, the LUT address pointers are incremented and the data is fetched from the selected LUTs at the strobe pulse rising edge. At the strobe falling edge they are loaded to channels.

6.2 LNASW Control

The LNASW pin provides fast switching of the RX input-stage step attenuator. Setting the LNASW pin low reduces the RX gain by the value set by RX_LinMode bits in RXV_LNA and RXH_LNA registers to improve the linearity of the RX. To enable fast linearity switching through the LNASW pin, set the RX_LinMode_ExtPinEN bit in the RXV_LNA and RXH_LNA registers to ‘1’. If fast switching is not used (RX_LinMode_ExtPinEN=0), LNA gain attenuation is fully configured by the RXV_LNA and RXH_LNA registers. In this case it is recommended to ground the LNASW pin.

Table 4. LNASW Control Truth Table

RX_LinMode_ExtPinEN	LNASW Pin	Linearity Mode
0	0	1 (RX_LinMode)
0	1	1 (RX_LinMode)
1	0	1 (RX_LinMode)
1	1	0 (Max gain)

6.3 VGA Gain Attenuation Control

TX VGA gain attenuation is controlled by registers TXVn_SET[7:0] and TXHn_SET[7:0] to provide 30dB dynamic range of gain control for vertical and horizontal channels, respectively. For TX gain control mapping and typical performance, see the following table.

Table 5. TX VGA Gain Attenuation Control (Typical Performance at 26GHz)

Gain Code	Gain (dB)	OP1dB (dBm)	OIP3 (dBm)	NF (dB)
255	31	19.4	30	21.1
249	30.5			
244	30	19.4	29.4	21.8
241	29.5			
236	29	19.4	28.4	22.2
233	28.5			
228	28	19.4	27.7	22.7
225	27.5			
221	27	19.4	27.2	23.1
214	26.4			
210	26	19.4	26.8	23.9
208	25.5			
205	25	19.2	26.5	24.3
198	24.5			
194	24	18.7	26.1	23.5
190	23.3			
187	23	17.9	25.9	24.1
182	22.5			
178	22	17.2	25.4	24.9
172	21.5			
168	20.9	15.9	25	24.4
167	20.6			
162	20	15.1	24.7	25.2
156	19.5			
155	19.2	11.2	24.5	26.9
153	18.5			
146	18	12.8	21.8	23.4
143	17.5			
138	17	11.9	21.6	24.2
137	16.7			
130	16	11	22	28
127	15.5			
123	15	13.1	21.4	27.5
118	14.6			
115	14.1	11.9	19.1	26.2
110	13.5			
104	13	10.8	18.6	27.2
103	12.5			
97	11.9	9.8	17	31.7
94	11.5			
91	11	8.8	16.2	28.5
86	10.5			
80	10	7.9	15.3	33.2
74	9.5			
70	9.1	6.9	13.3	34.1
68	8.3			
66	8.1	6.1	14.6	33.8
63	7.6			
57	7	5.1	13	38
52	6.3			
51	6	3.9	11.8	33.1
44	5.5			
41	5	3.1	10.8	38.3
35	4.4			
32	3.9	1.9	9.8	35.4
28	3.6			
22	3	0.9	7.9	36.2
16	2.4			

RX VGA gain attenuation is controlled by registers RXVn_SET[7:0] and RXHn_SET[7:0] to provide 15dB dynamic range of gain control for vertical and horizontal channels, respectively. The RX channel also features a low-gain mode (by setting RX_GAIN_MODE = 1) that can extend the overall gain control range up to 30dB. For RX gain control mapping and typical performance in high-gain mode, see the following table.

Table 6. RX VGA Gain Attenuation Control in High-Gain Mode (Typical Performance at 26GHz)

Gain Code	Gain (dB)	IP1dB (dBm)	IIP3 (dBm)	NF (dB)
255	19.2	-29.9	-20.7	4.8
247	18.7			
238	18.2	-29.9	-20.9	4.9
230	17.7			
221	17.2	-30.2	-20.9	4.7
213	16.7			
205	16.2	-30.2	-20.6	4.9
197	15.8			
188	15.2	-30.2	-20.9	5
182	14.7			
173	14.2	-30.2	-20.6	5
165	13.7			
155	13.2	-31.4	-22	5
148	12.7			
140	12.2	-30.4	-20.9	5.1
132	11.7			

Gain Code	Gain (dB)	IP1dB (dBm)	IIP3 (dBm)	NF (dB)
124	11.2	-30.9	-21.7	5.1
113	10.7			
105	10.2	-31.4	-22.2	5.1
99	9.7			
89	9.2	-30.6	-21.1	5
83	8.7			
78	8.2	-30.2	-21.5	5.3
66	7.7			
59	7.3	-30.2	-20.6	5.9
55	6.7			
39	6.2	-30.9	-21.2	6.3
37	5.7			
29	5.2	-30.2	-21.1	6.7
17	4.7			
9	4.2	-30.9	-21.2	6.6

6.4 Phase Shifter Control

TX phase shifter is controlled by registers TXVn_SET[15:8] and TXHn_SET[15:8] to provide 6-bit phase control with 360° dynamic range. Two bits are dedicated for process correction as shown in Table 7.

Table 7. TX Phase Shifter Control

D7 (MSB)	D6	D5	D4	D3	D2	Process Correction		Phase Shift (deg)
						D1	D0 (LSB)	
0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	5.6
0	0	0	0	1	0	0	0	11.2
0	0	0	1	0	0	0	0	22.4
0	0	1	0	0	0	0	0	44.8
0	1	0	0	0	0	0	0	89.6
1	0	0	0	0	0	0	0	179.2
1	1	1	1	1	1	0	0	352.8

RX phase shifter is controlled by registers RXVn_SET[15:8] and RXHn_SET[15:8] to provide 6-bit phase control with 360° dynamic range. Two bits are dedicated for process correction as shown in Table 8.

Table 8. RX Phase Shifter Control

Process Correction		D5	D4	D3	D2	D1	D0 (LSB)	Phase Shift (deg)
D7 (MSB)	D6							
0	1	0	0	0	0	0	0	0
0	1	0	0	0	0	0	1	5.6
0	1	0	0	0	0	1	0	11.2
0	1	0	0	0	1	0	0	22.4
0	1	0	0	1	0	0	0	44.8
0	1	0	1	0	0	0	0	89.6
0	1	1	0	0	0	0	0	179.2
0	1	1	1	1	1	1	0	352.8

6.5 RESETB Control

The device can be reset, without power supply cycling, by toggling the RESETB pin from logic high to low. The RESETB pin needs to be asserted back to logic high for normal device operation. During the chip reset, the register contents return to the factory default values.

Table 9. RESETB Control Truth Table

RESETB	State
0	Reset
1	Normal operation

7. Programming

7.1 Serial Peripheral Interface (SPI)

The F5268 uses a standard SPI protocol for synchronous serial communication. The SPI bus consists of four wire signals: Serial Clock (SCLK), Serial Data In (SDI), Serial Data Out (SDO), and Chip Select Bit (CSB). SPI clock operates up to 65MHz and SCLK pin is associated with the clock signal rising edge. For SPI write transactions, SPI clock can be operated up to 95MHz. The input data stream (addresses, commands, messages, and data) is received on the SDI pin, while the output data stream is transmitted from the SDO pin. The SDO pin shows a high-Z impedance level when the chip is in listen mode. The CSB pin acts as a chip-select pin. All SPI bus pins are synchronous and compatible with multi-chip connection.

There are eight general SPI modes defined by the three mode control bits of all SPI commands. Data is loaded with MSB first and transferred to the input register on the rising edges of SCLK.

Table 10. SPI Modes

Mode Control Bits	Mode of Operation	Description
000	LCL_REG_RD	Local Register Read
001	LCL_REG_WR	Local Register Write
010	GBL_LUT_WR	Global LUT Write
011	GBL_REG_WR	Global Register Write
100	GBL_FST_BM_STR	Global Fast Beam Steering
101	LCL_FST_BM_STR	Local Fast Beam Steering
110	LCL_LUT_WR	Local LUT Write
111	LCL_LUT_RD	Local LUT Read

7.1.1. LCL_REG_RD

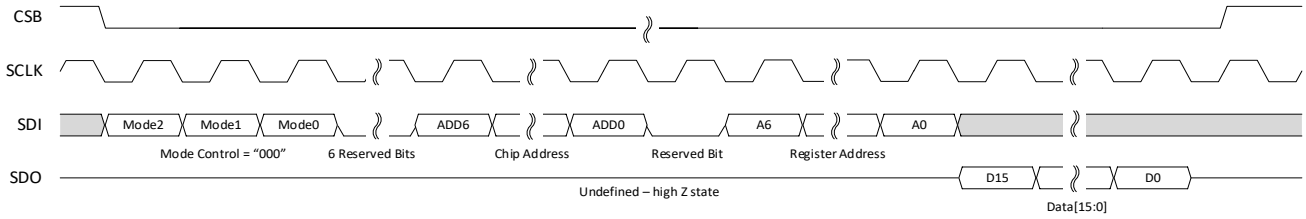


Figure 42. LCL_REG_RD Timing Sequence

Byte1								Byte2								Byte3								Byte4	Byte5
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7 … 0	7 … 0
MODE			Reserved Bits					Chip Address								RES	Register Address							Data Read	
0	0	0	0	0	0	0	0	0	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	0	A6	A5	A4	A3	A2	A1	A0	D15...D8	D7…D0

Figure 43. LCL_REG_RD Command Bit Sequence

Table 11. LCL_REG_RD Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Register Read, mode = 000.
2	6:0	Chip Address	
3	6:0	Register Address	
4	7:0	Data byte 1 – Data[15:8]	Master sends out the SCLK pulses and data is received on the SDO line.
5	7:0	Data byte 2 – Data[7:0]	

7.1.2. LCL_REG_WR

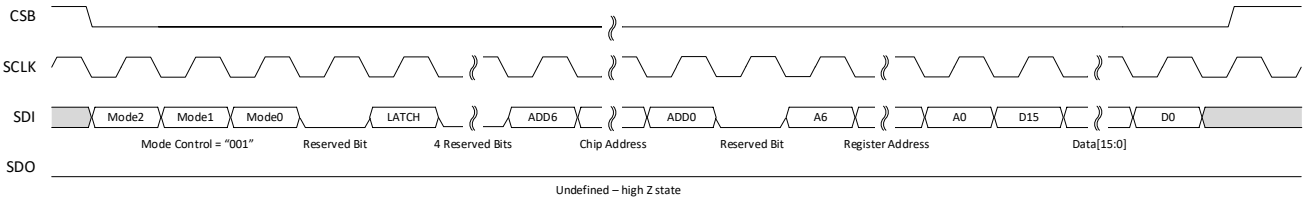


Figure 44. LCL_REG_WR Timing Sequence

Byte1								Byte2								Byte3								Byte4	Byte5
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	15 … 8	7 … 0
MODE			RF Load		Reserved Bits			Chip Address								RES	Register Address							Data	
0	0	1	0	LATCH	0	0	0	0	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	0	A6	A5	A4	A3	A2	A1	A0	D15...D8	D7…D0

Figure 45. LCL_REG_WR Command Bit Sequence

Table 12. LCL_REG_WR Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Register Write, mode = 001.
1	3	Data Latch	0 = Data is written to the buffer. 1 = Data is written to the buffer as well as the register. This also triggers the latch for all other buffered registers on the chip.
2	6:0	Chip Address	
3	6:0	Register Address	
4	7:0	Data byte 1 – Data[15:8]	Data sent on the SDI line will be saved to the buffer or register.
5	7:0	Data byte 2 – Data[7:0]	

7.1.3. GBL_REG_WR

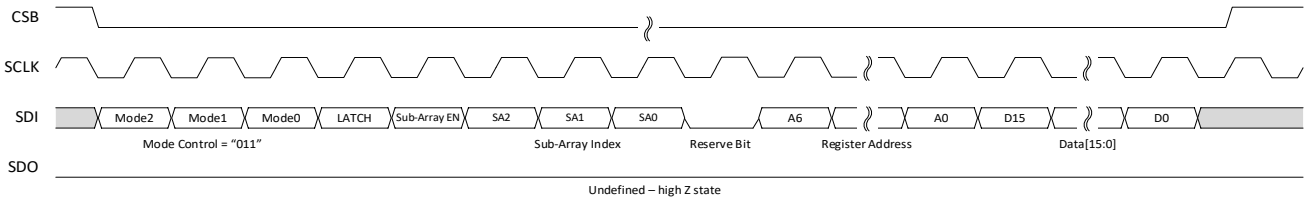


Figure 46. GBL_REG_WR Timing Sequence

Byte1								Byte2								Byte3								Byte4
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	15 … 8
MODE			RF Load	Sub Array Enable	Sub-Array Idx			RES	Register Address							Data								
0	1	1	LATCH	SE	SA2	SA1	SA0	0	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7 … D0

Figure 47. GBL_REG_WR Command Bit Sequence

Table 13. GBL_REG_WR Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Register Write, mode = 011.
1	4	Data Latch	0 = Data is written to the buffer. 1 = Data is written to the buffer as well as the register. This also triggers the latch for all other buffered registers on the chip.
1	3	Sub-Array Enable (SE)	0 = Command executed on all chips. 1 = Commands executed on chips with matching sub-array.
1	2:0	Sub-Array Index	If SE is set, data is written only when this index matches with the chip's sub-array index (stored in register 0x0).
2	6:0	Register Address	
3	7:0	Data byte 1 – Data[15:8]	Data sent on the SDI line will be saved to the buffer or register.
4	7:0	Data byte 2 – Data[7:0]	

7.1.4. LCL_LUT_RD

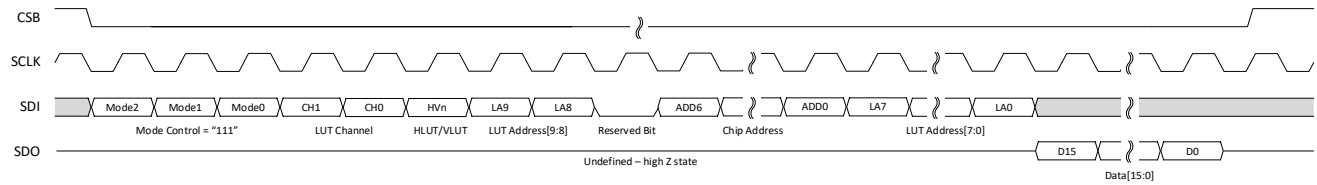


Figure 48. LCL_LUT_RD Timing Sequence

Byte1								Byte2								Byte3								Byte4	Byte5
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7…0	7…0
MODE			LUT Channel		LUT SEL	LUT Address		RES	Chip Address							LUT Address								Data	
1	1	1	CH1	CH0	HVn	LA9	LA8	0	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	D15…D8	D7…D0

Figure 49. LCL_LUT_RD Command Bit Sequence

Table 14. LCL_LUT_RD Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local LUT Read, mode = 111.
1	4:3	Channel Select	Choose between CH0-CH3 to read the data from.
1	2	HVn	0 = Reads from VLUT. 1 = Reads from HLUT.
1	1:0	LUT Address	The 2 MSBs of the LUT address, 9:8.
2	6:0	Chip Address	
3	7:0	LUT Address	The 8 LSBs of the LUT address, 7:0.
4	7:0	Data byte 1 – Data[15:8]	Master sends out the SCLK pulses and data is received on the SDO line.
5	7:0	Data byte 2 – Data[7:0]	

7.1.5. LCL_LUT_WR

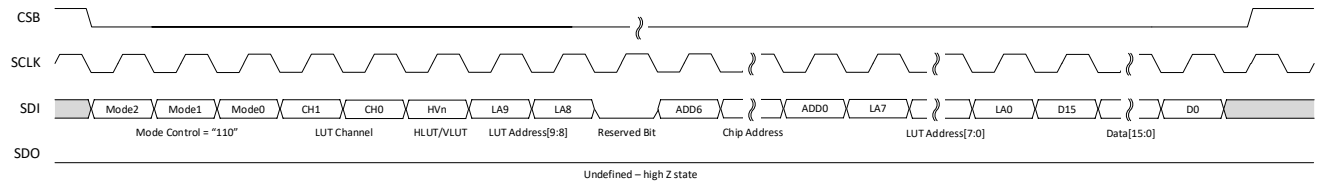


Figure 50. LCL_LUT_WR Timing Sequence

Byte1								Byte2								Byte3								Byte4	Byte5
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	15 … 8	7 … 0
MODE			LUT CH		LUT SEL	LUT Address		Res	Chip Address							LUT Address								Data	
1	1	0	CH1	CH0	HVn	LA9	LA8	0	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	D15…D8	D7 … D0

Figure 51. LCL_LUT_WR Command Bit Sequence

Table 15. LCL_LUT_WR Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local LUT Write, mode = 110.
1	4:3	Channel Select	Choose between CH0 - CH3 to write the data to.
1	2	HVn	0 = Writes to VLUT. 1 = Writes to HLUT.
1	1:0	LUT Address	The 2 MSBs of the LUT address, 9:8.
2	6:0	Chip Address	
3	7:0	LUT Address	The 8 LSBs of the LUT address, 7:0.
4	7:0	Data byte 1 – Data[15:8]	Data sent on the SDI is stored to the selected LUT.
5	7:0	Data byte 2 – Data[7:0]	

7.1.6. GBL_LUT_WR

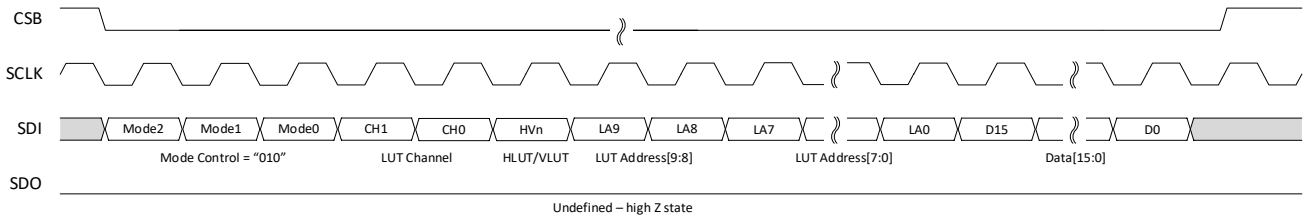


Figure 52. GBL_LUT_WR Timing Sequence

Byte1								Byte2								Byte3								Byte4
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	15 … 8
MODE			LUT Channel		LUT_SEL	LUT Address		LUT Address								Data								
0	1	0	CH1	CH0	HVn	LA9	LA8	LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	D15	D14	D13	D12	D11	D10	D9	D8	D7 … D0

Figure 53. GBL_LUT_WR Command Bit Sequence

Table 16. GBL_LUT_WR Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Global LUT Write, mode = 010.
1	4:3	Channel Select	Choose between CH0-CH3 to write the data to.
1	2	HVn	0 = Writes to VLUT. 1 = Writes to HLUT.
1	1:0	LUT Address	The 2 MSBs of the LUT address, 9:8.
2	7:0	LUT Address	The 8 LSBs of the LUT address, 7:0.
3	7:0	Data byte 1 – Data[15:8]	Data sent on the SDI is stored to the selected LUT.
4	7:0	Data byte 2 – Data[7:0]	

7.1.7. LCL_FST_BM_STR

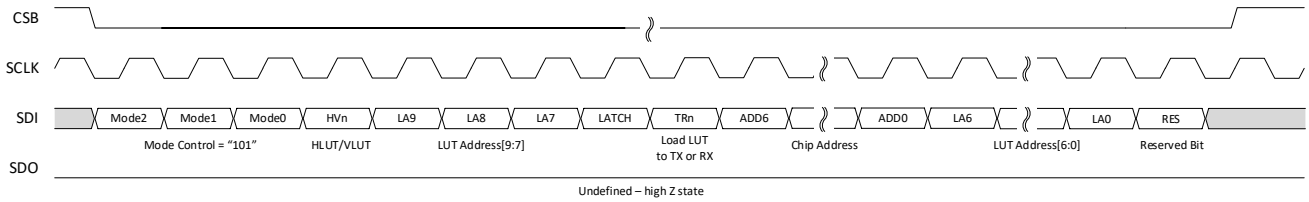


Figure 54. LCL_FST_BM_STR Timing Sequence

Byte1								Byte2								Byte3							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MODE			LUT SEL	LUT Address			RF Load	TRX	Chip Address							LUT Address							
1	0	1	HVn	LA9	LA8	LA7	LATCH	TRn	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	LA6	LA5	LA4	LA3	LA2	LA1	LA0	RES

Figure 55. LCL_FST_BM_STR Command Bit Sequence

Table 17. LCL_FST_BM_STR Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Fast Beam Steering, mode = 101.
1	4	HVn	0 = Loads V-pol channels from VLUT. 1 = Loads H-pol channels from HLUT.
1	3:1	LUT Address	The 3 MSBs of the LUT address, 9:7.
1	0	Latch	0 = Loads the LUT data only to the buffers. 1 = Loads the LUT data to both the buffers and the SET registers.
2	7	TRn	0 = Loads LUT data to RX channels. Also enables the RX channel. 1 = Loads LUT data to TX channels. Also enables the TX channel.
2	6:0	Chip Address	
3	7:1	LUT Address	The 7 LSBs of the LUT address, 6:0.

7.1.8. GBL_FST_BM_STR

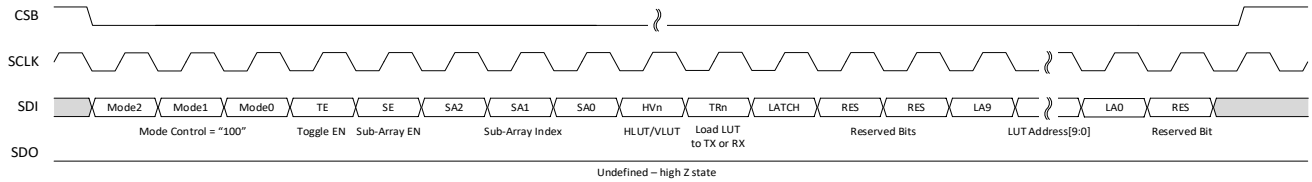


Figure 56. GBL_FST_BM_STR Timing Sequence

Byte1								Byte2								Byte3							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MODE			Toggle	SA Enable	Sub-Array Idx			LUT SEL	TRX	RF Load	RES		LUT Address											
1	0	0	TE	SE	SA2	LATCH	SA0	HVn	TRn	LATCH	RES	RES	LA9	LA8	LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	RES

Figure 57. GBL_FST_BM_STR Command Bit Sequence

Table 18. GBL_FST_BM_STR Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Global Fast Beam Steering, mode = 100.
1	4	Toggle Enable (TE)	0 = No LUT increment. 1 = After byte 3, every SCLK pulse increments the LUT address and loads the contents to the registers.
1	3	Sub-Array Enable (SE)	0 = Command executed on all chips. 1 = Commands executed on chips with matching sub-array.
1	2:0	Sub-Array Index	If SE is set, data is written only when this index matches with the chip's sub-array index (stored in register 0x0).
2	7	HVn	0 = Loads V-pol channels from VLUT. 1 = Loads H-pol channels from HLUT.
2	6	TRn	0 = Loads LUT data to RX channels. Also enables the RX channel. 1 = Loads LUT data to TX channels. Also enables the TX channel.
2	5	Latch	0 = Loads the LUT data only to the buffers. 1 = Loads the LUT data to both the buffers and the SET registers.
2	2:0	LUT Address	The 3 MSBs of the LUT address bits 9:7.
3	7:1	LUT Address	The 7 LSBs of the LUT address, 6:0.

Timing requirements for general Read/Write SPI operations are shown and described for a V_{DD} of +2.5V and 50°C ambient temperature.

Table 19. SPI Timing Typical Specifications

Symbol	Test Condition	Minimum	Typical	Maximum	Unit
t_S	CSB to SCLK setup time	2	-	-	ns
t_{DS}	SDI data setup time	2	-	-	ns
t_{DH}	SDI data hold time	4.2	-	-	ns
t_{CLK}	SCLK period	10.5	-	-	ns
t_{HI}	SCLK high time	5.25	-	-	ns
t_{DO}	SCLK falling edge to valid SDO (first valid output bit in a READ operation)	5.1	-	-	ns
t_H	SCLK to CSB hold time	7	-	-	ns
t_{CSB_HI}	CSB high time	7	-	-	ns

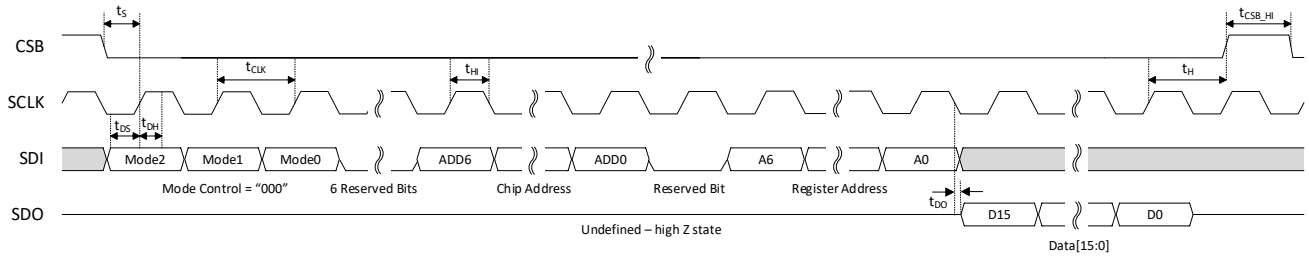


Figure 58. Timing Specification Diagram

8. Register Information

Default register values stated below are the recommended values for typical operation. It should be noted that these values need to be programmed by SPI register write after power-on-reset as some registers would power up with different values.

8.1 Control Configuration Register (CTRL_CFG)

Offset Address: 00h Default Value: 0000h

Bit	Field	Type	Description
15	IO_TEST	WO	IO test mode for IO's VIL/VIH and MISO's VOL/VOH tests, only reset by power-on reset. In IO test mode, MISO pin is the output pin and its logic is RESET OR SPI_CSB OR SPI_CLK OR SPI_MOSI OR ADD0 OR ADD1 OR ADD2 OR ADD3 OR STROBE_IN.
14	RSV	WO	Reserved.
13	SCAN_MODE	WO	Enable scan mode.
12	RESET	WO	1 = Reset the chip – auto self-reset to 0.
11	SHIFTREG_ADDR_EN	RO	1 = Shift register address is programmed and effective.
10	SHIFTREG_ADDR_PROG	WO	8-bit shift register is placed between ADD0 pin (in) and ADD1 pin (out). To program the address, set this bit, then, without releasing CSB, send in 8-bit data to ADD0 pin starting with LSB. Existing data is pushed out of ADD1 pin. New chip address = shift_reg[7:0].
9:7	SA_IDX	RW	Sub-array index.
6:4	STROBE_PROG	RW	Program the strobe pin functionality. 000 = Latch buffers. 001 = V TRX toggle. 010 = H TRX toggle. 011 = H and V TRX toggle. 100 = V LUT increment (enabled RX/TX). 101 = H LUT increment (enabled RX/TX). 110 = H and V LUT increment (enabled RX/TX).
3	H_TRn	RW	This bit is identical to HLUT[14]. Changing one will change the other. 0 = RXH enabled. 1 = TXH enabled.
2	V_TRn	RW	This bit is identical to VLUT[14]. Changing one will change the other. 0 = RXV enabled. 1 = TXV enabled.
1	H_EN	RW	Enable H channels.
0	V_EN	RW	Enable V channels.

8.2 Vertical-Polarization LUT Address Pointer Register (VLUT)

Offset Address: 01h Default Value: 000Fh

Bit	Field	Type	Description
15	RSV	RO	Reserved.
14	TRn	RW	This bit is identical to CTRL_CFG[2]. Changing one will change the other. 0 = RXV enabled. 1 = TXV enabled.
13:4	VLUT_PTR	RW	Updated when Global or Local FBS command is issued. When written to, channel SET register buffers are loaded with LUT data.
3	V4_EN	RW	Enable channel V4 when V_EN (CTRL_CFG[0]) = 1.
2	V3_EN	RW	Enable channel V3 when V_EN (CTRL_CFG[0]) = 1.
1	V2_EN	RW	Enable channel V2 when V_EN (CTRL_CFG[0]) = 1.
0	V1_EN	RW	Enable channel V1 when V_EN (CTRL_CFG[0]) = 1.

8.3 Horizontal-Polarization LUT Address Pointer Register (HLUT)

Offset Address: 02h Default Value: 000Fh

Bit	Field	Type	Description
15	RSV	RO	Reserved.
14	TRn	RW	This bit is identical to CTRL_CFG[3]. Changing one will change the other. 0 = RXH enabled. 1 = TXH enabled.
13:4	HLUT_PTR	RW	Updated when Global or Local FBS command is issued. When written to, channel SET register buffers are loaded with LUT data.
3	H4_EN	RW	Enable channel H4 when H_EN (CTRL_CFG[1]) = 1.
2	H3_EN	RW	Enable channel H3 when H_EN (CTRL_CFG[1]) = 1.
1	H2_EN	RW	Enable channel H2 when H_EN (CTRL_CFG[1]) = 1.
0	H1_EN	RW	Enable channel H1 when H_EN (CTRL_CFG[1]) = 1.

8.4 Master Bias Control Register 1 (MBIAS)

Offset Address: 05h Default Value: 809Bh

Bit	Field	Type	Description
15:12	SCTAT_CTRL	RW	Super CTAT Bias control.
11:9	SCTAT_TRIM	RW	Super CTAT Bias trim.
8	SCTAT_EN	RW	Super CTAT Bias enable.
7:5	PTAT2_SLOPE	RW	$PTAT^2$ slope control.
4:2	PTADJ	RW	Internal reference current generator level control. ±30% reference current adjustment.

Bit	Field	Type	Description
1	VBG_SEL	RW	Select band-gap generator. 0 = BG generated from PTAT source. 1 = Brokaw BG generator.
0	MBIAS_EN	RW	Master Bias enable.

8.5 PDET Enable Register (SENS_EN)

Offset Address: 06h Default Value: 0000h

Bit	Field	Type	Description
15:13	RSV	RW	Reserved.
12:9	TSENS_SEL	RW	<1XXX> = TSENS_CORE enable. <0111-0100> = H4-H1. <0011-0000> = V4-V1.
8	TSENS_EN	RW	TSENSE Engine enable.
7	HTX4_PDET_EN	RW	PDET H4 enable.
6	HTX3_PDET_EN	RW	PDET H3 enable.
5	HTX2_PDET_EN	RW	PDET H2 enable.
4	HTX1_PDET_EN	RW	PDET H1 enable.
3	VTX4_PDET_EN	RW	PDET V4 enable.
2	VTX3_PDET_EN	RW	PDET V3 enable.
1	VTX2_PDET_EN	RW	PDET V2 enable.
0	VTX1_PDET_EN	RW	PDET V1 enable.

8.6 Master Bias Control Register 2 (SENS_CTRL)

Offset Address: 07h Default Value: 0630h

Bit	Field	Type	Description
15:12	RSV	RW	Reserved.
11:10	PD_BIAS_BUF_PROF	RW	PDET Buffer Bias profile.
9:7	PD_BIAS_BUF_CTRL	RW	PDET Buffer Bias control.
6:5	PD_BIAS_PROF	RW	PDET Bias profile.
4:2	PD_BIAS_CTRL	RW	PDET Bias control.
1	PD_BIAS_EN	RW	PDET Bias enable.
0	TSENS_CHOPPER_EN	RW	TSENS Chopper enable.

8.7 Chip ID Register (CHIP_ID)

Offset Address: 08h Default Value: 0409h

Bit	Field	Type	Description
15:14	ID_CLASS	RO	0 = Beamformer.
13:12	ID_FREQ	RO	0 = 26GH. 1 = 28GHz. 2 = 39GHz.
11:8	BASE_REV	RO	Base layer revision. 1 = V1XY. 2 = V2XY. 3 = V3XY.
7:4	METAL_REV	RO	Metal layer revision. X in V1XY.
3:0	VARIANTS	RO	Variant number. Y in V1XY.

8.8 SRAM BIST Register (BIST)

Offset Address: 09h Default Value: 0000h

Bit	Field	Type	Description
15:8	RSV	RO	Reserved.
7	SRAM_DONE	RO	SRAM access (initialization, BIST, or CRC) status. 0 = SRAM access is requested. 1 = SRAM access is done.
6:4	SRAM_ERR	RO	Number of SRAM error times during SRAM BIST. When the number exceeds 7, it will be kept at 7.
3	SRAM_SEL	RW	0 = V-polarization SRAM. 1 = H-polarization SRAM.
2	SRAM_CRC	RW	SRAM CRC check request. Request SRAM CRC by writing ‘1’. The SRAM CRC algorithm is as follows: 1. Initial value is 0xFFFF. 2. CRC generator is $x^{16} + x^{12} + x^5 + 1$. 3. The sequence is: • N = 0 • Get data from LUT[N] • Do CRC on channel 1 data (bit11, bit 10, …, bit1, bit0) • Do CRC on channel 2, 3, and 4 • If N =1023, finish CRC check; else do N = N + 1 and go to step b.
1	SRAM_BIST	RW	SRAM BIST request. Request SRAM BIST by writing ‘1’.
0	SRAM_INIT	RW	SRAM initialization request (initialize all SRAM data to ‘0’). Request SRAM initialization by writing ‘1’.

8.9 SRAM CRC Result Register (CRC_RESULT)

Offset Address: 0Ah Default Value: 0000h

Bit	Field	Type	Description
15:0	CRC_RESULT	RO	16-bit SRAM CRC result.

8.10 ADC Channel Select Register 1 (ADC_SEL1)

Offset Address: 0Bh Default Value: 0000h

Bit	Field	Type	Description
15	EXT7	RW	Output data saved in register address 0x7F.
14	EXT6	RW	Vbg_ptat.
13	EXT5	RW	Vbg_por.
12	EXT4	RW	DVDD/2
11	EXT3	RW	VDD/2
10	EXT2	RW	IDC_TEST set by ADC_CTRL: 50μA sent to AOUT pin.
9	EXT1	RW	IDC_TEST set by ADC_CTRL: 50μA drawn on the internal 10kΩ resistor. Expected voltage = 0.5V.
8	TSENSE_H4	RW	Output data saved in register address 0x78.
7	TSENSE_H3	RW	Output data saved in register address 0x77.
6	TSENSE_H2	RW	Output data saved in register address 0x76.
5	TSENSE_H1	RW	Output data saved in register address 0x75.
4	TSENSE_V4	RW	Output data saved in register address 0x74.
3	TSENSE_V3	RW	Output data saved in register address 0x73.
2	TSENSE_V2	RW	Output data saved in register address 0x72.
1	TSENSE_V1	RW	Output data saved in register address 0x71.
0	TSENSE_CORE	RW	Output data saved in register address 0x70.

8.11 ADC Channel Select Register 2 (ADC_SEL2)

Offset Address: 0Ch Default Value: 0000h

Bit	Field	Type	Description
15	PDREF_H4	RW	Output data saved in register address 0x6F.
14	PDREF_H3	RW	Output data saved in register address 0x6E.
13	PDREF_H2	RW	Output data saved in register address 0x6D.
12	PDREF_H1	RW	Output data saved in register address 0x6C.
11	PDREF_V4	RW	Output data saved in register address 0x6B.
10	PDREF_V3	RW	Output data saved in register address 0x6A.
9	PDREF_V2	RW	Output data saved in register address 0x69.
8	PDREF_V1	RW	Output data saved in register address 0x68.

Bit	Field	Type	Description
7	PD_H4	RW	Output data saved in register address 0x67.
6	PD_H3	RW	Output data saved in register address 0x66.
5	PD_H2	RW	Output data saved in register address 0x65.
4	PD_H1	RW	Output data saved in register address 0x64.
3	PD_V4	RW	Output data saved in register address 0x63.
2	PD_V3	RW	Output data saved in register address 0x62.
1	PD_V2	RW	Output data saved in register address 0x61.
0	PD_V1	RW	Output data saved in register address 0x60.

8.12 ADC Control Register (ADC_CTRL)

Offset Address: 0Dh Default Value: 0000h

Bit	Field	Type	Description
15:14	RSV	RW	Reserved.
13:11	IDC_TEST	RW	Tested on EXT1. 000 = Disabled. 001 = Ibg_50μA. 010 = Ipt_50μA. 011 = Ipt2_50μA. 100 = Isct_50μA.
10	PD_DIFF_MODE	RW	0 = Software diff (PD_V1 = PD-PDREF). 1 = No diff.
9:8	OSC_FREQ	RW	Oscillator frequency. 0 = 80MHz. 1 = 40MHz. 2 = 20MHz. 3 = OFF.
7	OSC_EN	RW	Oscillator enable.
6:5	AOUT_SEL	RW	AOUT mux selection. 0 = ADC input specified by registers ADC_SEL1 and ADC_SEL2. 1 = cbn1_test. 2 = vref(v1p5). 3 = vcm(v0p9).
4	AOUT_EN	RW	AOUT mux enable.
3	LSB_SEL	RW	Turn down LSB. 0 = LSB is Vref/1023. 1 = LSB is Vref/1055.
2	CHOPPER_EN	RW	Chopper enable.
1	ADC_I_2X	RW	Double ADC bias current.
0	ADC_START	RW	Start ADC operation.

8.13 ADC Clock Control Register (ADC_CLK)

Offset Address: 0Eh Default Value: 6B30h

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14:12	ADC_AVG	RW	0 = No averaging. 1-6 = Averaging count = 2^{ADC_AVG}. 7: Averaging count = 2^6.
11:8	BASE_CLK_CTRL	RW	Select base clock (BASE_CLK) as OSC_60MHz/(N+1).
7:4	ADC_CLK_HIGH	RW	Select ADC clock's high width as BASE_CLK*(N+1).
3:0	ADC_CLK_LOW	RW	Select ADC clock's low width as BASE_CLK*(N+1).

8.14 OTP Control Register (OTP_CTRL)

Offset Address: 0Fh Default Value: 0000h

Bit	Field	Type	Description
15:13	RSV	RO	Reserved.
12:10	OTP_WR_BIT	RW	Bit number to burn during program mode.
9:6	OTP_RW_ADDRESS	RW	OTP Read/Write address back selection.
5	OTP_PROG	RW	OTP program mode.
4	OTP_POR	RW	OTP POR.
3:2	OTP_CUR	RW	OTP current control.
1	OTP_READ	RW	OTP Read enable.
0	OTP_EN	RW	OTP enable.

8.15 PCM Control Register (PCM_CTRL)

Offset Address: 10h Default Value: 0000h

Bit	Field	Type	Description
15:7	RSV	RO	Reserved.
6:3	PCM_CLK_DIV	RW	Counter duration = Tspi_clk/(PCM_CLK_DIV+1).
2:1	PCM_CH_SEL	RW	PCM channel selection. 0 = BJT ring oscillator. 1 = R ring oscillator. 2 = RC ring oscillator.
0	PCM_START	RW	PCM start (auto-reset).

8.16 TOP Spare Register 1 (SPARE1)

Offset Address: 11h Default Value: 0000h

Bit	Field	Type	Description
15:0	RSV	RW	Reserved.

8.17 TOP Spare Register 2 (SPARE2)

Offset Address: 12h Default Value: 0000h

Bit	Field	Type	Description
15:0	RSV	RW	Reserved.

8.18 PCM Data Register 1 (DATA_PCM1)

Offset Address: 15h Default Value: 0000h

Bit	Field	Type	Description
15:12	RSV	RO	Reserved.
11:0	DATA_CH1	RO	CH1: BJT.

8.19 PCM Data Register 2 (DATA_PCM2)

Offset Address: 16h Default Value: 0000h

Bit	Field	Type	Description
15:12	RSV	RO	Reserved.
11:0	DATA_CH2	RO	CH2: R.

8.20 PCM Data Register 3 (DATA_PCM3)

Offset Address: 17h Default Value: 0000h

Bit	Field	Type	Description
15:12	RSV	RO	Reserved.
11:0	DATA_CH3	RO	CH3: RC.

8.21 OTP Data Register 1 (DATA_OTP1)

Offset Address: 18h Default Value: 0000h

Bit	Field	Type	Description
15:8	DATA_OTP_REG1	RO	OTP address = 4’d1.
7:0	DATA_OTP_REG0	RO	OTP address = 4’d0.

8.22 OTP Data Register 2 (DATA_OTP2)

Offset Address: 19h Default Value: 0000h

Bit	Field	Type	Description
15:8	DATA_OTP_REG3	RO	OTP address = 4’d3.
7:0	DATA_OTP_REG2	RO	OTP address = 4’d2.

8.23 OTP Data Register 3 (DATA_OTP3)

Offset Address: 1Ah Default Value: 0000h

Bit	Field	Type	Description
15:8	DATA_OTP_REG5	RO	OTP address = 4'd5.
7:0	DATA_OTP_REG4	RO	OTP address = 4'd4.

8.24 OTP Data Register 4 (DATA_OTP4)

Offset Address: 1Bh Default Value: 0000h

Bit	Field	Type	Description
15:8	DATA_OTP_REG7	RO	OTP address = 4'd7.
7:0	DATA_OTP_REG6	RO	OTP address = 4'd6.

8.25 OTP Data Register 5 (DATA_OTP5)

Offset Address: 1Ch Default Value: 0000h

Bit	Field	Type	Description
15:8	DATA_OTP_REG9	RO	OTP address = 4'd9.
7:0	DATA_OTP_REG8	RO	OTP address = 4'd8.

8.26 OTP Data Register 6 (DATA_OTP6)

Offset Address: 1Dh Default Value: 0000h

Bit	Field	Type	Description
15:8	DATA_OTP_REG11	RO	OTP address = 4'd11.
7:0	DATA_OTP_REG10	RO	OTP address = 4'd10.

8.27 OTP Data Register 7 (DATA_OTP7)

Offset Address: 1Eh Default Value: 0000h

Bit	Field	Type	Description
15:8	DATA_OTP_REG13	RO	OTP address = 4'd13.
7:0	DATA_OTP_REG12	RO	OTP address = 4'd12.

8.28 OTP Data Register 8 (DATA_OTP8)

Offset Address: 1Fh Default Value: 0000h

Bit	Field	Type	Description
15:8	DATA_OTP_REG15	RO	OTP address = 4'd15.
7:0	DATA_OTP_REG14	RO	OTP address = 4'd14.

8.29 Vertical TRX Block Enable Register (ENV)

Offset Address: 20h Default Value: 1F0Fh

Bit	Field	Type	Description
15:13	RSV	RW	Reserved.
12	TX_PA_EN	RW	TX PA enable.
11	TX_DA_EN	RW	TX DA enable.
10	TX_PS_EN	RW	TX phase shifter enable.
9	TX_VGA2_EN	RW	TX VGA2 enable.
8	TX_VGA1_EN	RW	TX VGA1 enable.
7:4	RSV	RW	Reserved.
3	RX_LNA1_EN	RW	RX LNA1 enable.
2	RX_LNA2_EN	RW	RX LNA2 enable.
1	RX_PS_EN	RW	RX phase shifter enable.
0	RX_VGA_EN	RW	RX VGA enable.

8.30 Vertical LNA Control Register (RXV_LNA)

Offset Address: 21h Default Value: 0BA8h

<table>
<tr><th>Bit</th><th>Field</th><th>Type</th><th>Description</th></tr>
<tr><td>15:12</td><td>RSV</td><td>RW</td><td>Reserved.</td></tr>
<tr><td>11</td><td>RX_LNA2_PT</td><td>RW</td><td>0 = PTAT current source.
1 = PTAT^2 current source.</td></tr>
<tr><td>10:8</td><td>RX_LNA2_BIAS</td><td>RW</td><td>Set LNA2 bias.</td></tr>
<tr><td>7</td><td>RX_LNA1_PT</td><td>RW</td><td>0 = PTAT current source.
1 = PTAT^2 current source.</td></tr>
<tr><td>6:3</td><td>RX_LNA1_BIAS</td><td>RW</td><td>Set LNA1 bias.</td></tr>
<tr><td>2:1</td><td>RX_LinMode</td><td>RW</td><td>0 = Max gain.
1 = LNA1 gain reduced by 3dB.
2 = LNA2 gain reduced by 3dB.
3 = Both LNA1 and LNA2 gain reduced (6dB total)
<table>
<tr><th>Setting</th><th>LNA1 Attenuation</th><th>LNA2 Attenuation</th></tr>
<tr><td>0</td><td>0dB</td><td>0dB</td></tr>
<tr><td>1</td><td>3dB</td><td>0dB</td></tr>
<tr><td>2</td><td>0dB</td><td>3dB</td></tr>
<tr><td>3</td><td>3dB</td><td>3dB</td></tr>
</table></td></tr>
<tr><td>0</td><td>RX_LinMode_ExtPinEN</td><td>RW</td><td>0 = LNA linearity mode as defined by RX_LinMode.
1 = LNA linearity mode gated by LNASW pin.
<table>
<tr><th>RX_LinMode_ExtPinEN</th><th>LNASW Pin</th><th>Linearity Mode</th></tr>
<tr><td>0</td><td>0</td><td>1 (RX_LinMode)</td></tr>
<tr><td>0</td><td>1</td><td>1 (RX_LinMode)</td></tr>
<tr><td>1</td><td>0</td><td>1 (RX_LinMode)</td></tr>
<tr><td>1</td><td>1</td><td>0 (Max gain)</td></tr>
</table></td></tr>
</table>

8.31 Vertical RX PS/VGA Control Register (RXV_PS_VGA)

Offset Address: 22h Default Value: 020Ch

Bit	Field	Type	Description
15:11	RSV	RW	Reserved.
10	RX_VGA_PT	RW	0 = PTAT current source. 1 = $PTAT^2$ current source.
9:7	RX_VGA_BIAS	RW	Set VGA bias.
6:4	RX_PS_CORR	RW	Phase shifter correction.
3	RX_PS_PT	RW	0 = PTAT current source. 1 = $PTAT^2$ current source.
2:0	RX_PS_BIAS	RW	Set phase shifter bias.

8.32 Vertical RX Spare Register 1 (RXV_SPARE1)

Offset Address: 23h Default Value: 0000h

Bit	Field	Type	Description
15:0	RSV	RW	Reserved.

8.33 Vertical RX Spare Register 2 (RXV_SPARE2)

Offset Address: 24h Default Value: 0000h

Bit	Field	Type	Description
15:0	RSV	RW	Reserved.

8.34 Vertical TX PA Control Register (TXV_PA)

Offset Address: 25h Default Value: 1CB7h

Bit	Field	Type	Description
15:13	RSV	RW	Reserved.
12	TX_PA_FB	RW	PA RC feedback control.
11:10	TX_PA_BIASR	RW	PA bias resistor tuning.
9:8	TX_PA_CASCCAP	RW	PA cascade capacitor tuning.
7	TX_PA_BG	RW	0 = PTAT current source. 1 = Band-gap current source.
6:4	TX_PA_CASCBIAS	RW	PA cascade bias.
3:0	TX_PA_BIAS	RW	PA core bias.

8.35 Vertical TX Driver Control Register (TXV_DRV)

Offset Address: 26h Default Value: 01E6h

Bit	Field	Type	Description
15:13	RSV	RW	Reserved.
12	TX_DA_INPUTRTUNE	RW	Driver input resistor tuning.
11:10	TX_DA_INTERCTUNE	RW	Driver inter-stage capacitor tuning.
9:8	TX_DA_INPUTCTUNE	RW	Driver input capacitor tuning.
7	TX_DA_PT	RW	0 = PTAT current source. 1 = $PTAT^2$ current source.
6:4	TX_DA_CASCBIAS	RW	Driver cascade bias.
3:0	TX_DA_BIAS	RW	Driver core bias.

8.36 Vertical TX PS/VGA Control Register (TXV_PS_VGA)

Offset Address: 27h Default Value: 0C5Ch

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14:12	TX_PS_CORR	RW	Phase shifter correction.
11	TX_PS_PT	RW	0 = PTAT current source. 1 = $PTAT^2$ current source.
10:8	TX_PS_BIAS	RW	Set phase shifter bias.
7	TX_VGA2_PT	RW	0 = PTAT current source. 1 = $PTAT^2$ current source.
6:4	TX_VGA2_BIAS	RW	Set VGA2 bias.
3	TX_VGA1_PT	RW	0 = PTAT current source. 1 = $PTAT^2$ current source.
2:0	TX_VGA1_BIAS	RW	Set VGA1 bias.

8.37 Vertical TX Spare Register 1 (TXV_SPARE1)

Offset Address: 28h Default Value: 0000h

Bit	Field	Type	Description
15:0	RSV	RW	Reserved.

8.38 Vertical TX Spare Register 2 (TXV_SPARE2)

Offset Address: 29h Default Value: 0000h

Bit	Field	Type	Description
15:0	RSV	RW	Reserved.

8.39 Vertical PDET Control Register (PDETV)

Offset Address: 2Ah Default Value: 0053h

Bit	Field	Type	Description
15:8	RSV	RW	Reserved.
7:5	PDET_ATEST	RW	PDET Atest control.
4:3	PDET_Range	RW	Power range.
2	PDET_AMPEN	RW	PDET differential amplifier enable.
1:0	SW_BIAS	RW	RX antenna switch bias.

8.40 Horizontal TRX Block Enable Register (ENH)

Offset Address: 30h Default Value: 1F0Fh

Bit	Field	Type	Description
15:13	RSV	RW	Reserved.
12	TX_PA_EN	RW	TX PA enable.
11	TX_DA_EN	RW	TX DA enable.
10	TX_PS_EN	RW	TX phase shifter enable.
9	TX_VGA2_EN	RW	TX VGA2 enable.
8	TX_VGA1_EN	RW	TX VGA1 enable.
7:4	RSV	RW	Reserved.
3	RX_LNA1_EN	RW	RX LNA1 enable.
2	RX_LNA2_EN	RW	RX LNA2 enable.
1	RX_PS_EN	RW	RX phase shifter enable.
0	RX_VGA_EN	RW	RX VGA enable.

8.41 Horizontal LNA Control Register (RXH_LNA)

Offset Address: 31h Default Value: 0BA8h

Bit	Field	Type	Description
15:12	RSV	RW	Reserved.
11	RX_LNA2_PT	RW	0 = PTAT current source. 1 = $PTAT^2$ current source.
10:8	RX_LNA2_BIAS	RW	Set LNA2 bias.
7	RX_LNA1_PT	RW	0 = PTAT current source. 1 = $PTAT^2$ current source.
6:3	RX_LNA1_BIAS	RW	Set LNA1 bias.

<table>
<tr><th>Bit</th><th>Field</th><th>Type</th><th>Description</th></tr>
<tr><td>2:1</td><td>RX_LinMode</td><td>RW</td><td>0 = Max gain.
1 = LNA1 gain reduced by 3dB.
2 = LNA2 gain reduced by 3dB.
3 = Both LNA1 and LNA2 gain reduced (6dB total)
<table>
<tr><th>Setting</th><th>LNA1 Attenuation</th><th>LNA2 Attenuation</th></tr>
<tr><td>0</td><td>0dB</td><td>0dB</td></tr>
<tr><td>1</td><td>3dB</td><td>0dB</td></tr>
<tr><td>2</td><td>0dB</td><td>3dB</td></tr>
<tr><td>3</td><td>3dB</td><td>3dB</td></tr>
</table></td></tr>
<tr><td>0</td><td>RX_LinMode_ExtPinEN</td><td>RW</td><td>0 = LNA linearity mode as defined by RX_LinMode.
1 = LNA linearity mode gated by LNASW pin.
<table>
<tr><th>RX_LinMode_ExtPinEN</th><th>LNASW Pin</th><th>Linearity Mode</th></tr>
<tr><td>0</td><td>0</td><td>1 (RX_LinMode)</td></tr>
<tr><td>0</td><td>1</td><td>1 (RX_LinMode)</td></tr>
<tr><td>1</td><td>0</td><td>1 (RX_LinMode)</td></tr>
<tr><td>1</td><td>1</td><td>0 (Max gain)</td></tr>
</table></td></tr>
</table>

8.42 Horizontal RX PS/VGA Control Register (RXH_PS_VGA)

Offset Address: 32h Default Value: 020Ch

Bit	Field	Type	Description
15:11	RSV	RW	Reserved.
10	RX_VGA_PT	RW	0 = PTAT current source. 1 = $PTAT^2$ current source.
9:7	RX_VGA_BIAS	RW	Set VGA bias.
6:4	RX_PS_CORR	RW	Phase shifter correction.
3	RX_PS_PT	RW	0 = PTAT current source. 1 = $PTAT^2$ current source.
2:0	RX_PS_BIAS	RW	Set phase shifter bias.

8.43 Horizontal RX Spare Register 1 (RXH_SPARE1)

Offset Address: 33h Default Value: 0000h

Bit	Field	Type	Description
15:0	RSV	RW	Reserved.

8.44 Horizontal RX Spare Register 2 (RXH_SPARE2)

Offset Address: 34h Default Value: 0000h

Bit	Field	Type	Description
15:0	RSV	RW	Reserved.

8.45 Horizontal TX PA Control Register (TXH_PA)

Offset Address: 35h Default Value: 1CB7h

Bit	Field	Type	Description
15:13	RSV	RW	Reserved.
12	TX_PA_FB	RW	PA RC feedback control.
11:10	TX_PA_BIASR	RW	PA bias resistor tuning.
9:8	TX_PA_CASCCAP	RW	PA cascade capacitor tuning.
7	TX_PA_BG	RW	0 = PTAT current source. 1 = Band-gap current source.
6:4	TX_PA_CASCBIAS	RW	PA cascade bias.
3:0	TX_PA_BIAS	RW	PA core bias.

8.46 Horizontal TX Driver Control Register (TXH_DRV)

Offset Address: 36h Default Value: 01E6h

Bit	Field	Type	Description
15:13	RSV	RW	Reserved.
12	TX_DA_INPUTRTUNE	RW	Driver input resistor tuning.
11:10	TX_DA_INTERCTUNE	RW	Driver inter-stage capacitor tuning.
9:8	TX_DA_INPUTCTUNE	RW	Driver input capacitor tuning.
7	TX_DA_PT	RW	0 = PTAT current source. 1 = $PTAT^2$ current source.
6:4	TX_DA_CASCBIAS	RW	Driver cascade bias.
3:0	TX_DA_BIAS	RW	Driver core bias.

8.47 Horizontal TX PS/VGA Control Register (TXH_PS_VGA)

Offset Address: 37h Default Value: 0C5Ch

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14:12	TX_PS_CORR	RW	Phase shifter correction.
11	TX_PS_PT	RW	0 = PTAT current source. 1 = $PTAT^2$ current source.
10:8	TX_PS_BIAS	RW	Set phase shifter bias.
7	TX_VGA2_PT	RW	0 = PTAT current source. 1 = $PTAT^2$ current source.
6:4	TX_VGA2_BIAS	RW	Set VGA2 bias.
3	TX_VGA1_PT	RW	0 = PTAT current source. 1 = $PTAT^2$ current source.
2:0	TX_VGA1_BIAS	RW	Set VGA1 bias.

8.48 Horizontal TX Spare Register 1 (TXH_SPARE1)

Offset Address: 38h Default Value: 0000h

Bit	Field	Type	Description
15:0	RSV	RW	Reserved.

8.49 Horizontal TX Spare Register 2 (TXH_SPARE2)

Offset Address: 39h Default Value: 0000h

Bit	Field	Type	Description
15:0	RSV	RW	Reserved.

8.50 Horizontal PDET Control Register (PDETH)

Offset Address: 3Ah Default Value: 0053h

Bit	Field	Type	Description
15:8	RSV	RW	Reserved.
7:5	PDET_ATEST	RW	PDET Atest control.
4:3	PDET_Range	RW	Power range.
2	PDET_AMPEN	RW	PDET differential amplifier enable.
1:0	SW_BIAS	RW	RX antenna switch bias.

8.51 Vertical RX SET Register (RXVn_SET) (n = 1 to 4)

Offset Address: 40h + 4*(n-1) Default Value: 40FFh

Bit	Field	Type	Description
15:8	RX_PHASE_CTRL	RW	RX phase control.
7:0	RX_GAIN_CTRL	RW	RX gain control.

8.52 Vertical TX SET Register (TXVn_SET) (n = 1 to 4)

Offset Address: 41h + 4*(n-1) Default Value: 00FFh

Bit	Field	Type	Description
15:8	TX_PHASE_CTRL	RW	TX phase control.
7:0	TX_GAIN_CTRL	RW	TX gain control.

8.53 Vertical RX Bias Register (RXVn_BIAS) (n = 1 to 4)

Offset Address: 42h + 4*(n-1) Default Value: 0002h

Bit	Field	Type	Description
15:4	SPARE	RW	SPARE.
3	RX_GAIN_MODE	RW	RX gain mode.
2:0	RX_CH_BIAS	RW	RX channel bias.

8.54 Vertical TX Bias Register (TXVn_BIAS) (n = 1 to 4)

Offset Address: 43h + 4*(n-1) Default Value: 0004h

Bit	Field	Type	Description
15:4	RSV	RW	Reserved.
3	TX_GAIN_MODE	RW	TX gain mode.
2:0	TX_CH_BIAS	RW	TX channel bias.

8.55 Horizontal RX SET Register (RXHn_SET) (n = 1 to 4)

Offset Address: 50h + 4*(n-1) Default Value: 40FFh

Bit	Field	Type	Description
15:8	RX_PHASE_CTRL	RW	RX phase control.
7:0	RX_GAIN_CTRL	RW	RX gain control.

8.56 Horizontal TX SET Register (TXHn_SET) (n = 1 to 4)

Offset Address: 51h + 4*(n-1) Default Value: 00FFh

Bit	Field	Type	Description
15:8	TX_PHASE_CTRL	RW	TX phase control.
7:0	TX_GAIN_CTRL	RW	TX gain control.

8.57 Horizontal RX Bias Register (RXHn_BIAS) (n = 1 to 4)

Offset Address: 52h + 4*(n-1) Default Value: 0002h

Bit	Field	Type	Description
15:4	SPARE	RW	SPARE.
3	RX_GAIN_MODE	RW	RX gain mode.
2:0	RX_CH_BIAS	RW	RX channel bias.

8.58 Horizontal TX Bias Register (TXHn_BIAS) (n = 1 to 4)

Offset Address: 53h + 4*(n-1) Default Value: 0004h

Bit	Field	Type	Description
15:4	RSV	RW	Reserved.
3	TX_GAIN_MODE	RW	TX gain mode.
2:0	TX_CH_BIAS	RW	TX channel bias.

8.59 ADC DATA Register (DATA_ADC_CHn) (n = 1 to 32)

Offset Address: 60h + (n-1) Default Value: 0000h

Bit	Field	Type	Description
15:11	RSV	RO	Reserved.
10	DONE	RO	ADC status.
9:0	VALUE	RO	ADC data.

9. Evaluation Board Picture

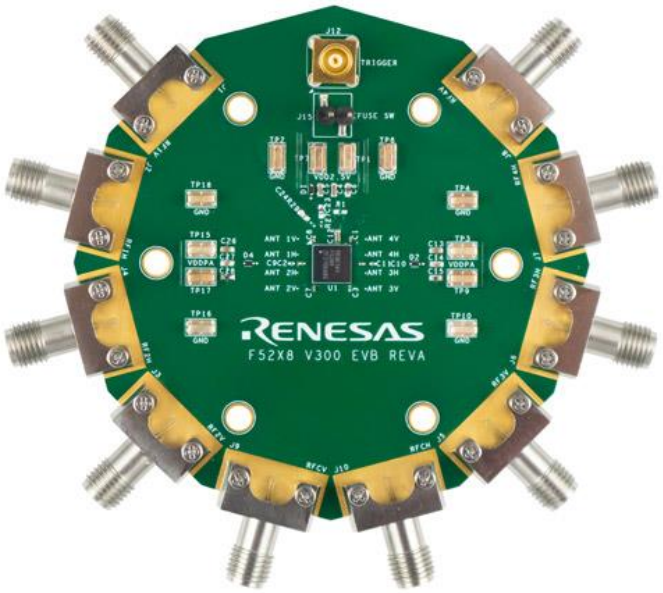


Figure 59. F5268/F5288 Evaluation Board (Top)

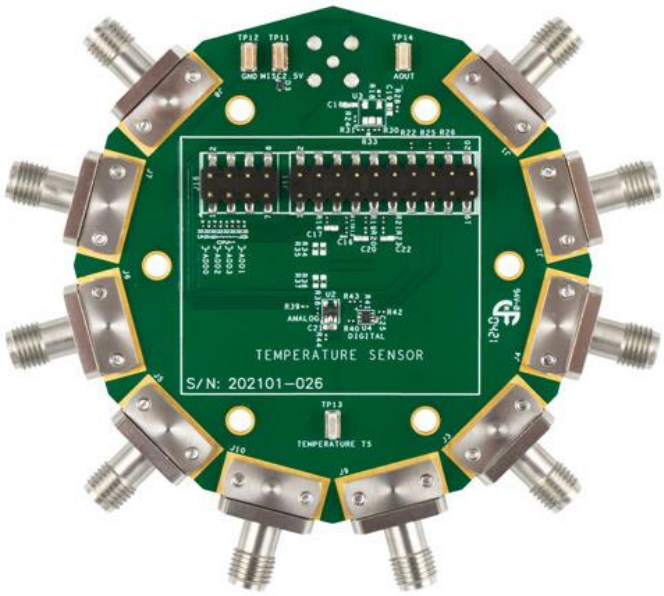


Figure 60. F5268/F5288 Evaluation Board (Bottom)

10. Evaluation Board / Application Circuits

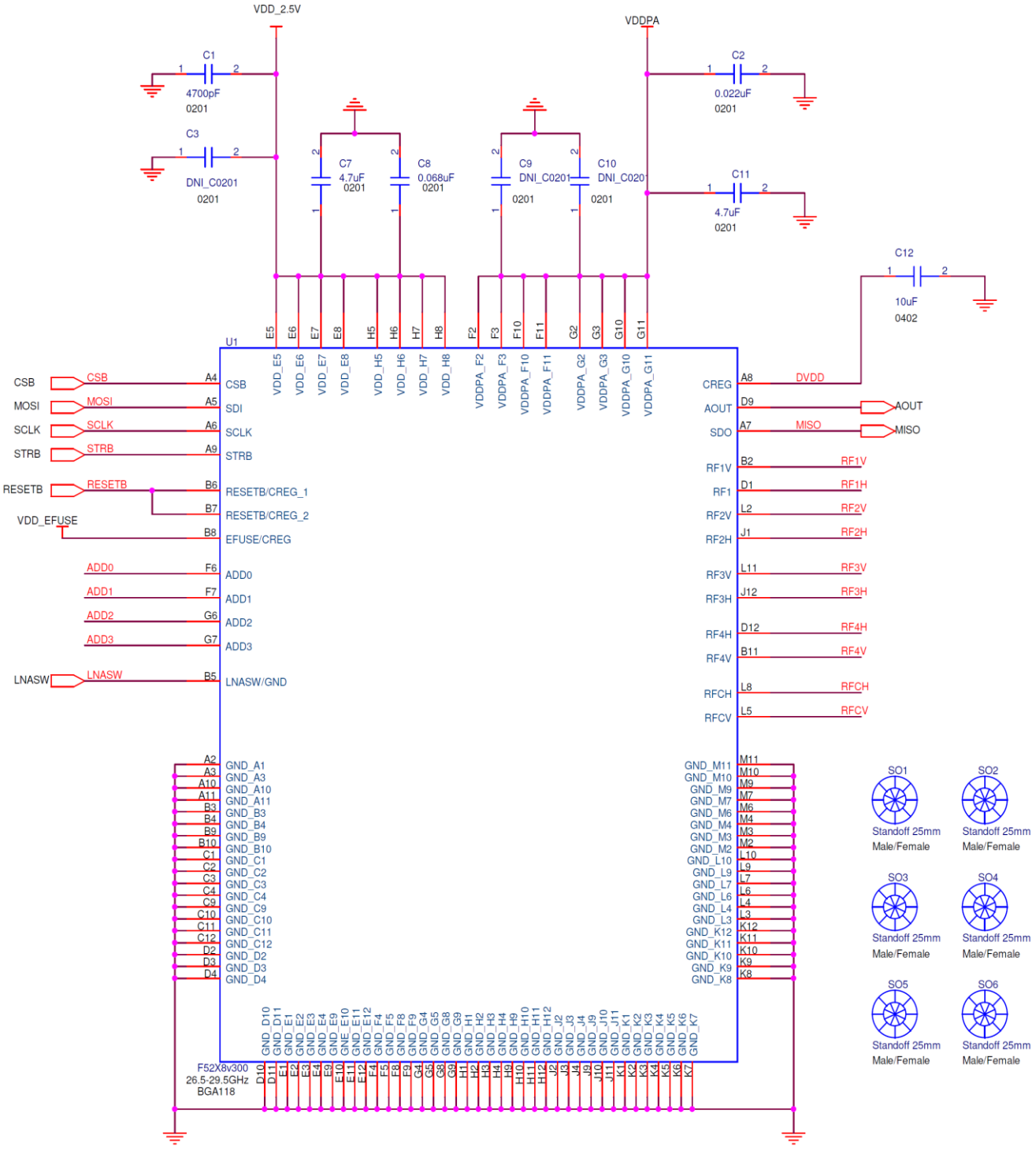


Figure 61. F5268/F5288 Evaluation Board Schematic (Part 1)

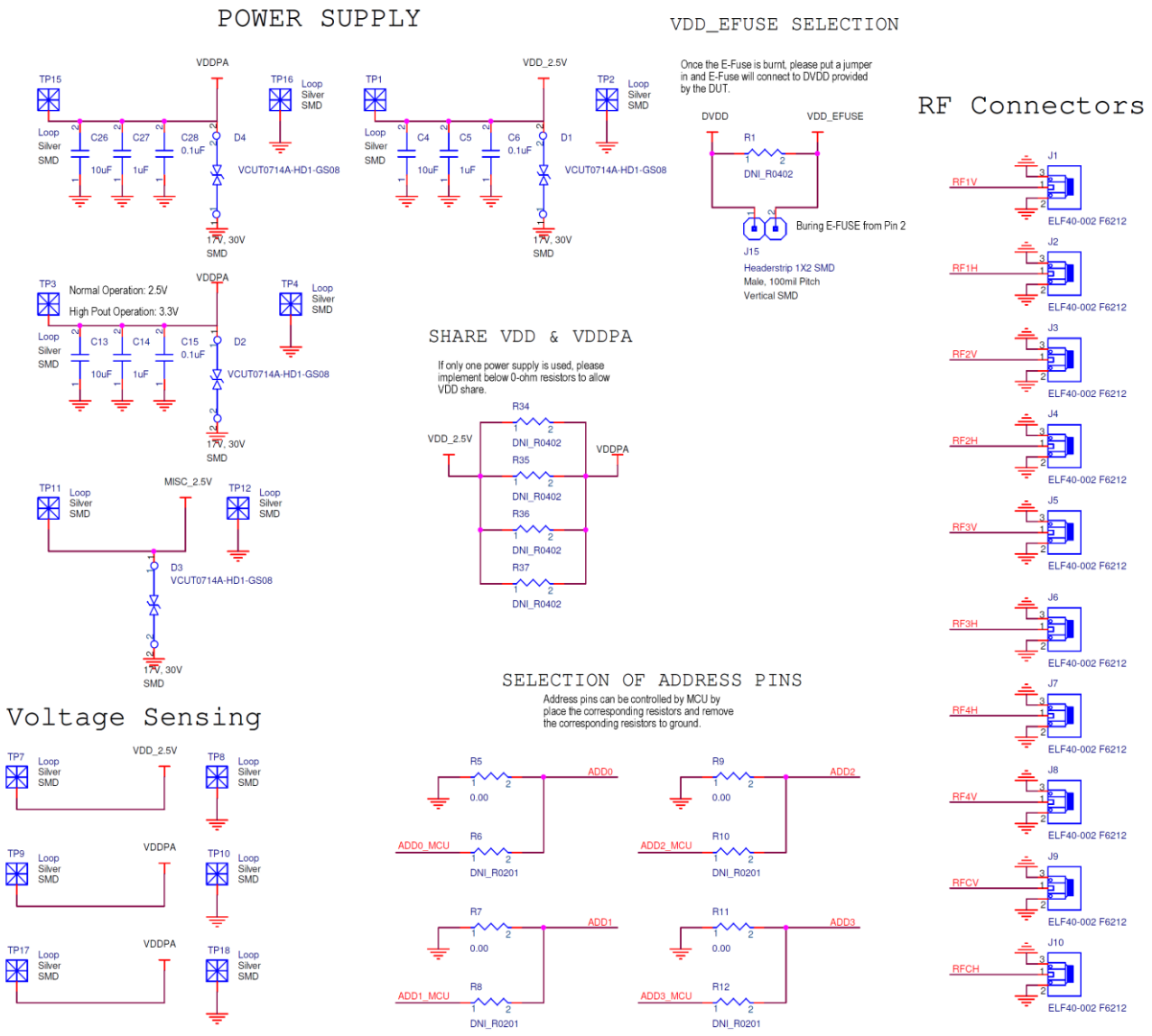


Figure 62. F5268/F5288 Evaluation Board Schematic (Part 2)

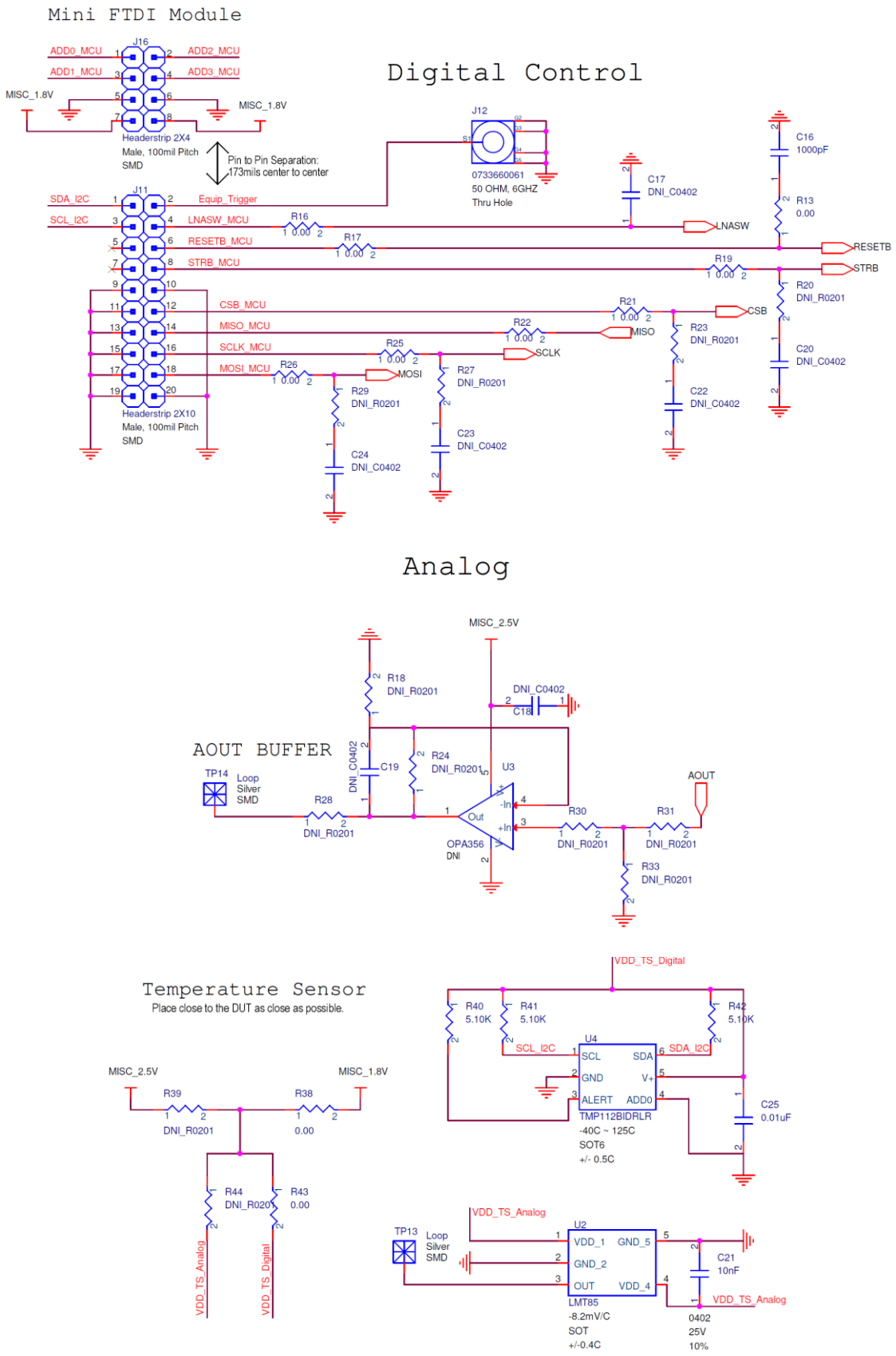


Figure 63. F5268/F5288 Evaluation Board Schematic (Part 3)

Table 20. Evaluation Board Bill of Material (BOM)

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C1	1	X7R Surface Mount Capacitor, 4700pF, 0201	GRM033R71E472K	Murata Electronics
C2	2	X6S Surface Mount Capacitor, 0.022µF, 0201	GRM033C80J223ME01D	Murata Electronics
C3, C9, C10	0	DNI	DNI	DNI
C4, C12, C13, C26	4	X5R Surface Mount Capacitor, 10µF, 0402	GRM155R60J106M	Murata Electronics
C5, C14, C27	3	X5R Surface Mount Capacitor, 1µF, 0402	CL05A105KA5NQNC	Samsung
C6, C15, C28	3	X5R Surface Mount Capacitor, 0.1µF, 0402	GRM155R61H104K	Murata Electronics
C7, C11	2	X5R Surface Mount Capacitor, 4.7µF, 0201	GRM035R60J475ME15D	Murata Electronics
C8	1	X6S Surface Mount Capacitor, 0.068µF, 0201	GRM033C80J683KE84D	Murata Electronics
C16	1	X7R Surface Mount Capacitor, 1000pF, 0201	GRM033R71E102J	Murata Electronics
C17, C18, C19, C20, C22, C23, C24	0	DNI	DNI	DNI
C21	1	COG Surface Mount Capacitor, 0.010µF, 0402	GRM155R71E103J	Murata Electronics
C25	1	X7R Surface Mount Capacitor, 0.01µF, 0201	GRM033R70J103J	Murata Electronics
D1, D2, D3, D4	4	17V, 30V Clamp 5A, 2A (8/20µs) Ipp Tvs Diode Surface Mount LLP1006-2L	VCUT0714A-HD1-GS08	Vishay
J1, J2, J3, J4, J5, J6, J7, J8, J9, J10	10	2.92mm edge launch, Female Standard Profile	ELF40-002	Signal Microwave
J11	1	2x10 Connector Header Surface Mount 20 position 0.100" (2.54mm)	M20-8761042	Harwin
J12	1	MCX Connector Jack, Female Socket 50Ohm Through Hole Solder	0733660061	Molex
J15	1	1x2 Header, Gold, Unshrouded, Breakaway, 100mil (2.54mm) pitch	M20-8770246	Harwin
J16	1	2x4 Connector Header Surface Mount 8 position 0.100" (2.54mm)	M20-8760442	Harwin
R1, R34, R35, R36, R37	0	DNI	DNI	DNI
R5, R7, R9, R11, R13, R16, R17, R19, R21, R22, R25, R26, R38, R43	14	Surface Mount Resistor, 0Ohm, 0201	ERJ-1GN0R00C	Panasonic
R6, R8, R10, R12, R18, R20, R23, R24, R27, R28, R29, R30, R31, R33, R39, R44	0	DNI	DNI	DNI
R40, R41, R42	3	Surface Mount Resistor, 5.10kOhm, 0201	ERJ-1GEJ512C	Panasonic
SO1, SO2, SO3, SO4, SO5, SO6	6	Hex Standoff Threaded M3 Nylon 0.984" (25.00mm) Natural	25506	Keystone

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
TP1, TP2, TP3, TP4, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18	16	Phosphor Bronze Loop, Silver Plating Mini SMD	5019	Keystone
U1	1	8-channel TRX half-duplex silicon IC for dual polarization 5G phased-array	F52X8v300	Renesas
U2	1	Analog Temperature Sensor, Local -50°C ~ 150°C 8.2mV/°C SC-70-5	LMT85DCKR	Texas Instruments
U3	0	DNI	DNI	DNI
U4	1	12-Bit Digital Temperature Sensor, Local -40°C ~ 125°C 6-SOT	TMP112BIDRLR	Texas Instruments

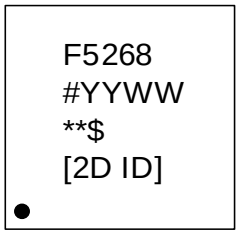
11. Evaluation System Information

See the F5268/F5288-Evaluation System Manual for instructions on how to use the evaluation board and graphical user interface software.

12. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

13. Marking Diagram



- Line 1: truncated part number.
- Line 2:
  - “#” denotes the stepping number
  - “YYWW” is the last two digits of the year and week that the part was assembled.
- Line 3:
  - “**” denotes the sequential lot number.
  - “$” denotes the mark code.
- Line 4: “2D ID” denotes barcode containing wafer and substrate information.

14. Ordering Information

Part Number	Package	MSL Rating	Carrier Type	Temp. Range
RA81F5268STGBX#BC0	5.1 × 5.1 × 0.8 mm 118-FCCSP	MSL 3	Tray	-40°C to +95°C
RA81F5268STGBX#HC0	5.1 × 5.1 × 0.8 mm 118-FCCSP	MSL 3	Reel	-40°C to +95°C
RTKA81F5268ST000RU	Evaluation Kit			

15. Revision History

Revision	Date	Description
1.02	Oct 30, 2024	▪ Added additional labels to the “Block Diagram”.
1.01	Jan 13, 2023	▪ Updated part numbers in Ordering Information. ▪ Updated Marking Diagram and diagram notes.
1.00	Oct 26, 2022	Initial release.