F5701

24.25GHz – 29.5GHz RF, 2.5GHz – 7GHz IF Upconverter/Downconverter

Description

The F5701 is a highly integrated RF upconverter/downconverter used in 5G beamforming applications targeting the n257/n261 and n258 bands. The device uses classic TX and RX heterodyne architectures to convert 2.5GHz to 7GHz IF signals to the 5G NR (new radio) millimeter-wave bands spanning the 24.25GHz to 29.5GHz spectrum. Low-side Local Oscillator (LO) injection is used with the TX and RX mixer cores supporting internal LO frequencies ranging between 17.25GHz and 27GHz. LO feed requirements are eased by two sequential on-chip LO frequency doublers that yield net multiplicative factors of either 2x or 4x. The F5701 supports programmability between separate RF ports for TX and RX, and a single RF input/output port with a low insertion loss TRX switch integrated on the chip, therefore, eliminating the need for an off-chip TRX switch for TDD applications. The F5701 provides real IF RX and TX ports with on-chip I/Q combination, resulting in much more relaxed requirements for IF routing, IF VGAs and data converters, compared to those of the up-down converters with complex I/Q IF interfaces. On-chip 9-bit DACs provide fine control for image-rejection calibration.

All RF, IF, and LO ports employ single-ended 50Ω impedances for ease of integration into the signal path. Each device uses a 2.5V analog supply and a programmable 2.5V–3.3V PA supply to provide a wide range of TX output power levels with high efficiency. The digital core and SPI use a 1.8V supply generated by an on-chip LDO.

Competitive Advantage

- Compact and highly-integrated design with low DC power consumption simplifies beamforming applications
- RF port programmability between RX/TX and TRX with integrated TRX switch provides ultimate flexibility and reduces RF routing and BOM cost
- On-chip I/Q combination with excellent sideband suppression and image rejection halves IF routing, VGAs and Data Converters
- Industry-leading TX linearity allows a single transceiver to drive up to 64 elements
- Two sequential LO frequency doublers eliminate the need to route troublesome high-frequency LO signals on printed circuit board (PCB)
- Advanced LO leakage calibration mechanism provides industry-leading performance

Features

General

- RF range: 24.25GHz to 29.5GHz (n257/n258)
- IF range: 2.5GHz to 7GHz
- Two integrated LO frequency doublers
- Analog supply voltage: +2.4V to +2.6V
- Dedicated PA supply voltage: selectable between +2.4V to +2.6V and +3.0V to +3.3V
- Operating temperature (T_A) range: -40°C to +95°C
- 4.0 × 4.5 × 0.9 mm 49-BGA package

Transmit Mode (Typical Across RF/IF Bands)

- > 28.9dB conversion gain from the IF/RF amplifiers and single-sideband (SSB) mixer core
- > +19.5dBm OP1dB and > +28dBm OIP3
- 30dB of Glitch-Free™ gain adjustment
- < -36dBc LO leakage and > 27dBc sideband suppression across the RF frequency band
- Envelope detector provided for accurate LO leakage estimation and calibration loop-back

Receive Mode (Typical Across RF/IF Bands)

- > 21dB conversion gain from the RF/IF amplifiers and image-reject mixer (IRM) core
- < 6.6dB noise figure (5.4dB for the RX2 path)
- > -15.3dBm IP1dB and > -7.8dBm IIP3
- 30dB of Glitch-Free gain adjustment
- > 33dBc image rejection across the RF frequency band
- Several additional knobs to trade off NF with IIP3

Applications

- 5G Phased Arrays and Massive MIMO

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1. Overview

1.1 Block Diagram

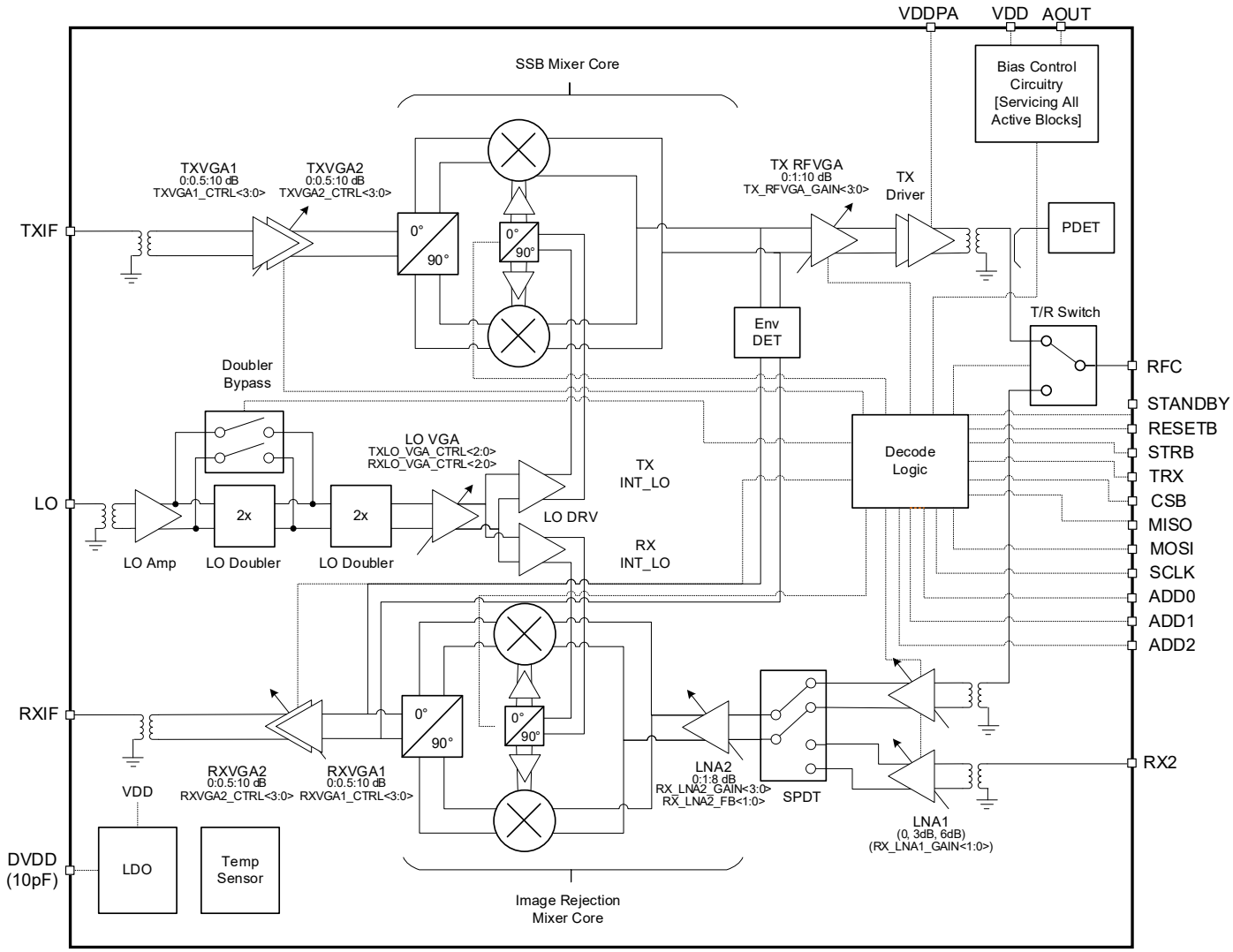

Figure 1. Block Diagram

2. Pin Information

2.1 Pin Assignments

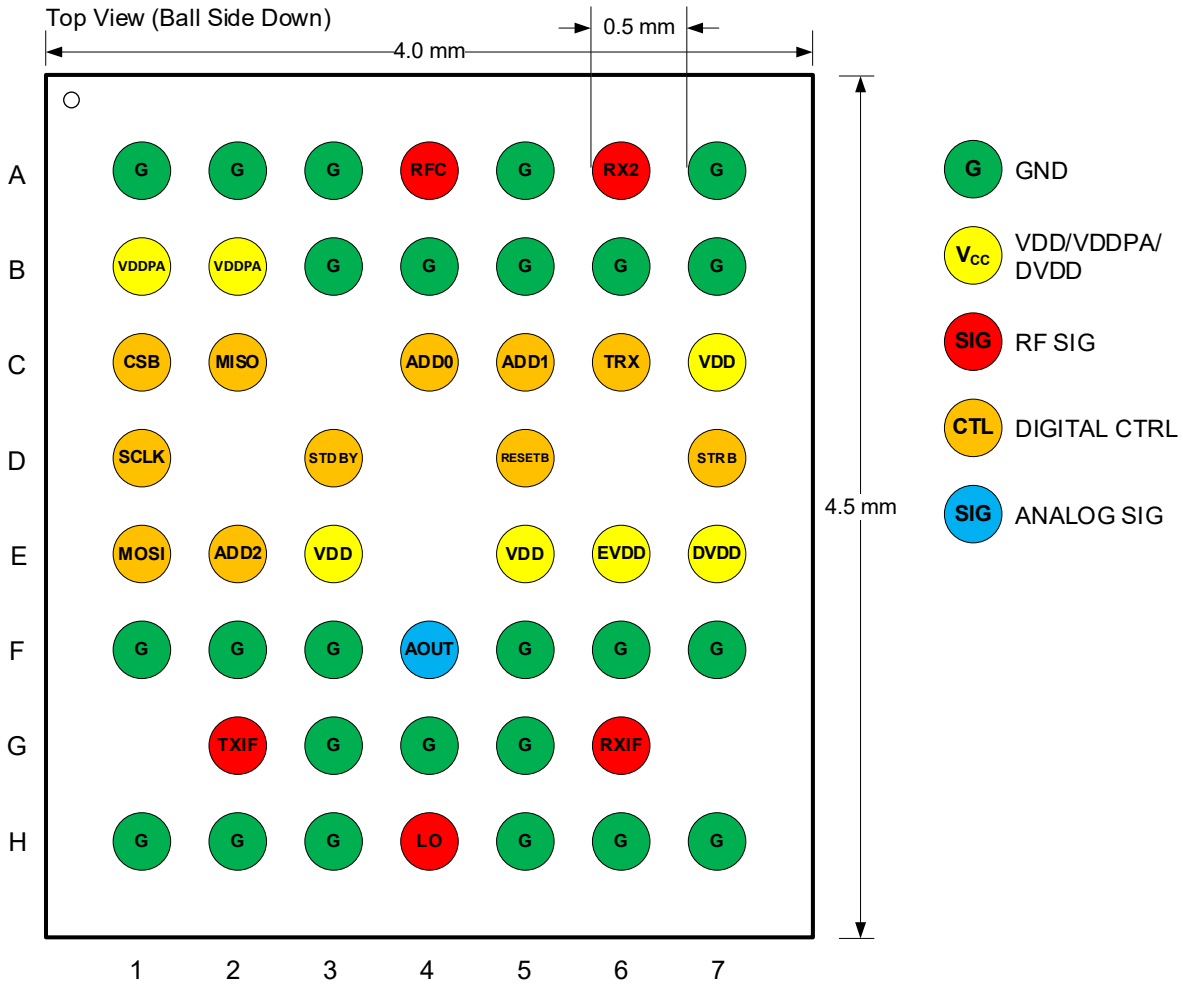

Figure 2. Pin Assignments – Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
A1, A2, A3, A5, A7, B3, B4, B5, B6, B7, F1, F2, F3, F5, F6, F7, G3, G4, G5, H1, H2, H3, H5, H6, H7	GND	Ground pins.
A4	RFC	RF input/output internally matched to 50Ω (single-ended).
A6	RX2	RF input for the second RX path internally matched to 50Ω (single-ended).
B1, B2	VDDPA	2.5V/3.3V analog power supply for PA.
C1	CSB (PD) [1]	Chip select input. 1.8V logic compatible.
C2	MISO	Serial data output. 1.8V logic compatible.
C4	ADD0 (PU)	Static chip address Bit 0 for SPI. Float for 1 or connect to ground for 0.

Pin Number	Pin Name	Description
C5	ADD1 (PU)	Static chip address Bit 1 for SPI. Float for 1 or connect to ground for 0.
C6	TRX (PU)	Transmit/receive mode select. Logic HIGH = TX mode. Logic LOW = RX mode.
C7, E3, E5	VDD	2.5V analog power supply. Connect to a common VDD and use bypass capacitors as close to the pin as possible.
D1	SCLK (PD)	Clock input. 1.8V logic compatible.
D3	STDBY (PU)	Standby pin. When a logic HIGH is applied to this pin (or this pin is left unconnected), the amplifier is powered off with the SPI still powered on (standby mode). When a logic LOW is applied to this pin, the part is in full operation mode. *Note*: In the standby mode, the master bias is disabled.
D5	RESETB (PU)	Active LOW = microcontroller reset. Clears and resets the on-chip registers to their power-on reset defaults.
D7	STRB	Digitally programmable strobe pin.
E1	MOSI (PD)	Serial data input. 1.8V logic compatible.
E2	ADD2 (PU)	Static chip address Bit 2 for SPI. Float for 1 or connect to ground for 0.
E6	EVDD	EFUSE programming supply voltage pin for write operation (internal use only). For read operation, connect to the VDD pin for the 2.5V supply.
E7	DVDD	Internal 1.8V digital power supply pin. Place 10µF bypass capacitor as close to the pin as possible.
F4	AOUT	Analog DC voltage test port. Used for debug/production test. This pin can be grounded or left floating if not used.
G2	TXIF	TX input internally matched to 50Ω (single ended).
G6	RXIF	RX output internally matched to 50Ω (single-ended).
H4	LO	External LO input internally matched to 50Ω (single-ended).

1. Pull-up (PU) and pull-down (PD) resistors, if applicable, are indicated in parentheses. The resistance is approximately 100kΩ.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F5701 at absolute maximum ratings is not implied. Exposure to such conditions might affect device reliability.

Parameter	Symbol	Minimum	Maximum	Unit
Analog Supply Voltage	V_{DD}	-0.3	+3.0	V
PA Supply Voltage	V_{DDPA}	-0.3	+3.3	V
MISO, MOSI, CSB, CLK, STRB, ADD1, ADD2, ADD3, AOUT, RESETB	V_{CTL}	-0.3	+2.1	V
EFUSE Supply Voltage	V_{EVDD}	-0.3	+4.5	V
RF to GND Externally Applied DC Voltage	V_{RF}	-0.3	+0.3	V
TXIF to GND Externally Applied DC voltage	V_{TXIF}	-0.3	+0.3	V
RXIF to GND Externally Applied DC voltage	V_{RXIF}	-0.3	+0.3	V
EXTLO to GND Externally Applied DC Voltage	V_{LO}	-0.3	+0.3	V
TX IF Input Continuous Wave (CW) Power Applied for 24 Hours Maximum [1] ▪ RF Output VSWR < 2:1 in a 50Ω system ▪ IF Input VSWR = 1:1 in a 50Ω system ▪ T_A = 95°C [1] ▪ V_{DD} = +2.5V ▪ V_{DDPA} = +2.5V to +3.3V	P_{MAX24_TX}	-	5	dBm
RX RF Input CW Power Applied for 24 Hours Maximum [1] ▪ RF Input VSWR = 1:1 in a 50Ω system ▪ IF Output VSWR < 2:1 in a 50Ω system ▪ T_A = 95°C [1] ▪ V_{DD} = +2.5V ▪ V_{DDPA} = +2.5V to +3.3V	P_{MAX24_RX}	-	0	dBm
Junction Temperature	T_J	-	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}	-	+260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}	-	2000 (Class 2)	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)	V_{ESDCDM}	-	500 (Class C4)	V

1. Exposure to these maximum RF levels can result in significant V_{CC} current draw because of overdriving the amplifier stages.
2. T_A = ambient temperature of the device.

3.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Analog Supply Voltage [1]	V_{DD}	-	+2.4	+2.5	+2.6	V
PA Supply Voltage	V_{DDPA}	Default power mode	+2.4	+2.5	+2.6	V
		High power mode	+3.0	-	+3.3	
Operating Temperature Range	T_A	Ambient temperature	-40	-	+95	°C
RF Frequency Range	f_{RF}	-	24.25	-	29.5	GHz
RF Occupied Bandwidth	BW	Instantaneous bandwidth	50	-	800	MHz
IF Frequency Range	f_{IF}	-	2.5	-	7	GHz
Internal LO Frequency Range [2]	f_{INTLO}	-	18.25	-	27	GHz
External LO Frequency Range [3] (Input at EXTLO Port)	f_{EXTLO}	2x LO multiplier	8.625	-	13.5	GHz
		4x LO multiplier	4.3125	-	6.75	GHz
External LO Drive Level	P_{EXTLO}	-	-10	-	0	dBm
TX IF Input Power [4]	$P_{MAX\_CW\_TX}$	CW	-	-	2	dBm
	$P_{MAX\_AV\_TX}$	Modulated: PAPR = 6dB	-	-	-4	
		Modulated: PAPR = 11dB	-	-	-9	
		Modulated: PAPR = 13dB	-	-	-11	
RF Port Impedance	Z_{RF}	Single-ended	-	50	-	Ω
LO Port Impedance	Z_{LO}	Single-ended	-	50	-	Ω
IF Port Impedance	Z_{IF}	Single-ended	-	50	-	Ω

1. Power-on resets only occur for V_{DD} < 1.7V. Device is designed to function with any supply voltage ≥ 1.9V, although performance might be degraded when operated outside the recommended voltage range.
2. The internal LO frequency is representative of the signal that is present at the mixer core after being subjected to one or both LO doubler stages.
3. The external LO frequency refers to the LO signal that is presented at the EXTLO port of the device. This signal is eventually multiplied by a factor of 2x or 4x before reaching the mixer core. (f_{LOINT} = 2 x f_{EXTLO}, or f_{LOINT} = 4 x f_{EXTLO}).
4. Recommended maximum average input power level for long-term reliability. Conditions: V_{DD} = +2.5V, V_{DDPA} = +2.5V to +3.3V, T_A = 95°C. $P_{MAX\_AV\_TX}$ = $P_{MAX\_CW\_TX}$ – PAPR, where PAPR is the Peak-To-Average Power Ratio of the modulated input signals.

3.3 Thermal Specifications

Parameter	Symbol	Value	Unit
Junction-to-Ambient Thermal Resistance	θ_{JA}	48.6	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	44.7	°C/W
Junction-to-Board Thermal Resistance	θ_{JB}	18.6	°C/W
Storage Temperature	T_{STOR}	-40 to +150	°C
Moisture Sensitivity Rating (Per J-STD-020)	-	MSL 3	-

3.4 Electrical Specifications

3.4.1 General

See the F5701 Evaluation Board (EVB) circuit (Figure 404 and Figure 405). Specifications apply when operated at V_{DD} = +2.5V, V_{DDPA} = +2.5V, f_{RF} = 26GHz and 28GHz, T_A = +25°C, P_{EXTLO} = -10dBm, RESETB = HIGH, $Z_{RF} = Z_{LO} = Z_{IF}$ = 50Ω, maximum gain setting (for example, all digital step attenuators (DSAs) = 0dB, all variable gain amplifiers (VGAs) set to maximum gain), P_{OUT} = 0dBm/tone, EVB traces and connectors are de-embedded, unless otherwise stated.

Parameter	Symbol	Conditions		Minimum	Typical	Maximum	Unit
Logic Input High Threshold	V_{IH}	-		1.17	-	1.95	V
Logic Input Low Threshold	V_{IL}	-		-0.3	-	0.63	V
Logic Input Current	I_{IH}, I_{IL}	For each input control pin		-	50	-	µA
Logic Output High Voltage	V_{OH}	-		1.35	-	1.8	V
Logic Output Low Voltage	V_{OL}	-		-	-	0.45	V
Logic Output High Driving Current	I_{OH}	-		-	8	-	mA
Logic Output Low Driving Current	I_{OL}	-		-	8	-	mA
Analog Supply Current	I_{VDD}	Standby mode		-	4	-	mA
		TX Mode	P_{OUT} at P1dB-10dB Over PVT	-	283 (284) [1]	-	
			P_{OUT} at P1dB Over PVT	-	295 (297) [1]	-	
		RX Mode Over VT		-	247	-	
PA Supply Current	I_{VDDPA}	Standby mode		-	0.5	-	mA
		TX Mode	P_{OUT} at P1dB-10dB Over PVT	-	99 (110) [1]	-	
			P_{OUT} at P1dB Over PVT	-	204 (225) [1]	-	
		RX Mode Over VT		-	0.5	-	
Power ON Switching Time	t_{ON}	50% STBY to RF output settled to within ±0.5dB of final gain value.		-	100	-	ns
Power OFF Switching Time	t_{OFF}	50% STBY to 35dBc reduction of output power.		-	100	-	ns
TDD Switching Time	t_{TX-RX}	TX mode to RX mode		-	100	-	ns
	t_{RX-TX}	RX mode to TX mode		-	100	-	
Serial Clock Speed	f_{CLK}	-		-	-	62.5	MHz

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
CSB to First Serial Clock Rising Edge	t_{LS}	SPI 3 wire Bus. 50% of CSB falling edge to 50% of CLK rising edge.	-	8	-	ns
Serial Data Hold Time	t_{H}	SPI 3 wire Bus. 50% of CLK rising edge to 50% of DATA falling edge.	-	8	-	ns
Final Serial Clock Rising Edge to CSB	t_{LCS}	SPI 3 wire Bus. 50% of CLK rising edge to 50% of CSB rising edge.	-	8	-	ns

1. For V_{DDPA} = +3.3V.

3.4.2 5GHz IF/28GHz RF (Band H8) – TX

See the F5701 EVB circuit (Figure 404 and Figure 405). Specifications apply when operated in TX Mode with V_{DD} = +2.5V, V_{DDPA} = +2.5V, T_A = +25°C, f_{RF} = 28GHz, f_{EXTLO} = 11.5GHz, f_{IF} = 5GHz, LO Multiplier Factor = 2, LO Injection = Low Side, P_{EXTLO} = -10dBm, RESETB = HIGH, $Z_{RF} = Z_{LO} = Z_{IF}$ = 50Ω single ended, maximum gain setting (TX IF DSA = 0dB, and TX RF VGA set to maximum gain), and P_{OUT} = 0dBm/tone, unless stated otherwise. EVB trace and connector losses are de-embedded.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Recommended RF Frequency Range	f_{RF}	-	26.5	28	29.5	GHz
Recommended IF Frequency Range	f_{IF}	-	3.5	5	7	GHz
IF Input Return Loss	RL_{IFIN}	f_{IF} = 3.5GHz to 7GHz Over PVT	-	11.7	-	dB
External LO Input Return Loss	RL_{EXTLO}	f_{EXTLO} = 9.75GHz to 13GHz Over PVT	-	12	-	dB
		f_{EXTLO} = 4.875GHz to 6.5GHz Over PVT	-	12	-	dB
RF Output Return Loss	RL_{RFOUT}	f_{RF} = 26.5GHz to 29.5GHz Over PVT	-	4.6 (3.6) [1]	-	dB
Maximum Small Signal Conversion Gain	G_{MAX}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	28.9 (29) [1]	-	dB
IF DSA Adjustment Range	G_{IFDSA_RANGE}	-	-	20	-	dB
IF DSA Step Resolution	G_{IFDSA_STEP}	LSB	-	0.5	-	dB
Phase Shift Relative to the 0dB IF DSA Attenuation State	$\Phi_{IFDSA\_\Delta MID1}$	IF DSA 5dB Attenuation	-	± 1.25	-	deg
	$\Phi_{IFDSA\_\Delta MID2}$	IF DSA 10dB Attenuation	-	± 2.5	-	deg
	$\Phi_{IFDSA\_\Delta MAX}$	IF DSA 20dB Attenuation	-	± 3.75	-	deg
IF DSA Gain Settling Time	t_{IFDSA_ST}	Any 1dB step in the 0dB to 15dB range. 50% of CSB to 10% / 90% RF	-	30	-	ns

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
RF VGA Adjustment Range	G_{RFDSA_RANGE}	-	-	10	-	dB
RF VGA Step Resolution	G_{RFDSA_STEP}	LSB	-	1.0	-	dB
RF VGA Gain Settling Time	t_{RFVGA_ST}	Any 1dB step in the 0dB to 10dB range. 50% of CSB to 10% / 90% RF	-	30	-	ns
Noise Figure	NF_{MAX_G}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	12.2 (12.5) [1]	-	dB
Output Third Order Intercept Point	OIP3	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	29.3 (30.2) [1]	-	dBm
Output 1dB Compression Point	OP1dB	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	19.5 (21.1) [1]	-	dBm
LO Leakage	LOL	f_{RF} = 26.5GHz to 29.5GHz Uncalibrated RF Output Power = 8dBm	-	-42 (-40.9) [1]	-	dBc
		f_{RF} = 26.5GHz to 29.5GHz Calibrated RF Output Power = 8dBm	-	-49 (-49.3) [1]	-	
TX EVM	EVM_{TX}	RF Output Power = 8dBm (9dBm with V_{DDPA} =+3.3V)	-	1.0 (0.8) [1]	-	%
TX-RX Isolation	ISO_{TX-RX}	-	-	35	-	dB
M x N Spurious Rejection	M x N	f_{RF} = 21GHz to 32.5GHz RF Output Power = 8dBm	-	35	-	dBc
		All other bands.	-	40	-	dBc
Sideband Suppression	SBS	f_{RF} = 26.5GHz to 29.5GHz Uncalibrated RF Output Power = 8dBm	-	51 (53.5) [1]	-	dBc

1. For V_{DDPA} = +3.3V.

3.4.3 5GHz IF/28GHz RF (Band H8) – RX

See the F5701 EVB circuit (Figure 404 and Figure 405). Specifications apply when operated in RX Mode with V_{DD} = +2.5V, V_{DDPA} = +2.5V, T_A = +25°C, f_{RF} = 28GHz, f_{EXTLO} = 11.5GHz, f_{IF} = 5GHz, LO Multiplier Factor = 2, LO Injection = Low Side, P_{EXTLO} = -10dBm, RESETB = HIGH, $Z_{RF} = Z_{LO} = Z_{IF}$ = 50Ω single ended , maximum gain setting (RX IF DSA = 0dB, and RX RF VGA set to maximum gain), P_{RF} = -30dBm, P_{IF_OUT} = -5 dBm/tone, and TBD tone spacing, unless stated otherwise. EVB trace and connector losses are de-embedded.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Recommended RF Frequency Range	f_{RF}	-	26.5	28	29.5	GHz
Recommended IF Frequency Range	f_{IF}	-	3.5	5	7	GHz
IF Output Return Loss	RL_{IFOUT}	f_{IF} = 3.5GHz to 7GHz Over PVT	-	12.7	-	dB
External LO Input Return Loss	RL_{EXTLO}	f_{EXTLO} = 9.75GHz to 13GHz Over PVT	-	12	-	dB
		f_{EXTLO} = 4.875GHz to 6.5GHz Over PVT	-	12	-	dB
RF Input Return Loss	RL_{RF_IN}	f_{RF} = 26.5GHz to 29.5GHz Over PVT	-	11.9	-	dB
Maximum Small Signal Conversion Gain	G_{MAX}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	22.7 (23.9) [1]	-	dB
Gain Variation Over IF Range	$G_{VAR\_\Delta IF}$	f_{RF} = 28GHz f_{EXTLO} = 10.5GHz to 12.25GHz f_{IF} = 3.5GHz to 7GHz Referenced to f_{IF} = 5GHz	-	2.2	-	dB
Gain Flatness	G_{FLAT}	Over any 100MHz bandwidth	-	0.2	-	dB
		Over any 1GHz bandwidth	-	0.7	-	dB
		Over any 3GHz bandwidth	-	0.9	-	dB
IF DSA Adjustment Range	G_{IFDSA_RANGE}	-	-	20	-	dB
IF DSA Step Resolution	G_{IFDSA_STEP}	LSB	-	0.5	-	dB
IF DSA Gain Settling Time	t_{IFDSA_ST}	Any 1dB step in the 0dB to 15dB range. 50% of CSB to 10% / 90% RF	-	30	-	ns
RF VGA Adjustment Range	G_{RFDSA_RANGE}	-	-	10	-	dB
RF VGA Step Resolution	G_{RFDSA_STEP}	LSB	-	1.0	-	dB
RF DSA Gain Settling Time	t_{RFDSA_ST}	Any 1dB step in the 0dB to 15dB range. 50% of CSB to 10% / 90% RF	-	30	-	ns
Noise Figure (SSB, No Blockers Present)	NF_{MAX_G}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	5.8 (4.8) [1]	-	dB

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input Third Order Intercept Point	IIP3	IF DSA setting = 0dB RF VGA setting = Max Gain P_{RF} = -30dBm / tone 100MHz Tone Spacing Over PVT	-	-7.2 (-8.2) [1]	-	dBm
Input 1dB Compression Point	IP1dB	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	-15.3 (-16.6) [1]	-	dBm
Image Rejection	IRR	f_{RF} = 26.5GHz to 29.5GHz Uncalibrated Over PVT	-	46.9 (44.5) [1]	-	dBc

1. For the separate RX2 path.

3.4.4 5GHz IF/26GHz RF (Band H6) – TX

See the F5701 EVB circuit (Figure 404 and Figure 405). Specifications apply when operated in TX Mode with V_{DD} = +2.5V, V_{DDPA} = +2.5V, T_A = +25°C, f_{RF} = 26GHz, f_{EXTLO} = 10.5GHz, f_{IF} = 5GHz, LO Multiplier Factor = 2, LO Injection = Low Side, P_{EXTLO} = -10dBm, RESETB = HIGH, Z_{RF} = Z_{LO} = Z_{IF} = 50Ω single ended, maximum gain setting (TX IF DSA = 0dB, and TX RF VGA set to maximum gain), and P_{OUT} = 0dBm/tone, unless stated otherwise. EVB trace and connector losses are de-embedded.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Recommended RF Frequency Range	f_{RF}	-	24.25	26	27.5	GHz
Recommended IF Frequency Range	f_{IF}	-	3.5	5	7	GHz
IF Input Return Loss	RL_{IFIN}	f_{IF} = 3.5GHz to 7GHz Over PVT	-	11.7	-	dB
External LO Input Return Loss	RL_{EXTLO}	f_{EXTLO} = 8.625GHz to 12GHz Over PVT	-	12	-	dB
		f_{EXTLO} = 4.3125GHz to 6GHz Over PVT	-	12	-	dB
RF Output Return Loss	RL_{RFOUT}	f_{RF} = 24.25GHz to 27.5GHz Over PVT	-	6.5 (6) [1]	-	dB
Maximum Small Signal Conversion Gain	G_{MAX}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	29.3 (29.4) [1]	-	dB
IF DSA Adjustment Range	G_{IFDSA_RANGE}	-	-	20	-	dB
IF DSA Step Resolution	G_{IFDSA_STEP}	LSB	-	0.5	-	dB
Phase Shift Relative to the 0dB IF DSA Attenuation State	$\Phi_{IFDSA\_\Delta MID1}$	IF DSA 5dB Attenuation	-	± 1.25	-	deg
	$\Phi_{IFDSA\_\Delta MID2}$	IF DSA 10dB Attenuation	-	± 2.5	-	deg
	$\Phi_{IFDSA\_\Delta MAX}$	IF DSA 20dB Attenuation	-	± 3.75	-	deg

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
IF DSA Gain Settling Time	t_{IFDSA_ST}	Any 1dB step in the 0dB to 15dB range. 50% of CSB to 10% / 90% RF	-	30	-	ns
RF VGA Adjustment Range	G_{RFDSA_RANGE}	-	-	10	-	dB
RF VGA Step Resolution	G_{RFDSA_STEP}	LSB	-	1.0	-	dB
RF VGA Gain Settling Time	t_{RFVGA_ST}	Any 1dB step in the 0dB to 10dB range. 50% of CSB to 10% / 90% RF	-	30	-	ns
Noise Figure	NF_{MAX_G}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	12.7 (12.8) [1]	-	dB
Output Third Order Intercept Point	OIP3	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	31.8 (33.6) [1]	-	dBm
Output 1dB Compression Point	OP1dB	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	20.3 (22.4) [1]	-	dBm
LO Leakage	LOL	f_{RF} = 24.25GHz to 27.5GHz Uncalibrated RF Output Power = 8dBm	-	-45.3 (-46) [1]	-	dBc
		f_{RF} = 24.25GHz to 27.5GHz Calibrated RF Output Power = 8dBm	-	-58.6 (-60) [1]	-	
TX EVM	EVM_{TX}	RF Output Power = 8dBm (9dBm with V_{DDPA} = +3.3V)	-	1.0 (0.8) [1]	-	%
TX-RX Isolation	ISO_{TX-RX}	-	-	35	-	dB
M x N Spurious Rejection	M x N	f_{RF} = 21GHz to 32.5GHz RF Output Power = 8dBm	-	35	-	dBc
		All other bands.	-	40	-	dBc
Sideband Suppression	SBS	f_{RF} = 24.25GHz to 27.5GHz Uncalibrated RF Output Power = 8dBm	-	70 (70) [1]	-	dBc

1. For V_{DDPA} = +3.3V.

3.4.5 5GHz IF/26GHz RF (Band H6) – RX

See the F5701 EVB circuit (Figure 404 and Figure 405). Specifications apply when operated in RX Mode with V_{DD} = +2.5V, V_{DDPA} = +2.5V, T_A = +25°C, f_{RF} = 26GHz, f_{EXTLO} = 10.5GHz, f_{IF} = 5GHz, LO Multiplier Factor = 2, LO Injection = Low Side, P_{EXTLO} = -10dBm, RESETB = HIGH, $Z_{RF} = Z_{LO} = Z_{IF}$ = 50Ω single ended , maximum gain setting (RX IF DSA = 0dB, and RX RF VGA set to maximum gain), P_{RF} = -30dBm, P_{IF_OUT} = -5 dBm/tone, and TBD tone spacing, unless stated otherwise. EVB trace and connector losses are de-embedded.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Recommended RF Frequency Range	f_{RF}	-	24.25	26	27.5	GHz
Recommended IF Frequency Range	f_{IF}	-	3.5	5	7	GHz
IF Output Return Loss	RL_{IFOUT}	f_{IF} = 3.5GHz to 7GHz Over PVT	-	12.7	-	dB
External LO Input Return Loss	RL_{EXTLO}	f_{EXTLO} = 8.625GHz to 12GHz Over PVT	-	12	-	dB
		f_{EXTLO} = 4.3125GHz to 6GHz Over PVT	-	12	-	dB
RF Input Return Loss	RL_{RF_IN}	f_{RF} = 24.25GHz to 27.5GHz Over PVT	-	11.8	-	dB
Maximum Small Signal Conversion Gain	G_{MAX}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	21.5 (22.5) [1]	-	dB
Gain Variation Over IF Range	$G_{VAR\_\Delta IF}$	f_{RF} = 26GHz f_{EXTLO} = 9.5GHz to 11.25GHz f_{IF} = 3.5GHz to 7GHz Referenced to f_{IF} = 5GHz	-	2.6	-	dB
Gain Flatness	G_{FLAT}	Over any 100MHz bandwidth	-	0.2	-	dB
		Over any 1GHz bandwidth	-	1.1	-	dB
		Over any 3GHz bandwidth	-	1.6	-	dB
IF DSA Adjustment Range	G_{IFDSA_RANGE}	-	-	20	-	dB
IF DSA Step Resolution	G_{IFDSA_STEP}	LSB	-	0.5	-	dB
IF DSA Gain Settling Time	t_{IFDSA_ST}	Any 1dB step in the 0dB to 15dB range. 50% of CSB to 10% / 90% RF	-	30	-	ns
RF VGA Adjustment Range	G_{RFDSA_RANGE}	-	-	10	-	dB
RF VGA Step Resolution	G_{RFDSA_STEP}	LSB	-	1.0	-	dB
RF DSA Gain Settling Time	t_{RFDSA_ST}	Any 1dB step in the 0dB to 15dB range. 50% of CSB to 10% / 90% RF	-	30	-	ns
Noise Figure (SSB, No Blockers Present)	NF_{MAX_G}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	6.4 (5.2) [1]	-	dB

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input Third Order Intercept Point	IIP3	IF DSA setting = 0dB RF VGA setting = Max Gain P_{RF} = -30dBm / tone 100MHz Tone Spacing Over PVT	-	-7.1 (-8) [1]	-	dBm
Input 1dB Compression Point	IP1dB	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	-14.1 (-15.2) [1]	-	dBm
Image Rejection	IRR	f_{RF} = 24.25GHz to 27.5GHz Uncalibrated Over PVT	-	46.6 (42.8) [1]	-	dBc

1. For the separate RX2 path.

3.4.6 5GHz IF/26GHz RF (Band H6h) – RX (High Linearity Mode)

See the F5701 EVB circuit (Figure 404 and Figure 405). Specifications apply when operated in RX Mode with V_{DD} = +2.5V, V_{DDPA} = +2.5V, T_A = +25°C, f_{RF} = 26GHz, f_{EXTLO} = 10.5GHz, f_{IF} = 5GHz, LO Multiplier Factor = 2, LO Injection = Low Side, P_{EXTLO} = -10dBm, RESETB = HIGH, Z_{RF} = Z_{LO} = Z_{IF} = 50Ω single ended , maximum gain setting (RX IF DSA = 0dB, and RX RF VGA set to maximum gain), P_{RF} = -30dBm, P_{IF_OUT} = -5 dBm/tone, and TBD tone spacing, unless stated otherwise. EVB trace and connector losses are de-embedded.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Recommended RF Frequency Range	f_{RF}	-	24.25	26	27.5	GHz
Recommended IF Frequency Range	f_{IF}	-	3.5	5	7	GHz
IF Output Return Loss	RL_{IFOUT}	f_{IF} = 3.5GHz to 7GHz Over PVT	-	12.7	-	dB
External LO Input Return Loss	RL_{EXTLO}	f_{EXTLO} = 8.625GHz to 12GHz Over PVT	-	12	-	dB
		f_{EXTLO} = 4.3125GHz to 6GHz Over PVT	-	12	-	dB
RF Input Return Loss	RL_{RF_IN}	f_{RF} = 24.25GHz to 27.5GHz Over PVT	-	11.8	-	dB
Maximum Small Signal Conversion Gain	G_{MAX}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	13.1	-	dB
Gain Variation Over IF Range	$G_{VAR\_\Delta IF}$	f_{RF} = 26GHz f_{EXTLO} = 9.5GHz to 11.25GHz f_{IF} = 3.5GHz to 7GHz Referenced to f_{IF} = 5GHz	-	2.7	-	dB
Gain Flatness	G_{FLAT}	Over any 100MHz bandwidth	-	0.3	-	dB
		Over any 1GHz bandwidth	-	2.4	-	dB
		Over any 3GHz bandwidth	-	3.8	-	dB
IF DSA Adjustment Range	G_{IFDSA_RANGE}	-	-	20	-	dB

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
IF DSA Step Resolution	G_{IFDSA_STEP}	LSB	-	0.5	-	dB
IF DSA Gain Settling Time	t_{IFDSA_ST}	Any 1dB step in the 0dB to 15dB range. 50% of CSB to 10% / 90% RF	-	30	-	ns
RF VGA Adjustment Range	G_{RFDSA_RANGE}	-	-	6	-	dB
RF VGA Step Resolution	G_{RFDSA_STEP}	LSB	-	3	-	dB
Noise Figure (SSB, No Blockers Present)	NF_{MAX_G}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	10.8	-	dB
Input Third Order Intercept Point	IIP3	IF DSA setting = 0dB RF VGA setting = Max Gain P_{RF} = -30dBm / tone 100MHz Tone Spacing Over PVT	-	1.5	-	dBm
Input 1dB Compression Point	IP1dB	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	-8.1	-	dBm
Image Rejection	IRR	f_{RF} = 24.25GHz to 27.5GHz Uncalibrated Over PVT	-	41.6	-	dBc

3.4.7 3GHz IF/28GHz RF (Band L8) – TX

See the F5701 EVB circuit (Figure 404 and Figure 405). Specifications apply when operated in TX Mode with V_{DD} = +2.5V, V_{DDPA} = +2.5V, T_A = +25°C, f_{RF} = 28GHz, f_{EXTLO} = 12.5GHz, f_{IF} = 3GHz, LO Multiplier Factor = 2, LO Injection = Low Side, P_{EXTLO} = -10dBm, RESETB = HIGH, $Z_{RF} = Z_{LO} = Z_{IF}$ = 50Ω single ended, maximum gain setting (TX IF DSA = 0dB, and TX RF VGA set to maximum gain), and P_{OUT} = 0dBm/tone, unless stated otherwise. EVB trace and connector losses are de-embedded.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Recommended RF Frequency Range	f_{RF}	-	26.5	28	29.5	GHz
Recommended IF Frequency Range	f_{IF}	-	2.5	3	4	GHz
IF Input Return Loss	RL_{IFIN}	f_{IF} = 2.5GHz to 4GHz Over PVT	-	13.6	-	dB
External LO Input Return Loss	RL_{EXTLO}	f_{EXTLO} = 11.25GHz to 13.5GHz Over PVT	-	12	-	dB
		f_{EXTLO} = 5.625GHz to 6.75GHz Over PVT	-	12	-	dB
RF Output Return Loss	RL_{RFOUT}	f_{RF} = 26.5GHz to 29.5GHz Over PVT	-	3.6 (3.6) [1]	-	dB
Maximum Small Signal Conversion Gain	G_{MAX}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	32.9 (32.7) [1]	-	dB

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
IF DSA Adjustment Range	G_{IFDSA_RANGE}	-	-	20	-	dB
IF DSA Step Resolution	G_{IFDSA_STEP}	LSB	-	0.5	-	dB
Phase Shift Relative to the 0dB IF DSA Attenuation State	$\Phi_{IFDSA\_\Delta MID1}$	IF DSA 5dB Attenuation	-	±1.25	-	deg
	$\Phi_{IFDSA\_\Delta MID2}$	IF DSA 10dB Attenuation	-	±2.5	-	deg
	$\Phi_{IFDSA\_\Delta MAX}$	IF DSA 20dB Attenuation	-	±3.75	-	deg
IF DSA Gain Settling Time	t_{IFDSA_ST}	Any 1dB step in the 0dB to 15dB range. 50% of CSB to 10% / 90% RF	-	30	-	ns
RF VGA Adjustment Range	G_{RFDSA_RANGE}	-	-	10	-	dB
RF VGA Step Resolution	G_{RFDSA_STEP}	LSB	-	1.0	-	dB
RF VGA Gain Settling Time	t_{RFVGA_ST}	Any 1dB step in the 0dB to 10dB range. 50% of CSB to 10% / 90% RF	-	30	-	ns
Noise Figure	NF_{MAX_G}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	10 (9.8) [1]	-	dB
Output Third Order Intercept Point	OIP3	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	28 (29) [1]	-	dBm
Output 1dB Compression Point	OP1dB	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	19.7 (21) [1]	-	dBm
LO Leakage	LOL	f_{RF} = 26.5GHz to 29.5GHz Uncalibrated RF Output Power = 8dBm	-	-40 (-40) [1]	-	dBc
		f_{RF} = 26.5GHz to 29.5GHz Calibrated RF Output Power = 8dBm	-	-45.7 (-45.9) [1]	-	
TX EVM	EVM_{TX}	RF Output Power = 8dBm (9dBm with V_{DDPA} = +3.3V)	-	1.0 (0.8) [1]	-	%
TX-RX Isolation	ISO_{TX-RX}	-	-	35	-	dB
M x N Spurious Rejection	M x N	f_{RF} = 21GHz to 32.5GHz RF Output Power = 8dBm	-	35	-	dBc
		All other bands.	-	40	-	dBc
Sideband Suppression	SBS	f_{RF} = 26.5GHz to 29.5GHz Uncalibrated RF Output Power = 8dBm	-	32 (32) [1]	-	dBc

1. For V_{DDPA} = +3.3V.

3.4.8 3GHz IF/28GHz RF (Band L8) – RX

See the F5701 EVB circuit (Figure 404 and Figure 405). Specifications apply when operated in RX Mode with V_{DD} = +2.5V, V_{DDPA} = +2.5V, T_A = +25°C, f_{RF} = 28GHz, f_{EXTLO} = 12.5GHz, f_{IF} = 3GHz, LO Multiplier Factor = 2, LO Injection = Low Side, P_{EXTLO} = -10dBm, RESETB = HIGH, Z_{RF} = Z_{LO} = Z_{IF} = 50Ω single ended , maximum gain setting (RX IF DSA = 0dB, and RX RF VGA set to maximum gain), P_{RF} = -30dBm, P_{IF_OUT} = -5 dBm/tone, and TBD tone spacing, unless stated otherwise. EVB trace and connector losses are de-embedded.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Recommended RF Frequency Range	f_{RF}	-	26.5	28	29.5	GHz
Recommended IF Frequency Range	f_{IF}	-	2.5	3	4	GHz
IF Output Return Loss	RL_{IFOUT}	f_{IF} = 2.5GHz to 4GHz Over PVT	-	12	-	dB
External LO Input Return Loss	RL_{EXTLO}	f_{EXTLO} = 11.25GHz to 13.5GHz Over PVT	-	12	-	dB
		f_{EXTLO} = 5.625GHz to 6.75GHz Over PVT	-	12	-	dB
RF Input Return Loss	RL_{RF_IN}	f_{RF} = 26.5GHz to 29.5GHz Over PVT	-	8.5	-	dB
Maximum Small Signal Conversion Gain	G_{MAX}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	21.5 (22.4) [1]	-	dB
Gain Variation Over IF Range	$G_{VAR\_\Delta IF}$	f_{RF} = 28GHz f_{EXTLO} = 12GHz to 12.75GHz f_{IF} = 2.5GHz to 4GHz Referenced to f_{IF} = 3GHz	-	2	-	dB
Gain Flatness	G_{FLAT}	Over any 100MHz bandwidth	-	0.2	-	dB
		Over any 1GHz bandwidth	-	0.7	-	dB
		Over any 3GHz bandwidth	-	0.9	-	dB
IF DSA Adjustment Range	G_{IFDSA_RANGE}	-	-	20	-	dB
IF DSA Step Resolution	G_{IFDSA_STEP}	LSB	-	0.5	-	dB
IF DSA Gain Settling Time	t_{IFDSA_ST}	Any 1dB step in the 0dB to 15dB range. 50% of CSB to 10% / 90% RF	-	30	-	ns
RF VGA Adjustment Range	G_{RFDSA_RANGE}	-	-	10	-	dB
RF VGA Step Resolution	G_{RFDSA_STEP}	LSB	-	1.0	-	dB
RF DSA Gain Settling Time	t_{RFDSA_ST}	Any 1dB step in the 0dB to 15dB range. 50% of CSB to 10% / 90% RF	-	30	-	ns
Noise Figure (SSB, No Blockers Present)	NF_{MAX_G}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	6 (4.9) [1]	-	dB

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input Third Order Intercept Point	IIP3	IF DSA setting = 0dB RF VGA setting = Max Gain P_{RF} = -30dBm / tone 100MHz Tone Spacing Over PVT	-	-7.8 (-8.9) [1]	-	dBm
Input 1dB Compression Point	IP1dB	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	-15.2 (-16.5) [1]	-	dBm
Image Rejection	IRR	f_{RF} = 26.5GHz to 29.5GHz Uncalibrated Over PVT	-	35 (33.6) [1]	-	dBc

1. For the separate RX2 path.

3.4.9 3GHz IF/26GHz RF (Band L6) – TX

See the F5701 EVB circuit (Figure 404 and Figure 405). Specifications apply when operated in TX Mode with V_{DD} = +2.5V, V_{DDPA} = +2.5V, T_A = +25°C, f_{RF} = 26GHz, f_{EXTLO} = 11.5GHz, f_{IF} = 3GHz, LO Multiplier Factor = 2, LO Injection = Low Side, P_{EXTLO} = -10dBm, RESETB = HIGH, Z_{RF} = Z_{LO} = Z_{IF} = 50Ω single ended, maximum gain setting (TX IF DSA = 0dB, and TX RF VGA set to maximum gain), and P_{OUT} = 0dBm/tone, unless stated otherwise. EVB trace and connector losses are de-embedded.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Recommended RF Frequency Range	f_{RF}	-	24.25	26	27.5	GHz
Recommended IF Frequency Range	f_{IF}	-	2.5	3	4	GHz
IF Input Return Loss	RL_{IFIN}	f_{IF} = 2.5GHz to 4GHz Over PVT	-	13.6	-	dB
External LO Input Return Loss	RL_{EXTLO}	f_{EXTLO} = 10.125GHz to 12.5GHz Over PVT	-	12	-	dB
		f_{EXTLO} = 5.0625GHz to 6.25GHz Over PVT	-	12	-	dB
RF Output Return Loss	RL_{RFOUT}	f_{RF} = 24.25GHz to 27.5GHz Over PVT	-	5.5 (6) [1]	-	dB
Maximum Small Signal Conversion Gain	G_{MAX}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	33.4 (33.5) [1]	-	dB
IF DSA Adjustment Range	G_{IFDSA_RANGE}	-	-	20	-	dB
IF DSA Step Resolution	G_{IFDSA_STEP}	LSB	-	0.5	-	dB
Phase Shift Relative to the 0dB IF DSA Attenuation State	$\Phi_{IFDSA\_\Delta MID1}$	IF DSA 5dB Attenuation	-	± 1.25	-	deg
	$\Phi_{IFDSA\_\Delta MID2}$	IF DSA 10dB Attenuation	-	± 2.5	-	deg
	$\Phi_{IFDSA\_\Delta MAX}$	IF DSA 20dB Attenuation	-	± 3.75	-	deg

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
IF DSA Gain Settling Time	t_{IFDSA_ST}	Any 1dB step in the 0dB to 15dB range. 50% of CSB to 10% / 90% RF	-	30	-	ns
RF VGA Adjustment Range	G_{RFDSA_RANGE}	-	-	10	-	dB
RF VGA Step Resolution	G_{RFDSA_STEP}	LSB	-	1.0	-	dB
RF VGA Gain Settling Time	t_{RFVGA_ST}	Any 1dB step in the 0dB to 10dB range. 50% of CSB to 10% / 90% RF	-	30	-	ns
Noise Figure	NF_{MAX_G}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	9.8 (9.8) [1]	-	dB
Output Third Order Intercept Point	OIP3	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	29.4 (30.3) [1]	-	dBm
Output 1dB Compression Point	OP1dB	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	20.4 (21.6) [1]	-	dBm
LO Leakage	LOL	f_{RF} = 24.25GHz to 27.5GHz Uncalibrated RF Output Power = 8dBm	-	-41 (-41) [1]	-	dBc
		f_{RF} = 24.25GHz to 27.5GHz Calibrated RF Output Power = 8dBm	-	-49.8 (-50.7) [1]	-	
TX EVM	EVM_{TX}	RF Output Power = 8dBm (9dBm with V_{DDPA} = +3.3V)	-	1.0 (0.8) [1]	-	%
TX-RX Isolation	ISO_{TX-RX}	-	-	35	-	dB
M x N Spurious Rejection	M x N	f_{RF} = 21GHz to 32.5GHz RF Output Power = 8dBm	-	35	-	dBc
		All other bands	-	40	-	dBc
Sideband Suppression	SBS	f_{RF} = 24.25GHz to 27.5GHz Uncalibrated RF Output Power = 8dBm	-	51.4 (47.2) [1]	-	dBc

1. For V_{DDPA} = +3.3V.

3.4.10 3GHz IF/26GHz RF (Band L6) – RX

See the F5701 EVB circuit (Figure 404 and Figure 405). Specifications apply when operated in RX Mode with V_{DD} = +2.5V, V_{DDPA} = +2.5V, T_A = +25°C, f_{RF} = 26GHz, f_{EXTLO} = 11.5GHz, f_{IF} = 3GHz, LO Multiplier Factor = 2, LO Injection = Low Side, P_{EXTLO} = -10dBm, RESETB = HIGH, $Z_{RF} = Z_{LO} = Z_{IF}$ = 50Ω single ended , maximum gain setting (RX IF DSA = 0dB, and RX RF VGA set to maximum gain), P_{RF} = -30dBm, P_{IF_OUT} = -5 dBm/tone, and TBD tone spacing, unless stated otherwise. EVB trace and connector losses are de-embedded.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Recommended RF Frequency Range	f_{RF}	-	24.25	26	27.5	GHz
Recommended IF Frequency Range	f_{IF}	-	2.5	3	4	GHz
IF Output Return Loss	RL_{IFOUT}	f_{IF} = 2.5GHz to 4GHz Over PVT	-	13	-	dB
External LO Input Return Loss	RL_{EXTLO}	f_{EXTLO} = 10.125GHz to 12.5GHz Over PVT	-	12	-	dB
		f_{EXTLO} = 5.0625GHz to 6.25GHz Over PVT	-	12	-	dB
RF Input Return Loss	RL_{RF_IN}	f_{RF} = 24.25GHz to 27.5GHz Over PVT	-	13	-	dB
Maximum Small Signal Conversion Gain	G_{MAX}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	21 (22) [1]	-	dB
Gain Variation Over IF Range	$G_{VAR\_\Delta IF}$	f_{RF} = 26GHz f_{EXTLO} = 11 GHz to 11.75GHz f_{IF} = 2.5GHz to 4GHz Referenced to f_{IF} = 3GHz	-	1.9	-	dB
Gain Flatness	G_{FLAT}	Over any 100MHz bandwidth	-	0.1	-	dB
		Over any 1GHz bandwidth	-	0.9	-	dB
		Over any 3GHz bandwidth	-	1.2	-	dB
IF DSA Adjustment Range	G_{IFDSA_RANGE}	-	-	20	-	dB
IF DSA Step Resolution	G_{IFDSA_STEP}	LSB	-	0.5	-	dB
IF DSA Gain Settling Time	t_{IFDSA_ST}	Any 1dB step in the 0dB to 15dB range. 50% of CSB to 10% / 90% RF	-	30	-	ns
RF VGA Adjustment Range	G_{RFDSA_RANGE}	-	-	10	-	dB
RF VGA Step Resolution	G_{RFDSA_STEP}	LSB	-	1.0	-	dB
RF DSA Gain Settling Time	t_{RFDSA_ST}	Any 1dB step in the 0dB to 15dB range. 50% of CSB to 10% / 90% RF	-	30	-	ns
Noise Figure (SSB, No Blockers Present)	NF_{MAX_G}	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	6.6 (5.4) [1]	-	dB

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input Third Order Intercept Point	IIP3	IF DSA setting = 0dB RF VGA setting = Max Gain P_{RF} = -30dBm / tone 100MHz Tone Spacing Over PVT	-	-7.7 (-7.4) [1]	-	dBm
Input 1dB Compression Point	IP1dB	IF DSA setting = 0dB RF VGA setting = Max Gain Over PVT	-	-15.2 (-15.3) [1]	-	dBm
Image Rejection	IRR	f_{RF} = 24.25GHz to 27.5GHz Uncalibrated Over PVT	-	42.3 (38.4) [1]	-	dBc

1. For the separate RX2 path.

4. Typical Performance Graphs

Unless otherwise noted, the following conditions apply for the typical performance characteristics on the following pages:

- V_{DD} = V_{DDPA} = +2.5V typical
- Z_{LO} = Z_{RF} = Z_{IF} = 50Ω single-ended
- RESETB = HIGH
- 100MHz tone spacing
- Gain setting = maximum gain
- T_A = 25°C ambient
- Evaluation Board traces and connector losses are de-embedded

4.1 7GHz IF/28GHz RF (Band H8)

4.1.1 TX Performance

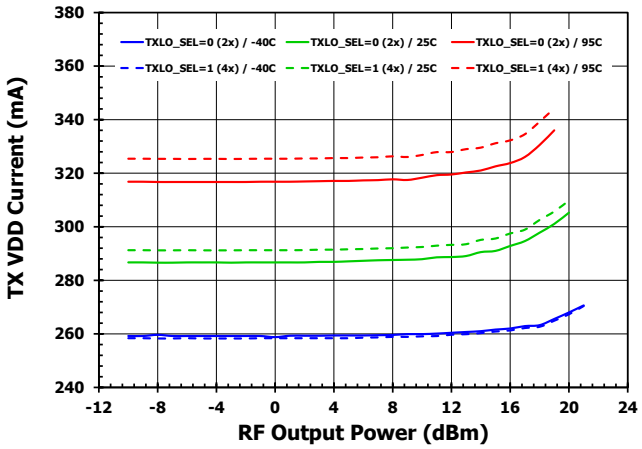

Figure 3. TX VDD Current

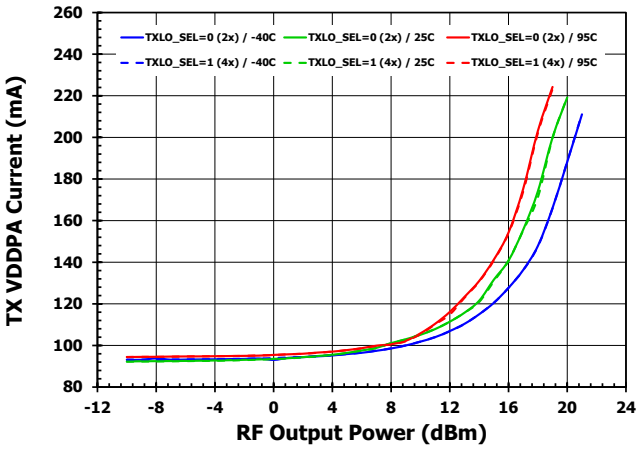

Figure 4. TX VDDPA Current

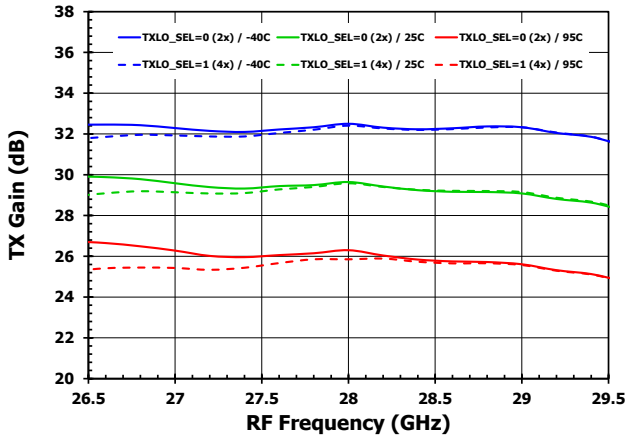

Figure 5. TX Gain

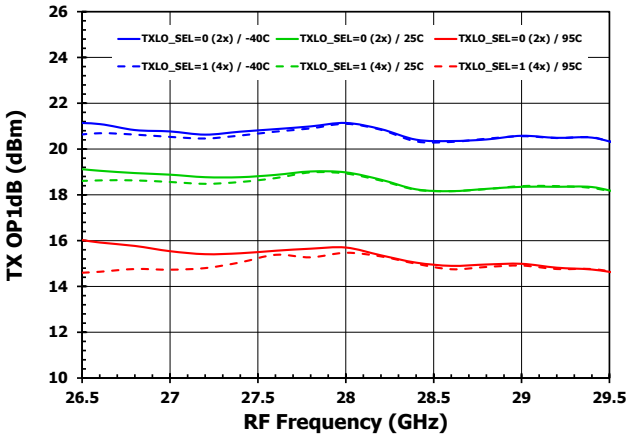

Figure 6. TX OP1dB

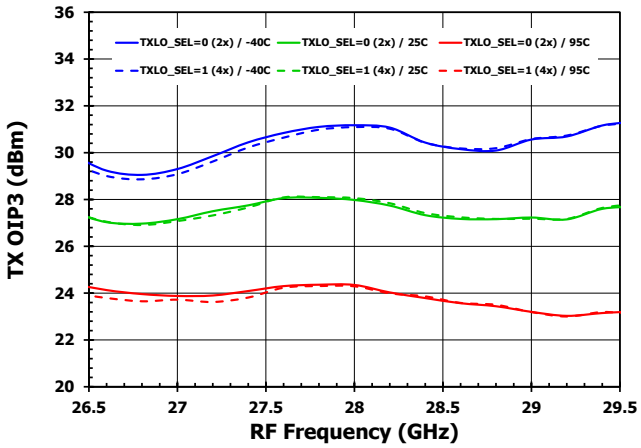

Figure 7. TX OIP3

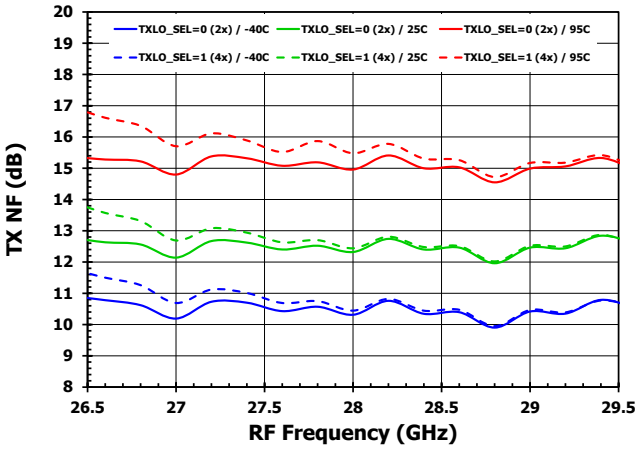

Figure 8. TX NF

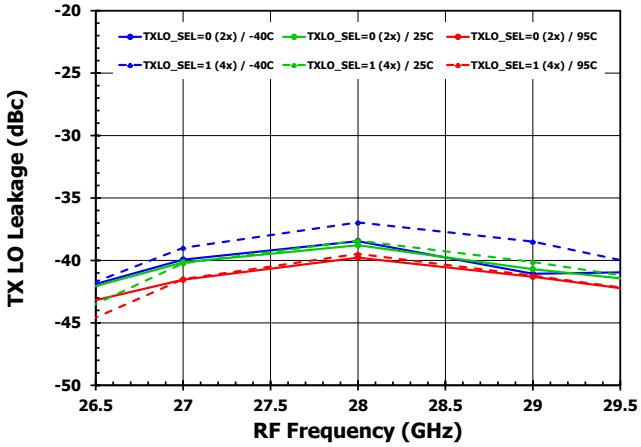

Figure 9. TX LO Leakage (uncalibrated)

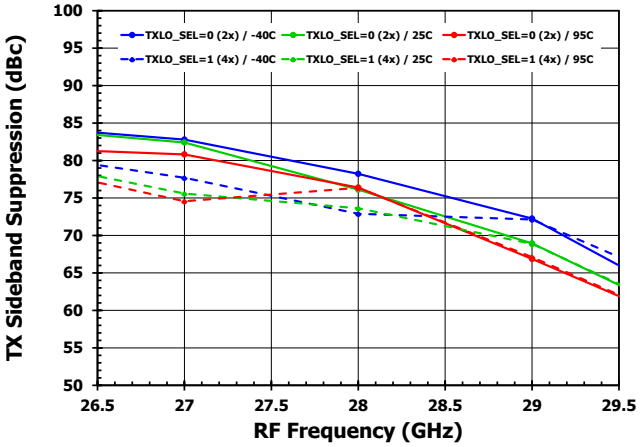

Figure 10. TX Sideband Suppression (uncalibrated)

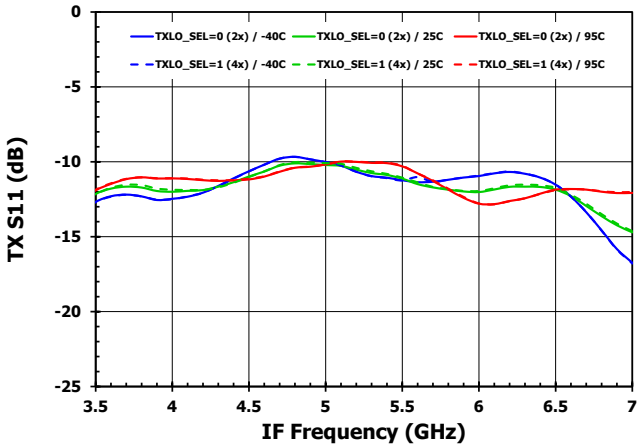

Figure 11. TX S11

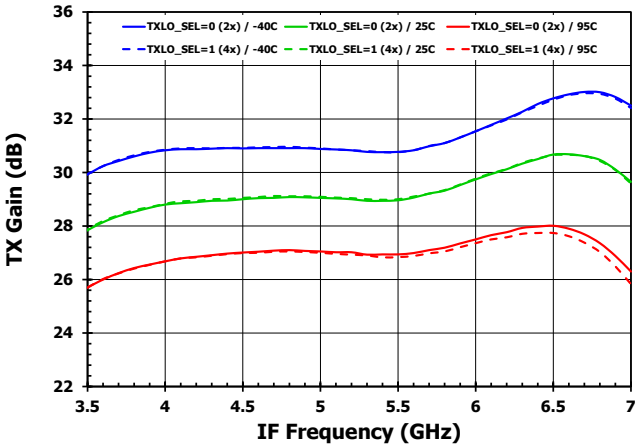

Figure 12. TX Gain vs IF

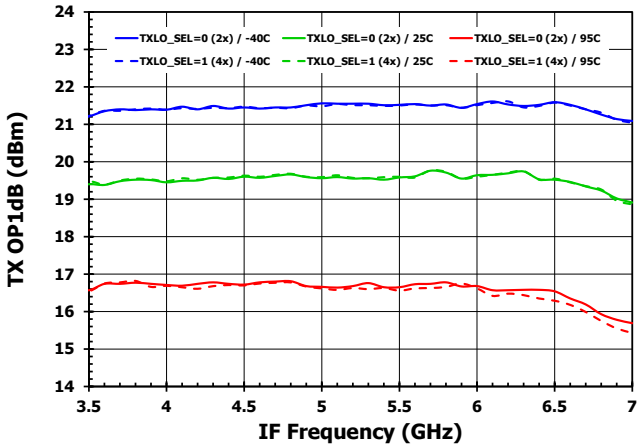

Figure 13. TX OP1dB vs IF

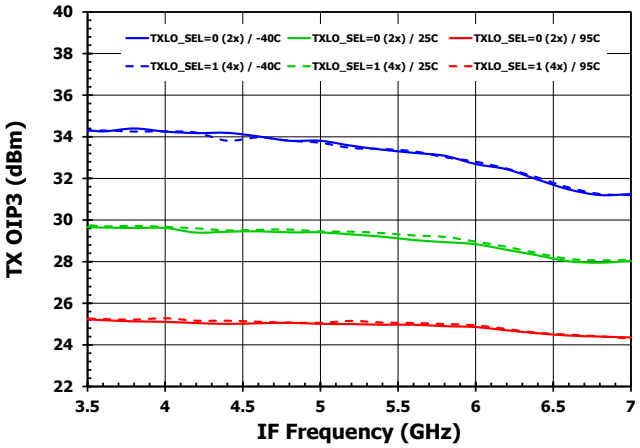

Figure 14. TX OIP3 vs IF

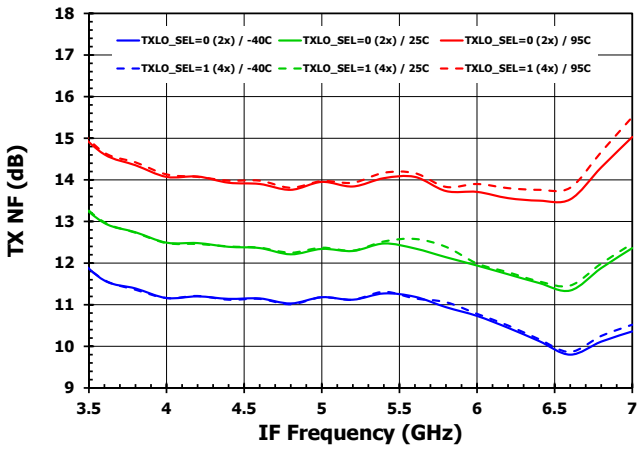

Figure 15. TX NF vs IF

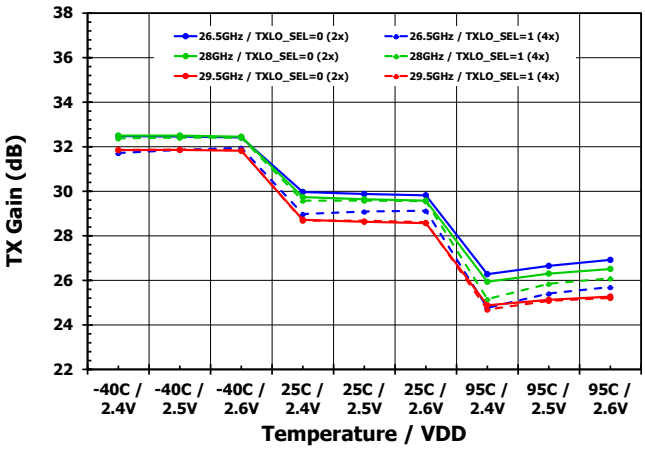

Figure 16. TX Gain over VT

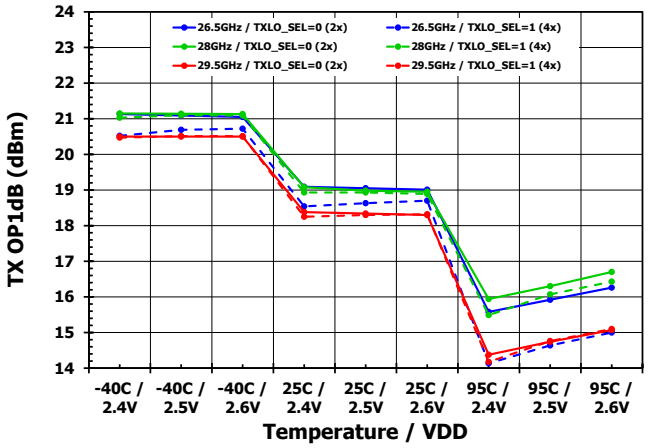

Figure 17. TX OP1dB over VT

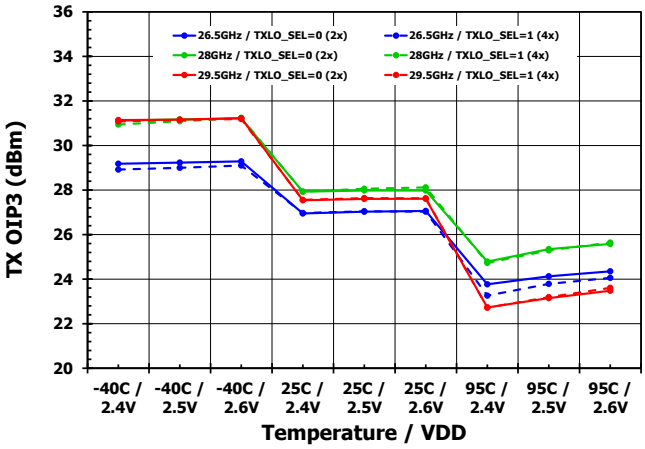

Figure 18. TX OIP3 over VT

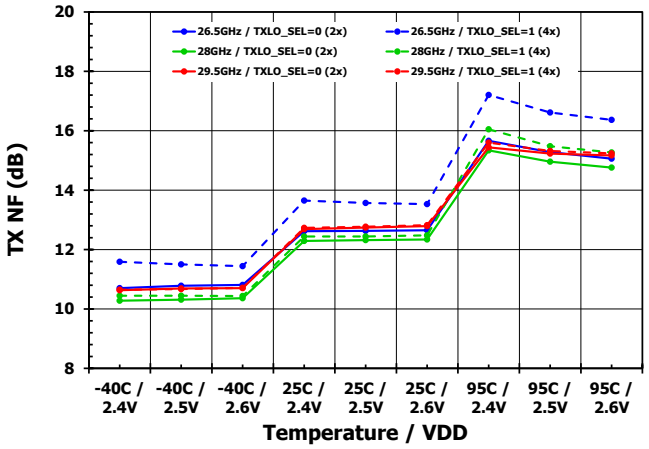

Figure 19. TX NF over VT

4.1.2 TX Performance – V_{DDPA} = 3.3V

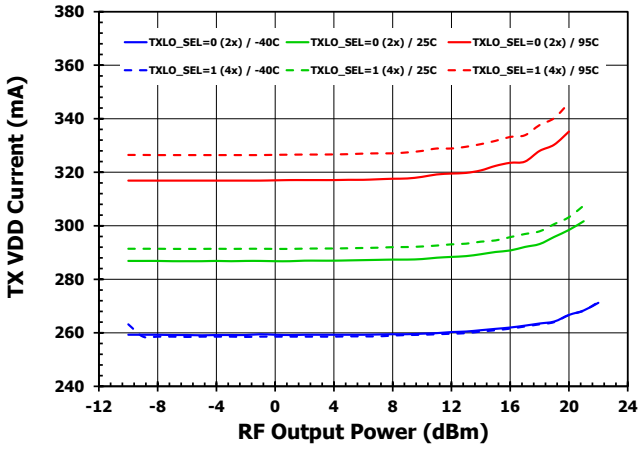

Figure 20. TX VDD Current

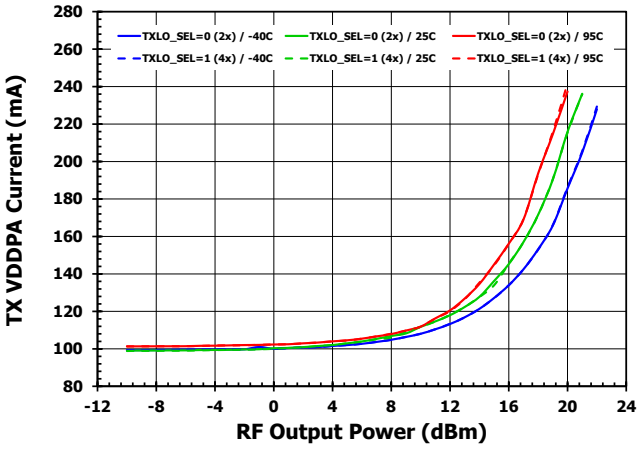

Figure 21. TX VDDPA Current

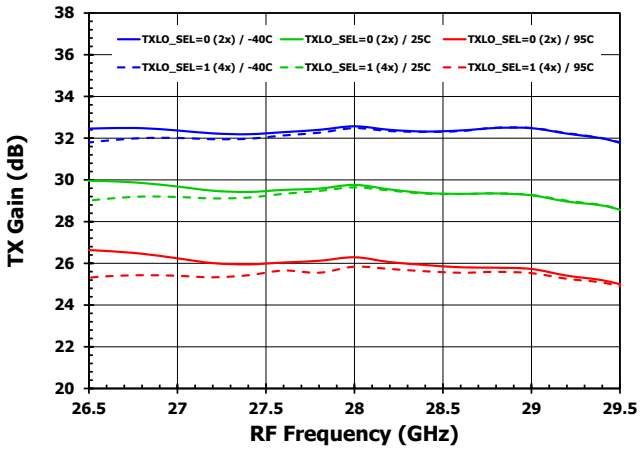

Figure 22. TX Gain

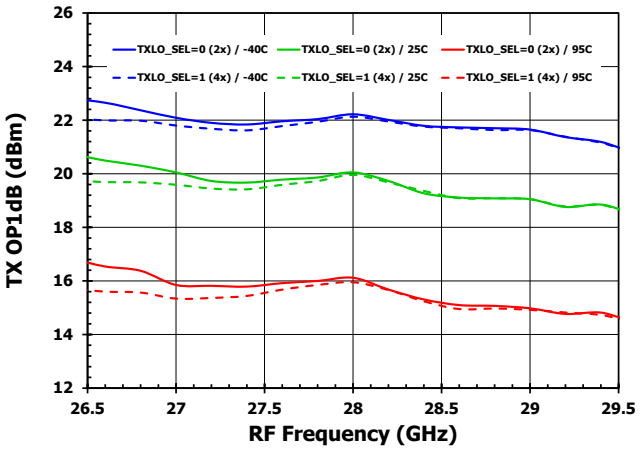

Figure 23. TX OP1dB

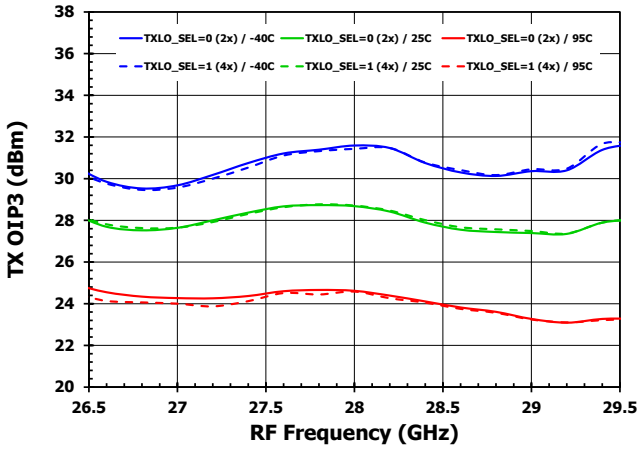

Figure 24. TX OIP3

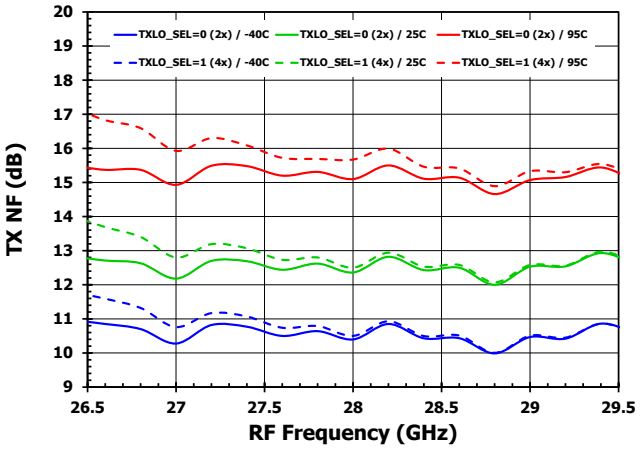

Figure 25. TX NF

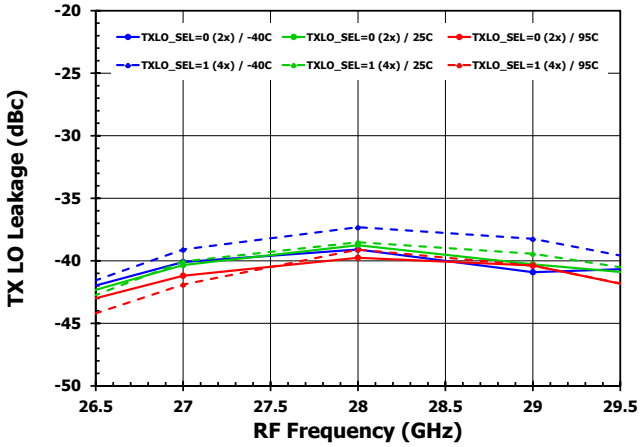

Figure 26. TX LO Leakage (uncalibrated)

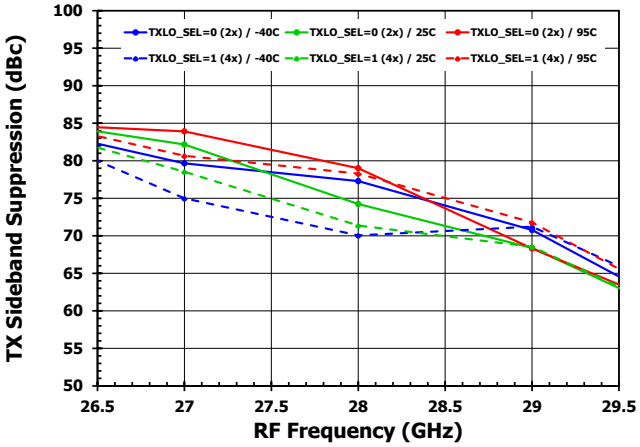

Figure 27. TX Sideband Suppression (uncalibrated)

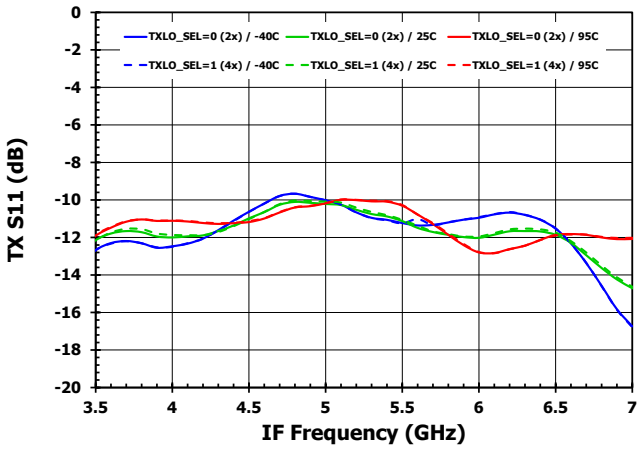

Figure 28. TX S11

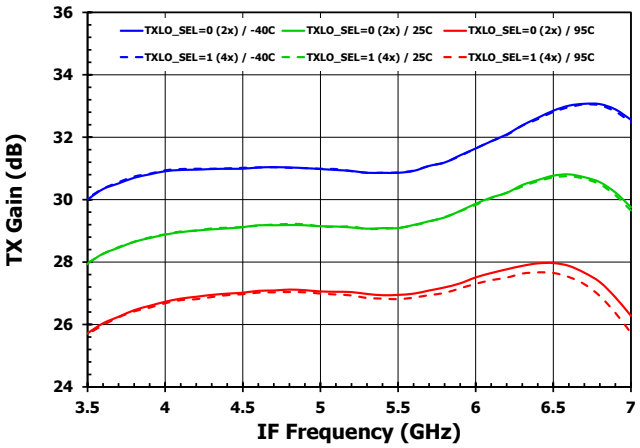

Figure 29. TX Gain vs IF

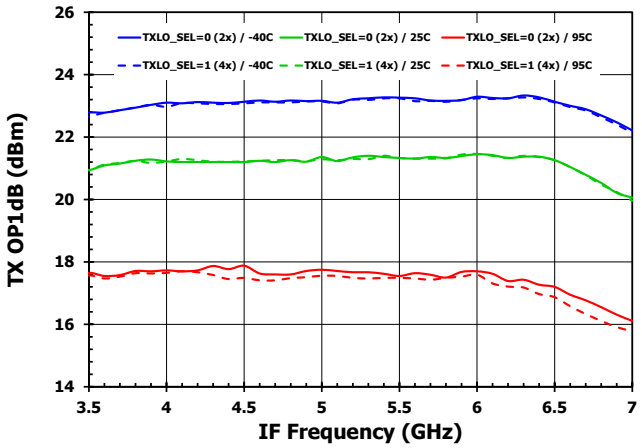

Figure 30. TX OP1dB vs IF

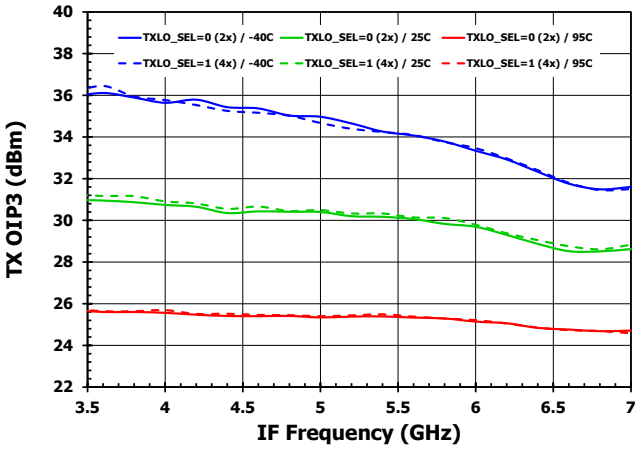

Figure 31. TX OIP3 vs IF

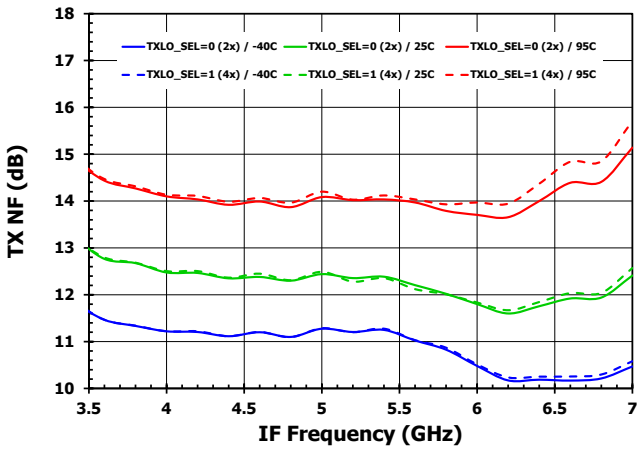

Figure 32. TX NF vs IF

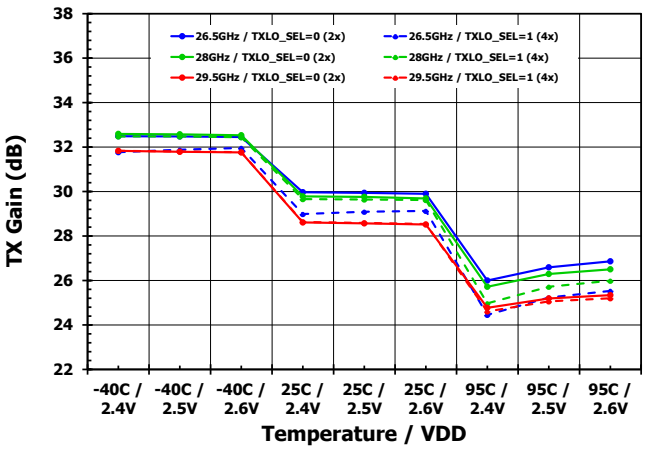

Figure 33. TX Gain over VT

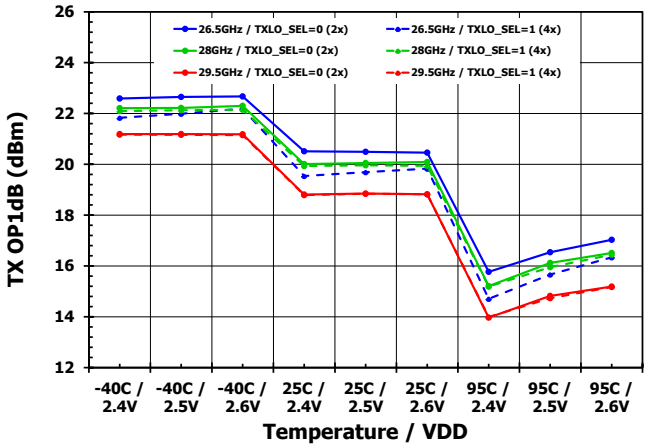

Figure 34. TX OP1dB over VT

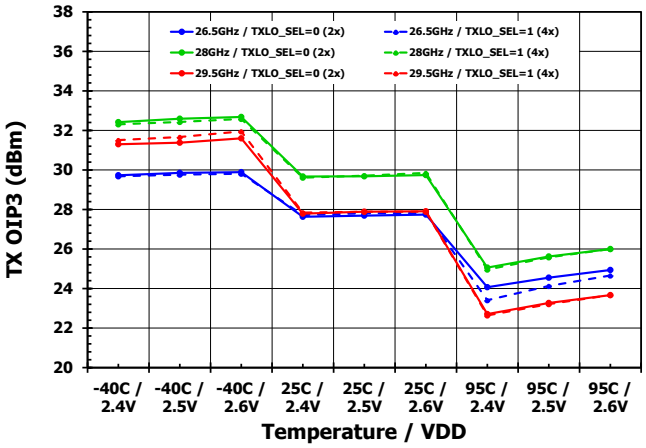

Figure 35. TX OIP3 over VT

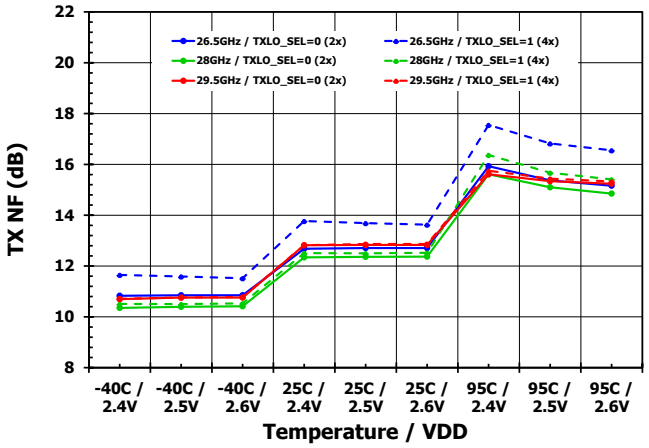

Figure 36. TX NF over VT

4.1.3 RX Performance

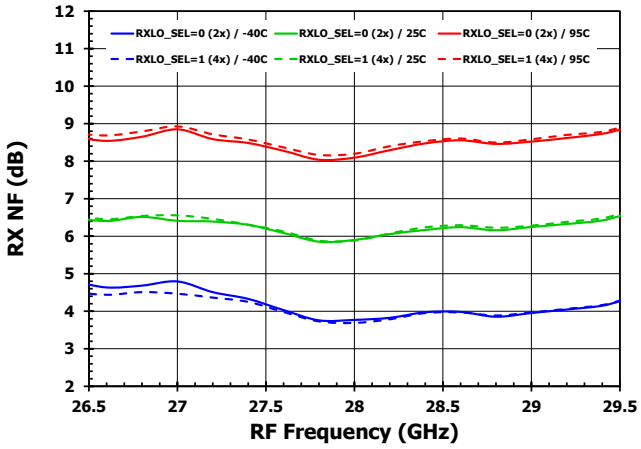

Figure 37. RX NF

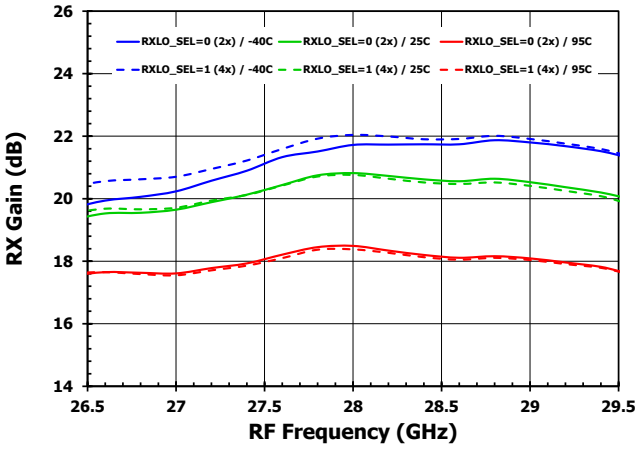

Figure 38. RX Gain

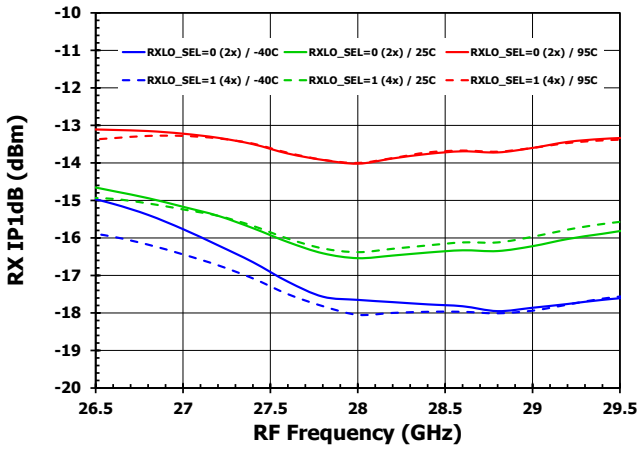

Figure 39. RX IP1dB

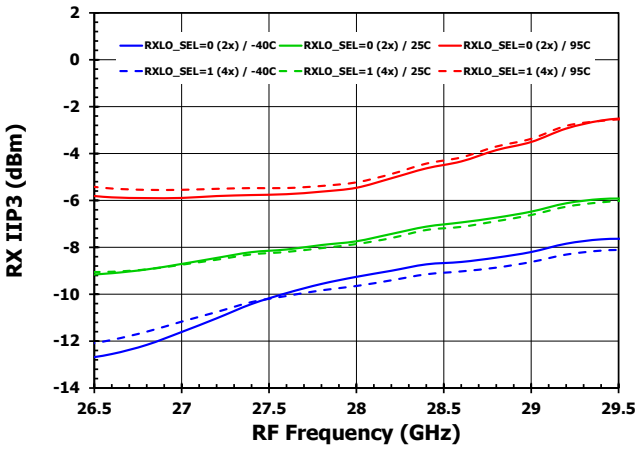

Figure 40. RX IIP3

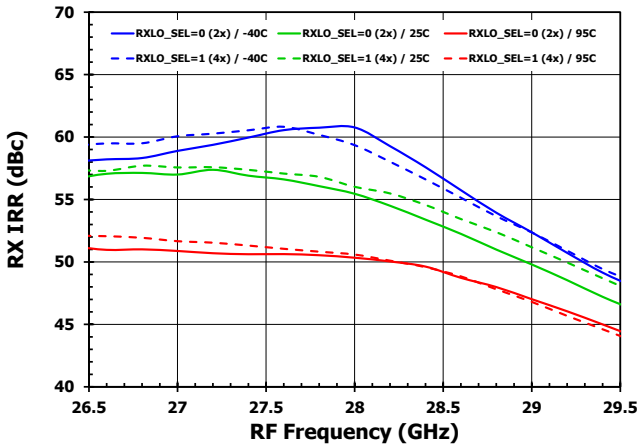

Figure 41. RX Image Rejection Ratio (uncalibrated)

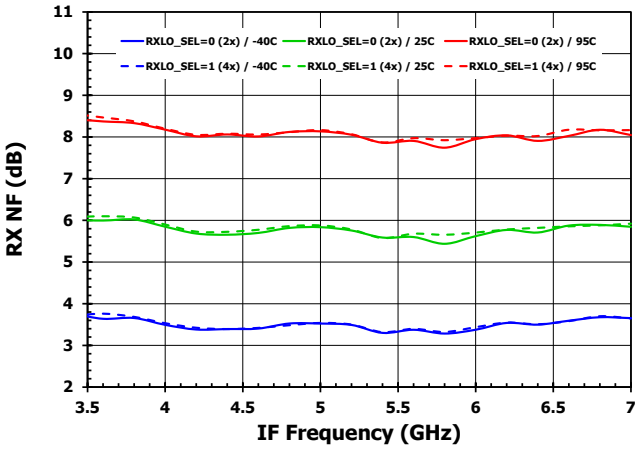

Figure 42. RX NF vs IF

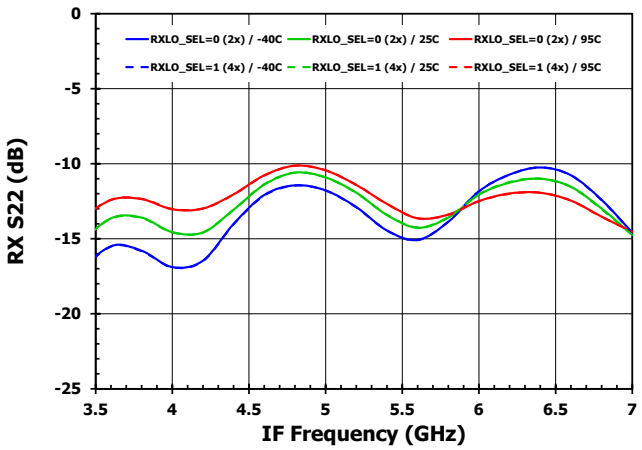

Figure 43. RX S22 vs IF

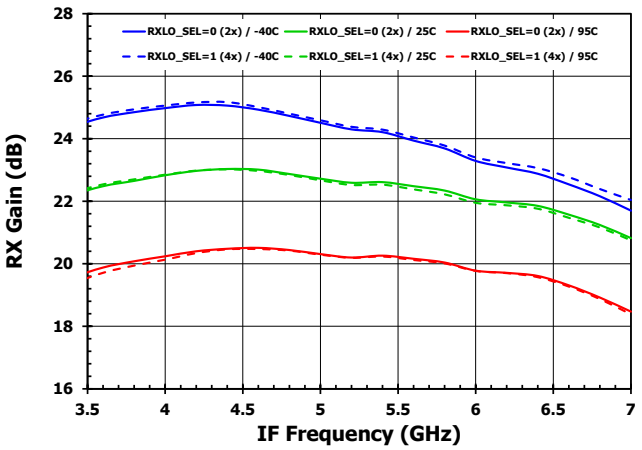

Figure 44. RX Gain vs IF

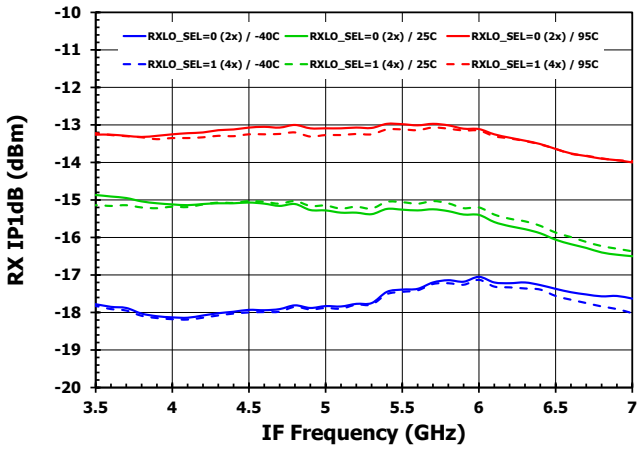

Figure 45. RX IP1dB vs IF

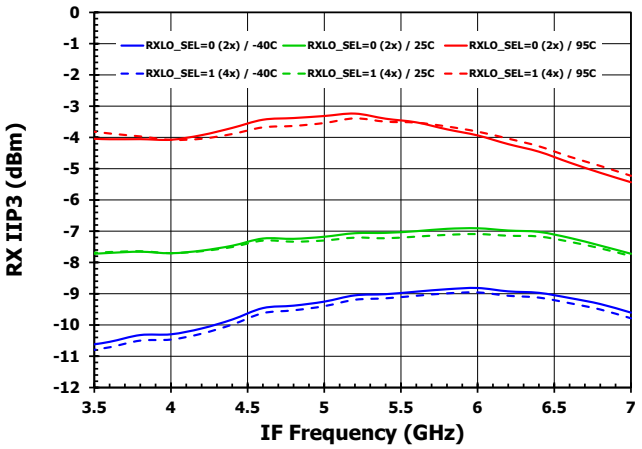

Figure 46. RX IIP3 vs IF

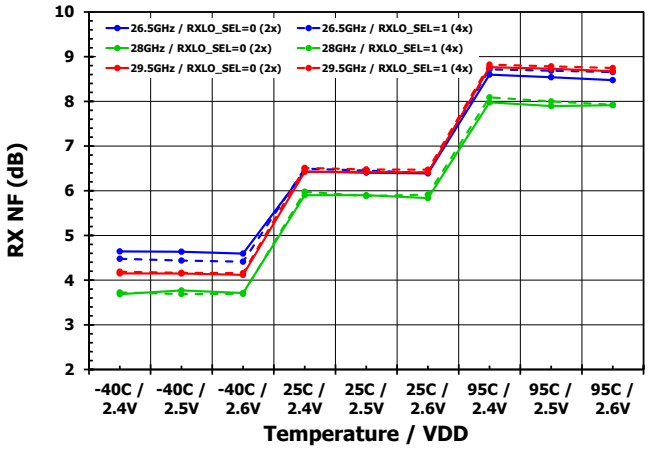

Figure 47. RX NF over VT

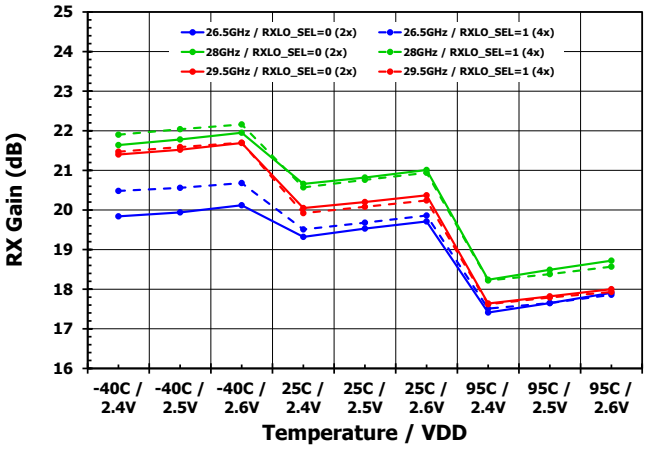

Figure 48. RX Gain over VT

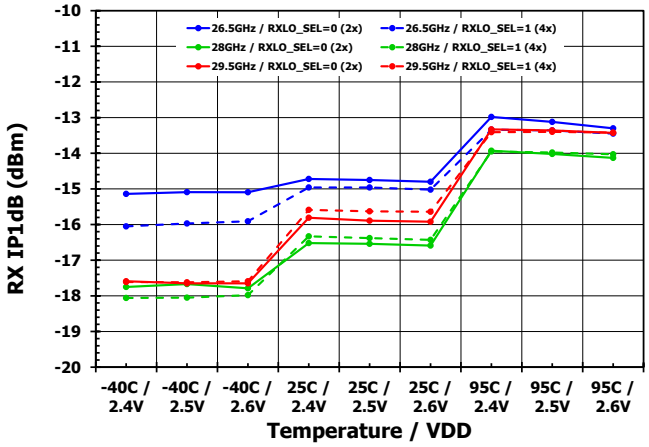

Figure 49. RX IP1dB over VT

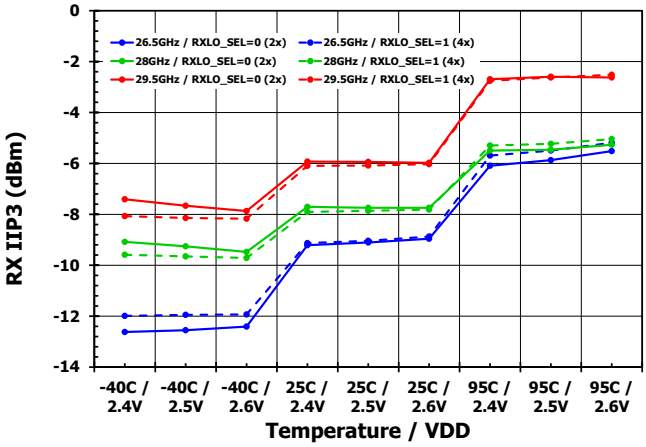

Figure 50. RX IIP3 over VT

4.1.4 RX Performance – RX2 Path

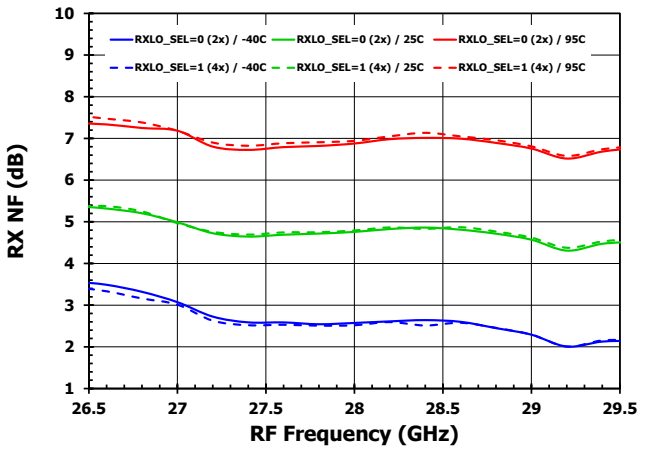

Figure 51. RX2 NF

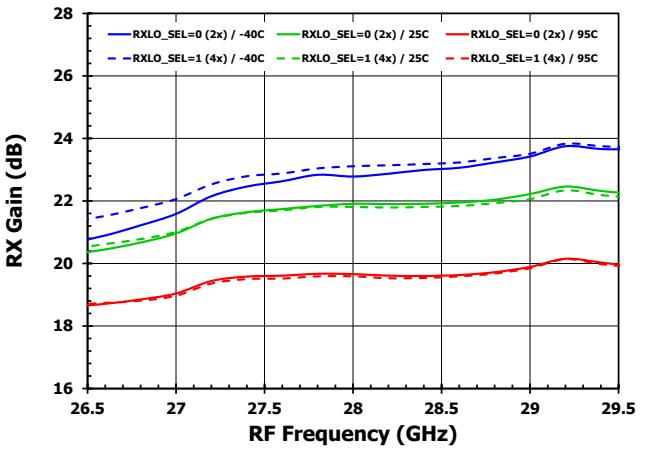

Figure 52. RX2 Gain

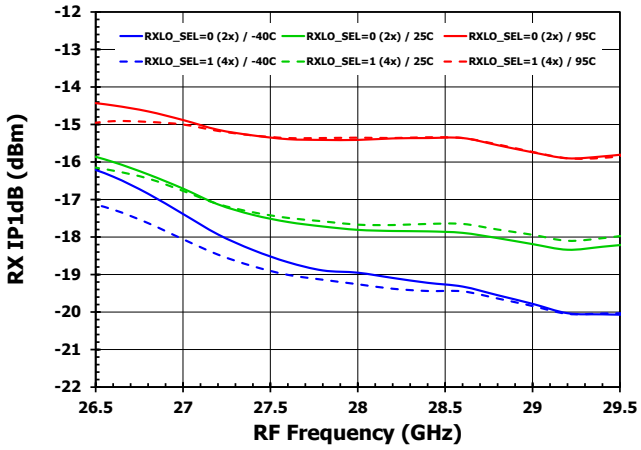

Figure 53. RX2 IP1dB

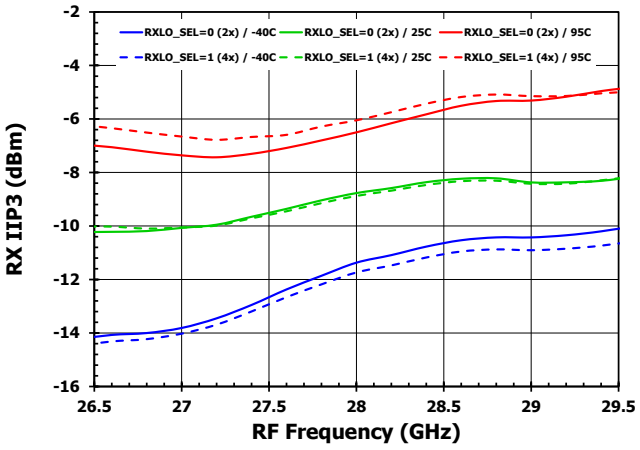

Figure 54. RX2 IIP3

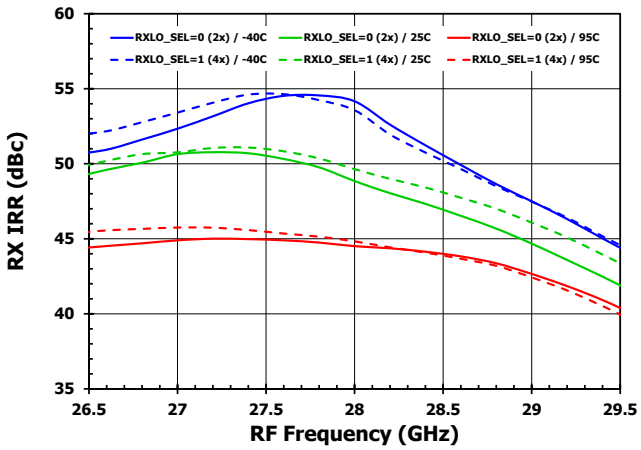

Figure 55. RX2 Image Rejection Ratio (uncalibrated)

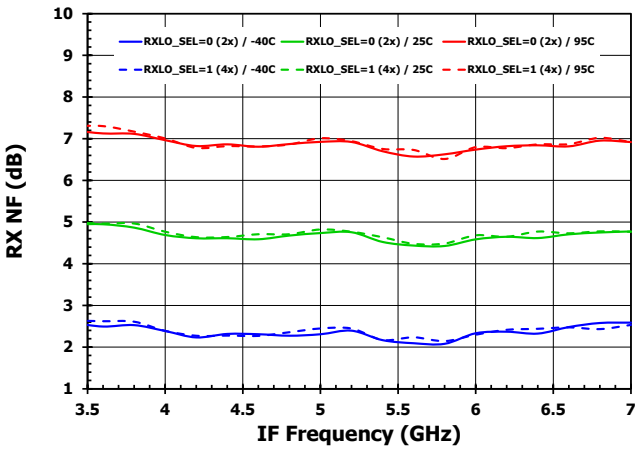

Figure 56. RX2 NF vs IF

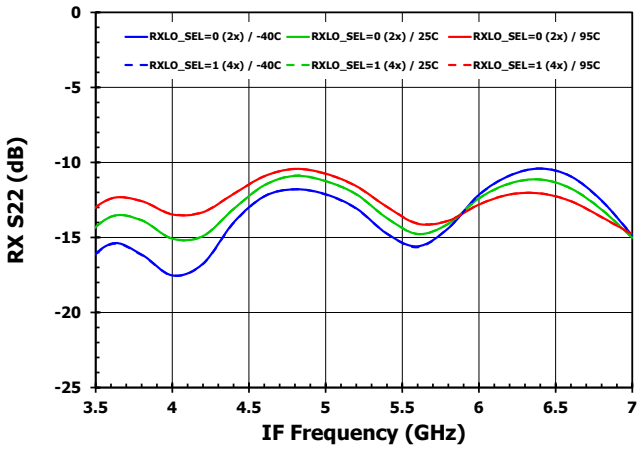

Figure 57. RX2 S22 vs IF

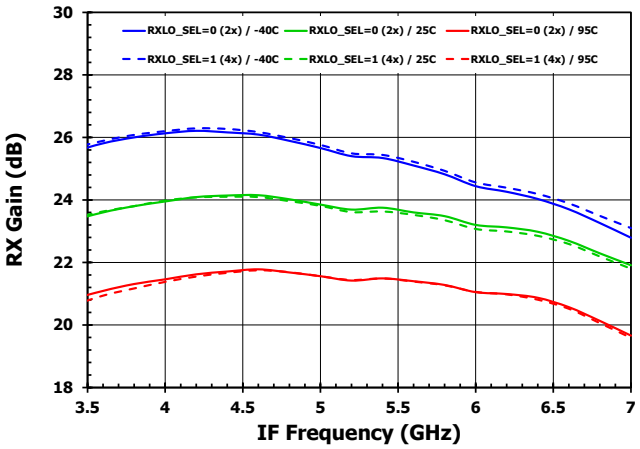

Figure 58. RX2 Gain vs IF

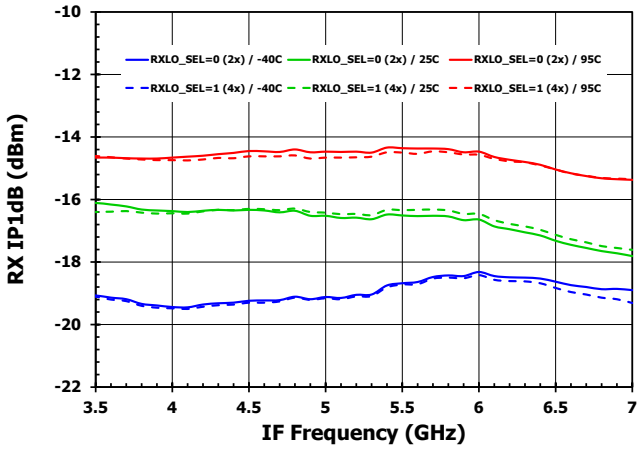

Figure 59. RX2 IP1dB vs IF

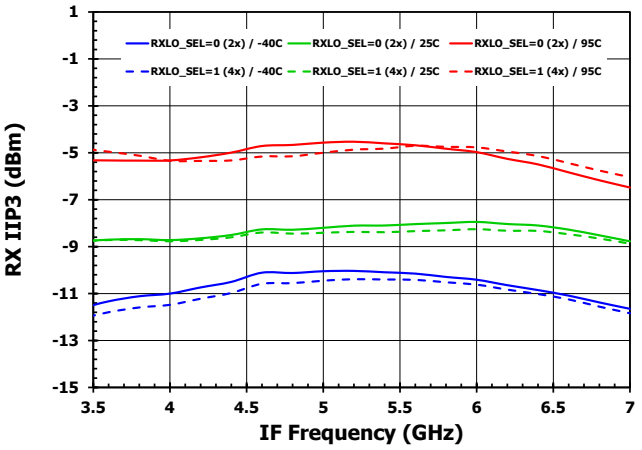

Figure 60. RX2 IIP3 vs IF

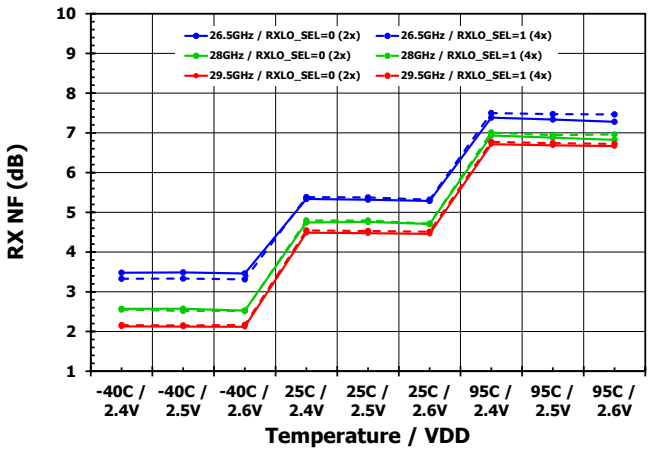

Figure 61. RX2 NF over VT

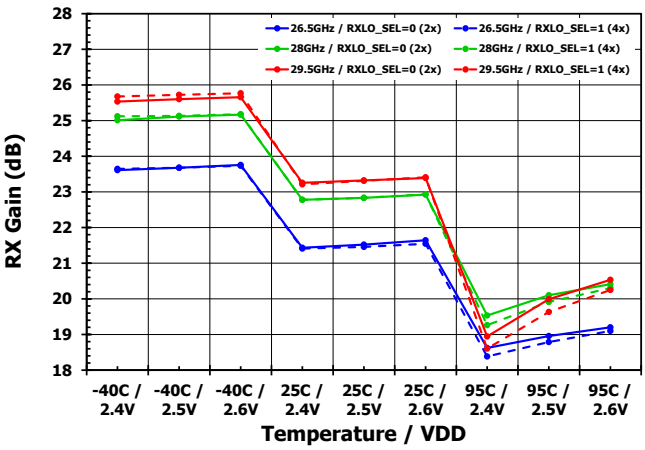

Figure 62. RX2 Gain over VT

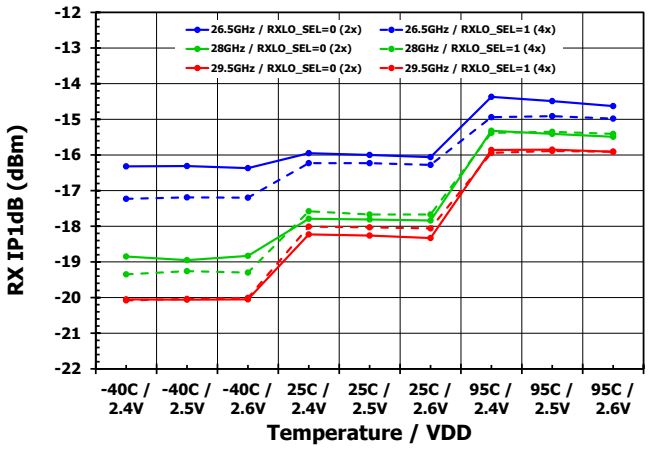

Figure 63. RX2 IP1dB over VT

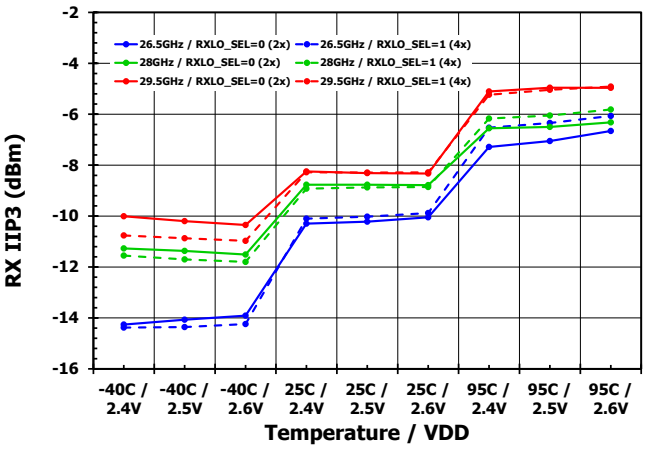

Figure 64. RX2 IIP3 over VT

4.2 7GHz IF/26GHz RF (Band H6)

4.2.1 TX Performance

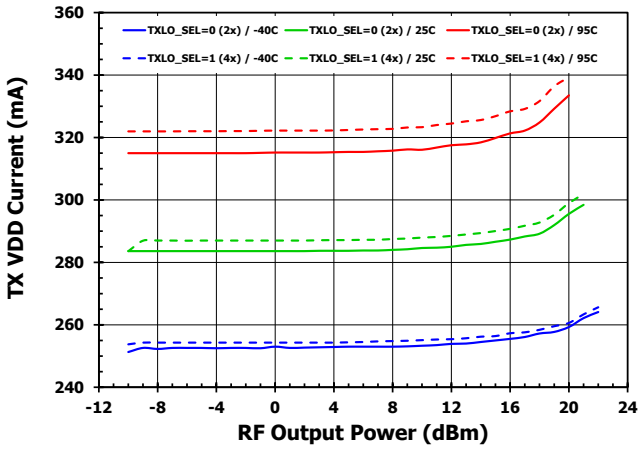

Figure 65. TX VDD Current

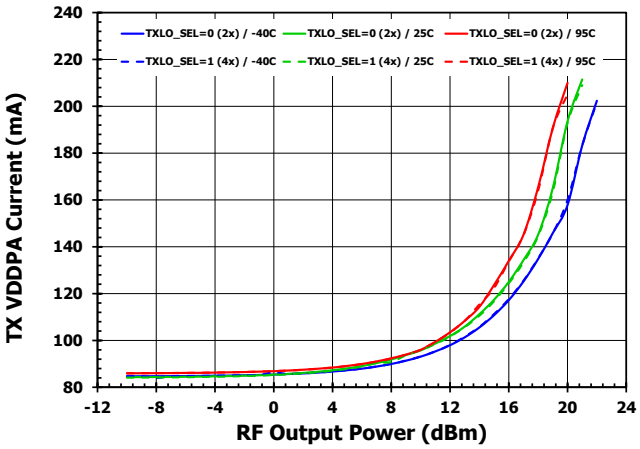

Figure 66. TX VDDPA Current

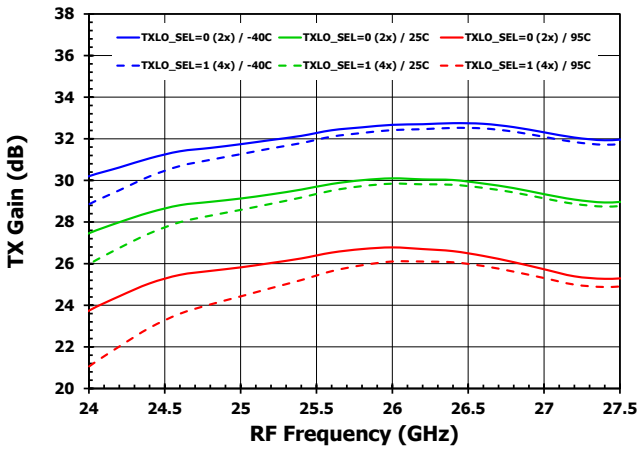

Figure 67. TX Gain

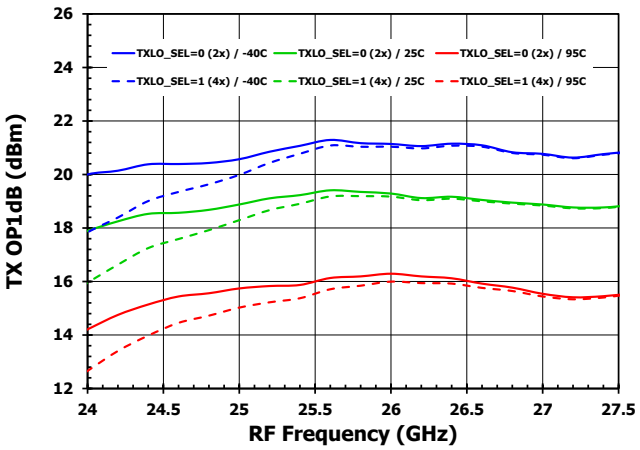

Figure 68. TX OP1dB

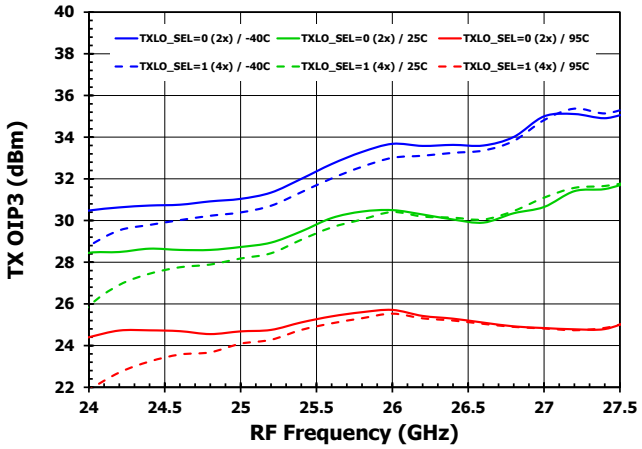

Figure 69. TX OIP3

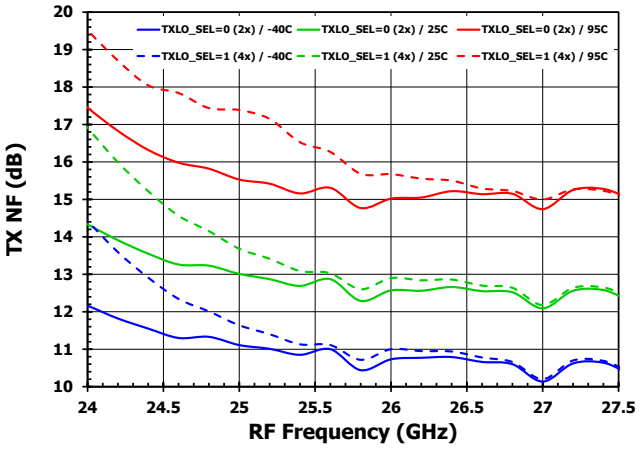

Figure 70. TX NF

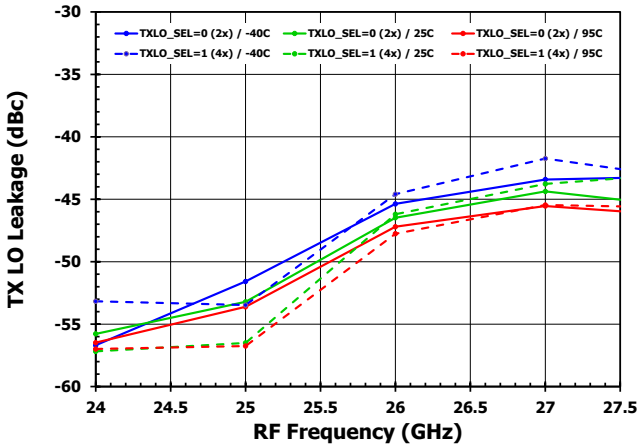

Figure 71. TX LO Leakage (uncalibrated)

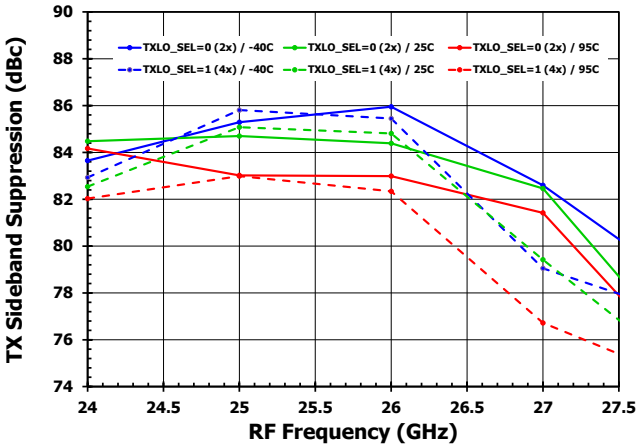

Figure 72. TX Sideband Suppression (uncalibrated)

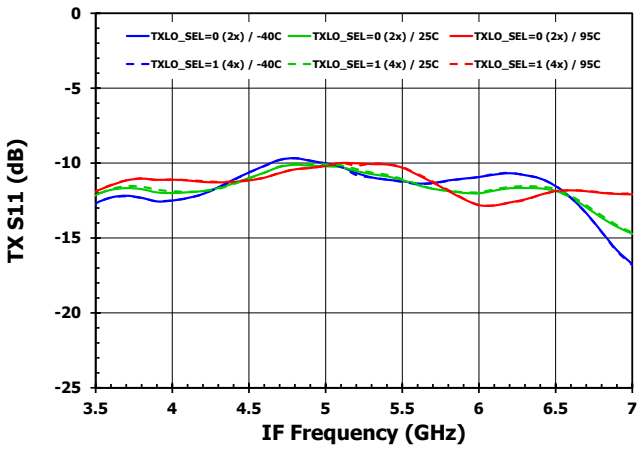

Figure 73. TX S11

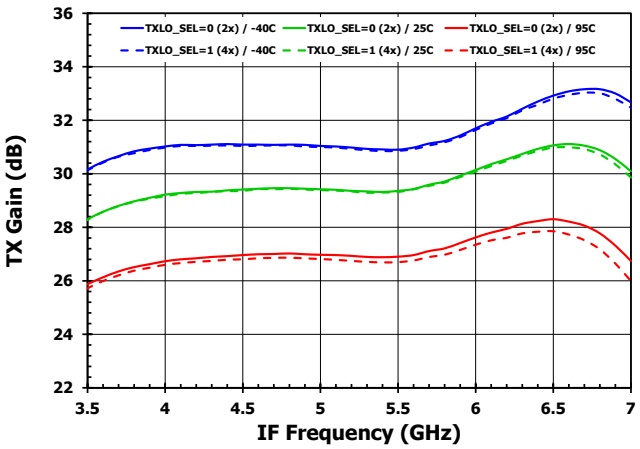

Figure 74. TX Gain vs IF

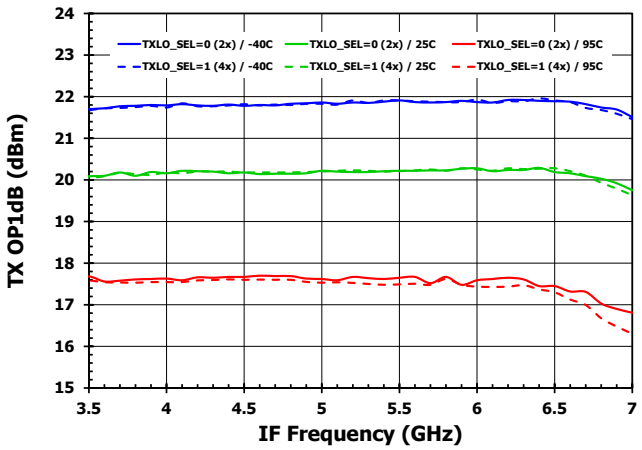

Figure 75. TX OP1dB vs IF

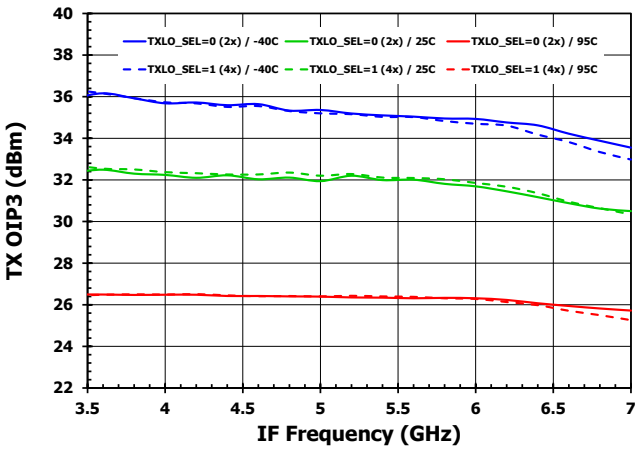

Figure 76. TX OIP3 vs IF

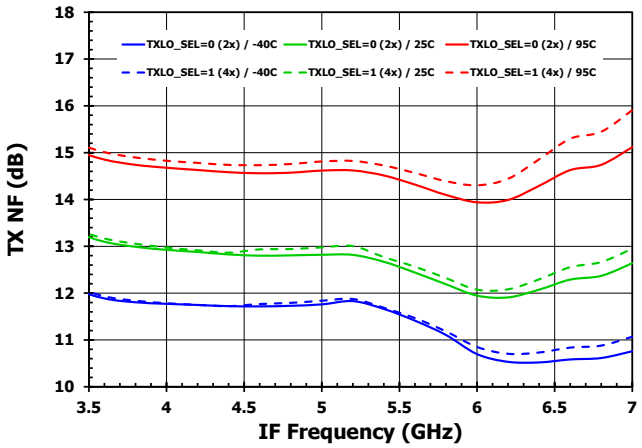

Figure 77. TX NF vs IF

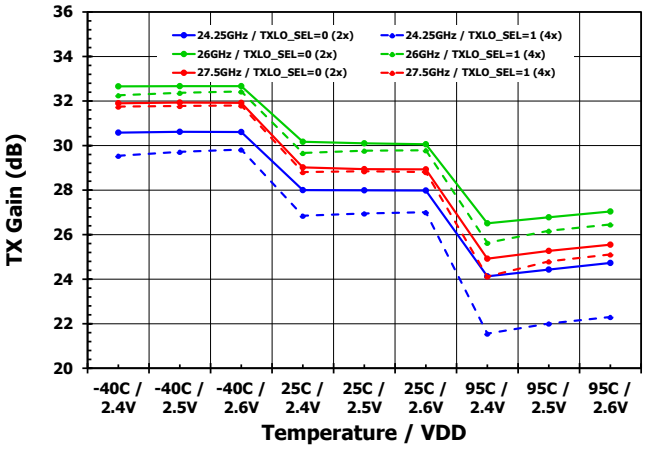

Figure 78. TX Gain over VT

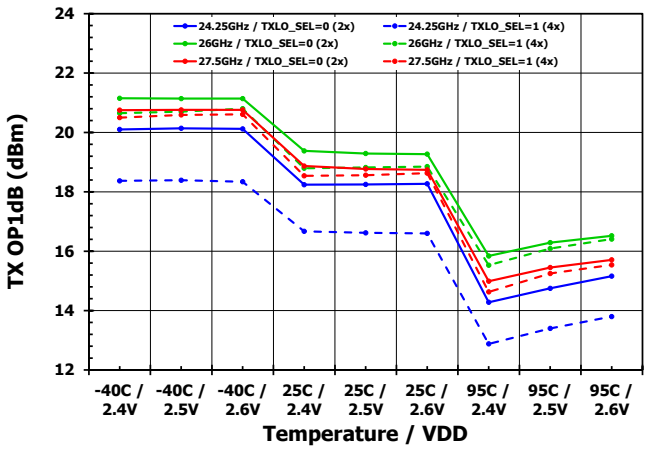

Figure 79. TX OP1dB over VT

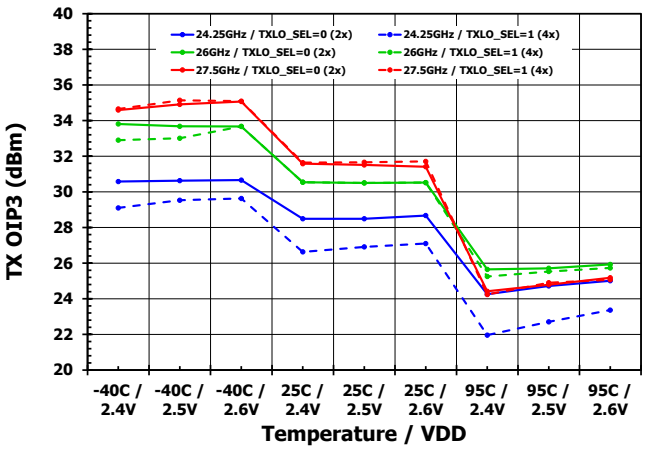

Figure 80. TX OIP3 over VT

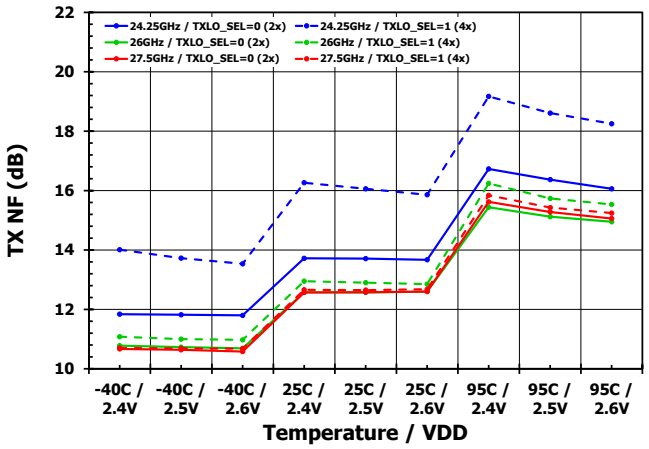

Figure 81. TX NF over VT

4.2.2 TX Performance – V_{DDPA} = 3.3V

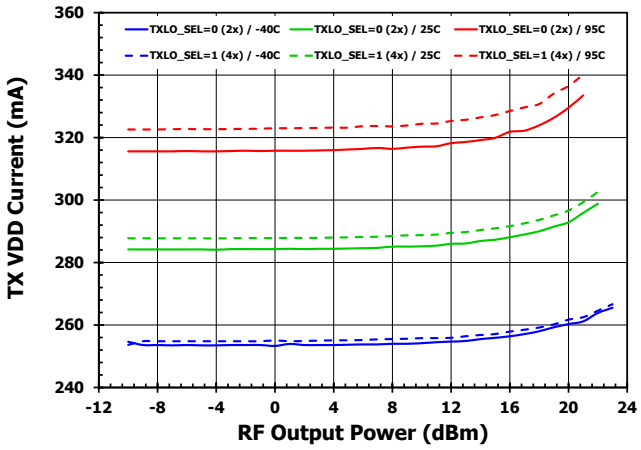

Figure 82. TX VDD Current

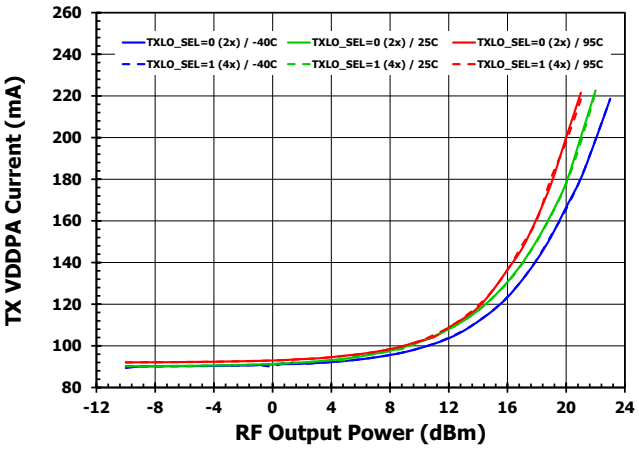

Figure 83. TX VDDPA Current

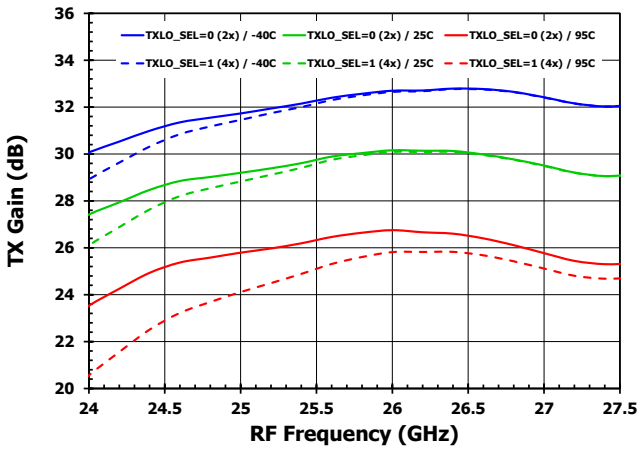

Figure 84. TX Gain

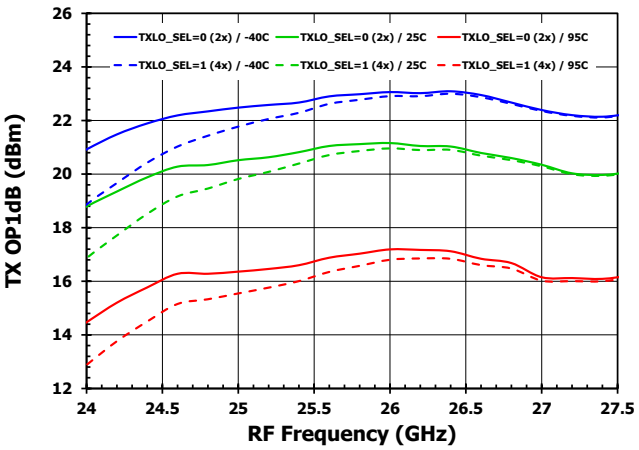

Figure 85. TX OP1dB

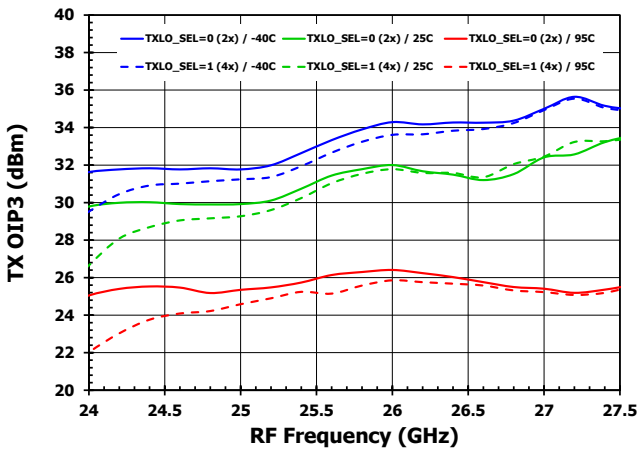

Figure 86. TX OIP3

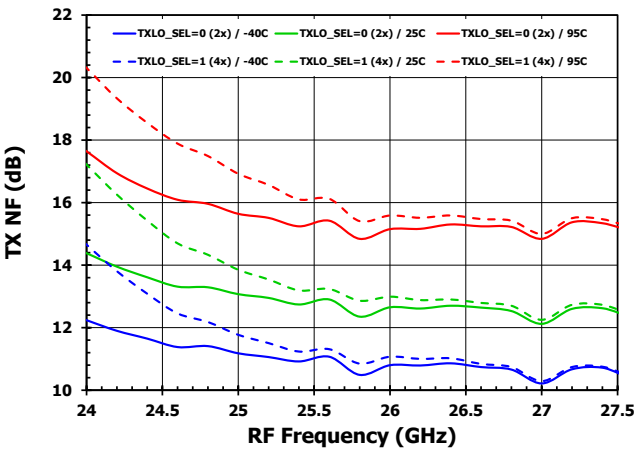

Figure 87. TX NF

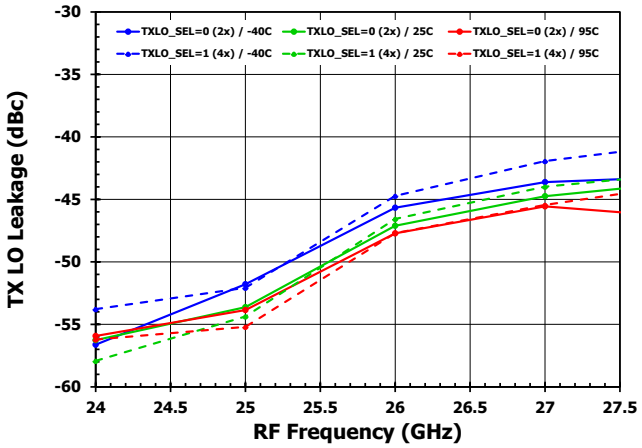

Figure 88. TX LO Leakage (uncalibrated)

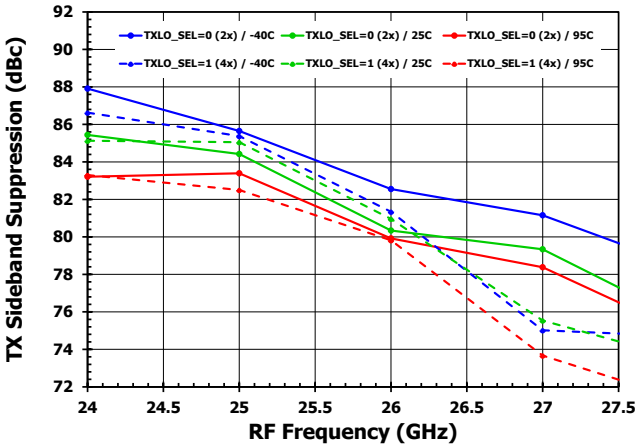

Figure 89. TX Sideband Suppression (uncalibrated)

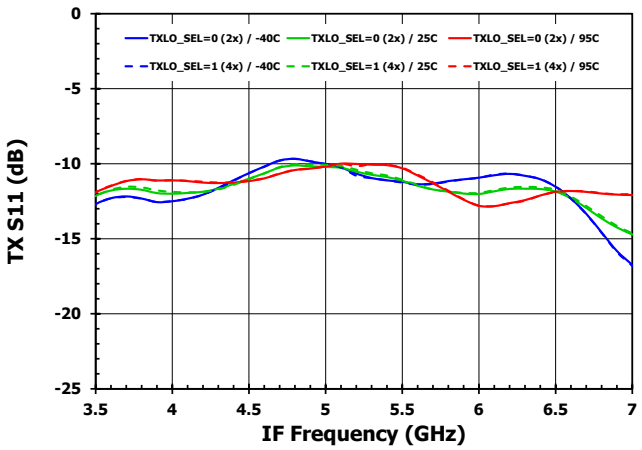

Figure 90. TX S11

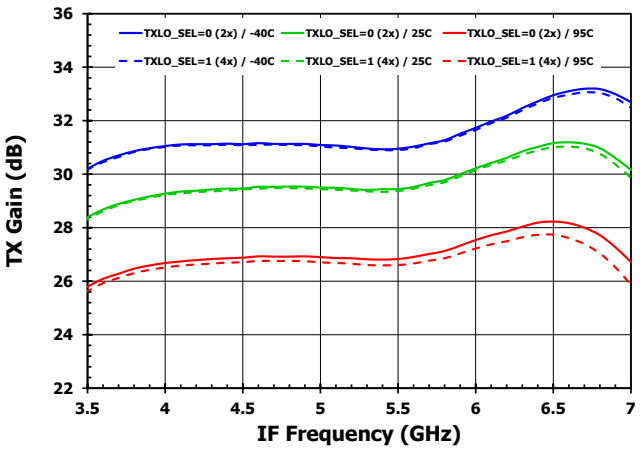

Figure 91. TX Gain vs IF

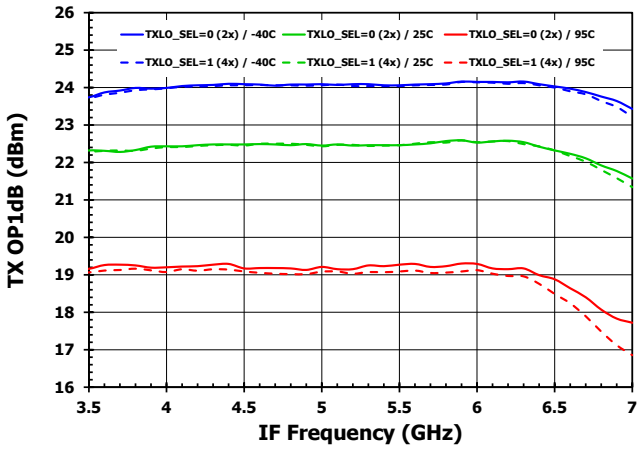

Figure 92. TX OP1dB vs IF

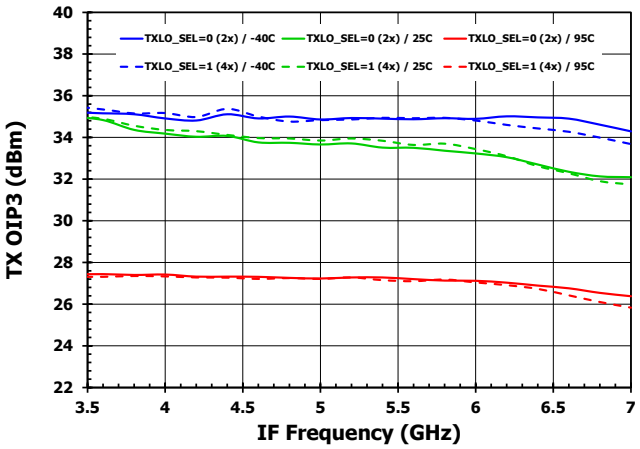

Figure 93. TX OIP3 vs IF

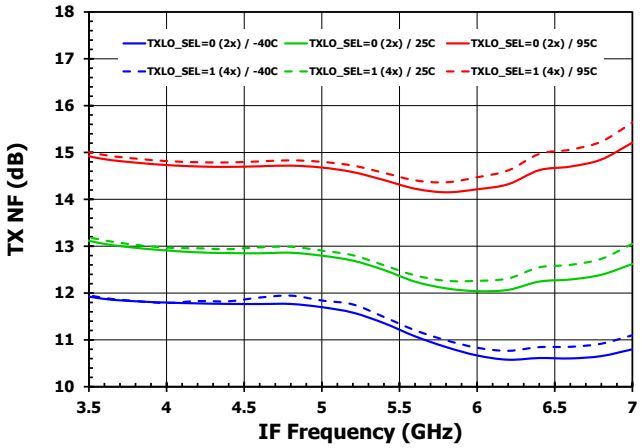

Figure 94. TX NF vs IF

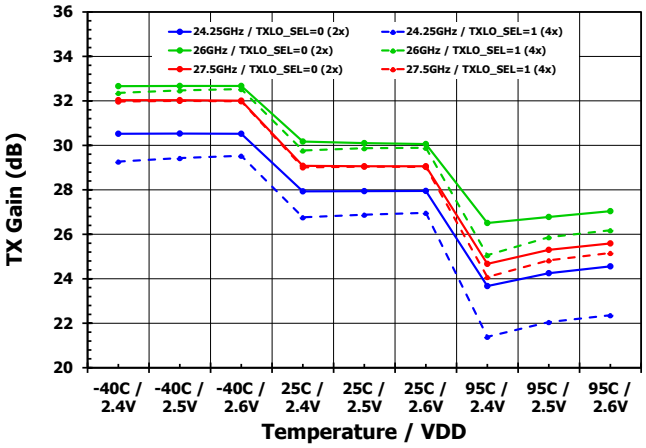

Figure 95. TX Gain over VT

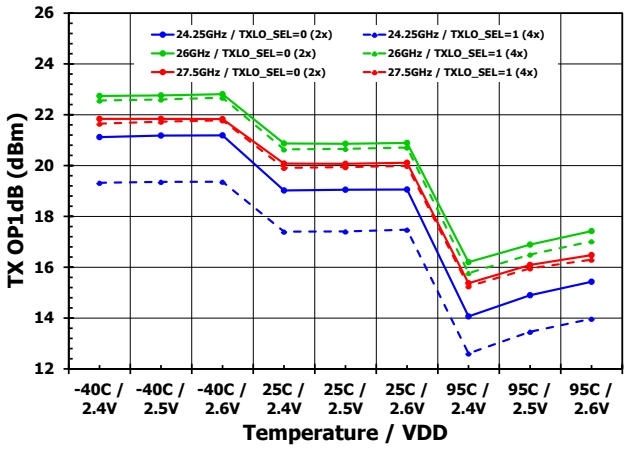

Figure 96. TX OP1dB over VT

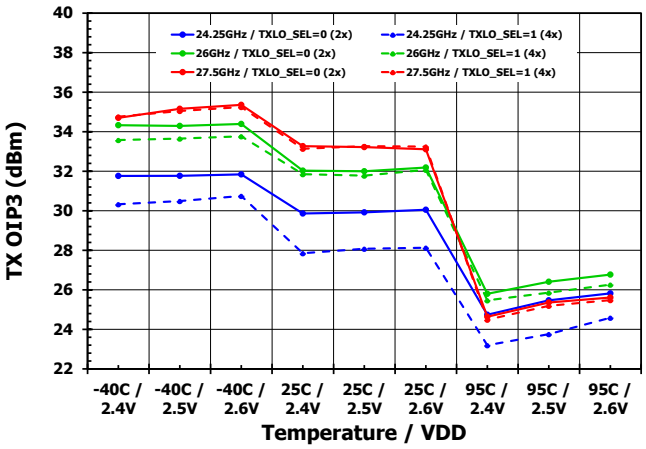

Figure 97. TX OIP3 over VT

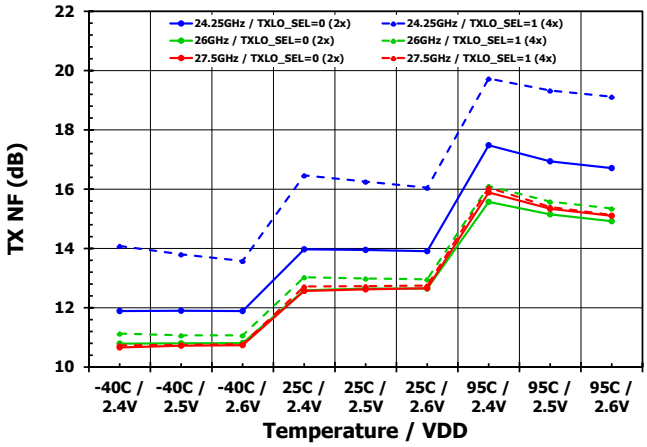

Figure 98. TX NF over VT

4.2.3 RX Performance

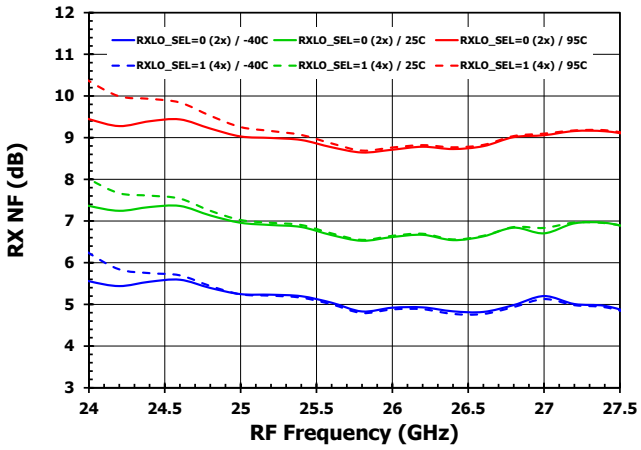

Figure 99. RX NF

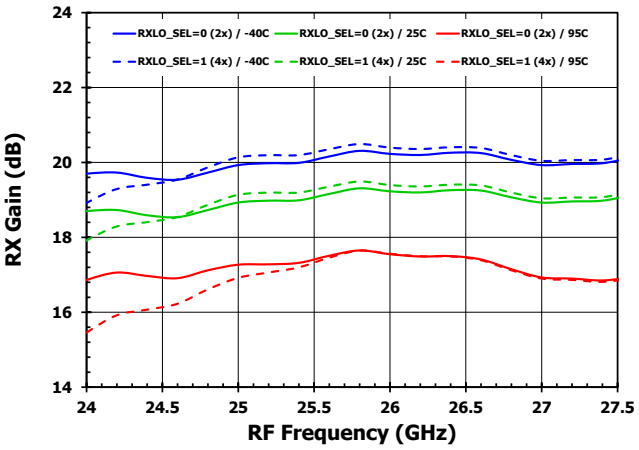

Figure 100. RX Gain

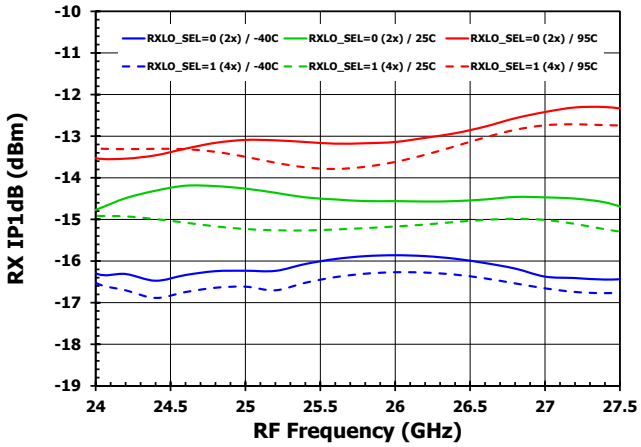

Figure 101. RX IP1dB

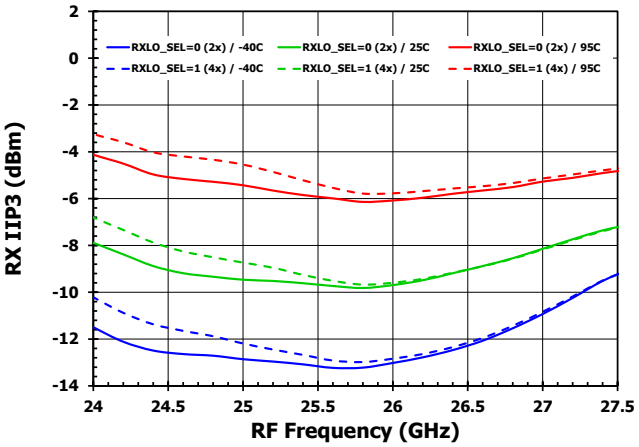

Figure 102. RX IIP3

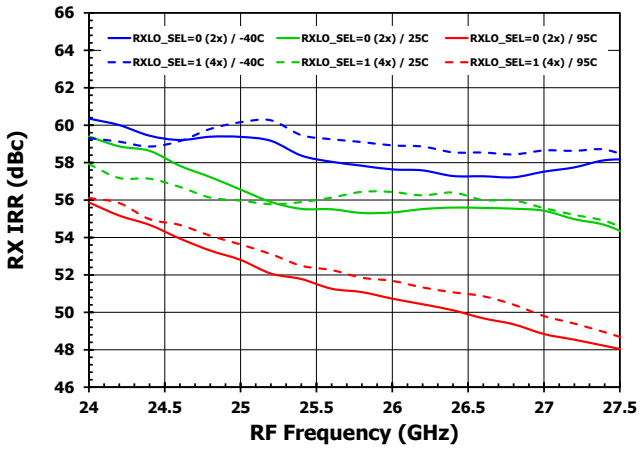

Figure 103. RX Image Rejection Ratio (uncalibrated)

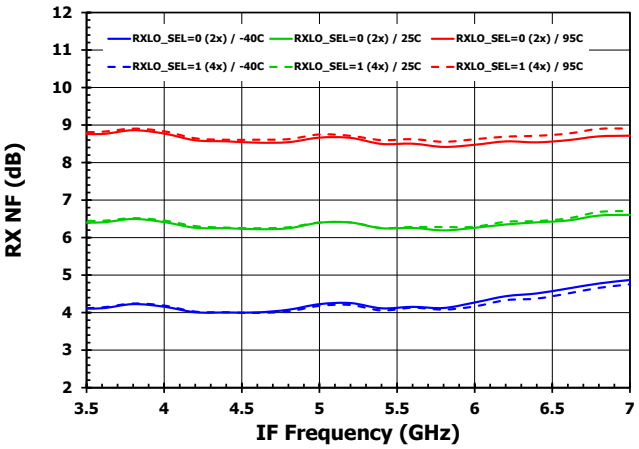

Figure 104. RX NF vs IF

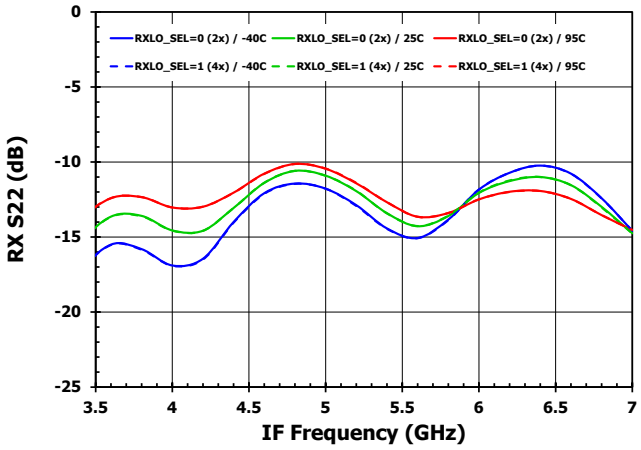

Figure 105. RX S22 vs IF

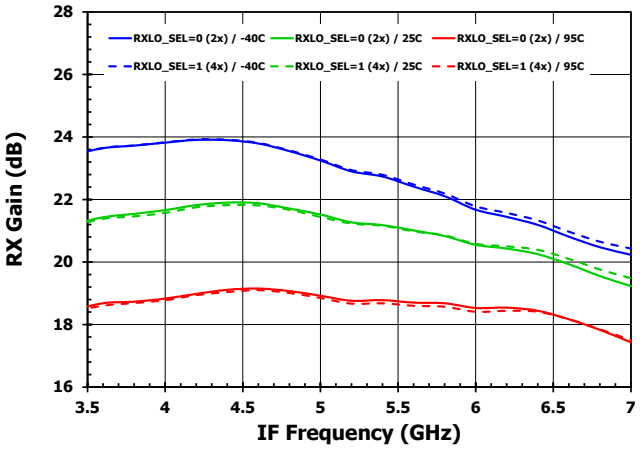

Figure 106. RX Gain vs IF

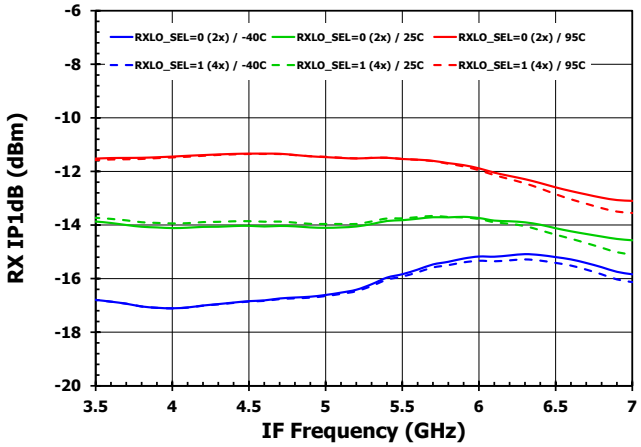

Figure 107. RX IP1dB vs IF

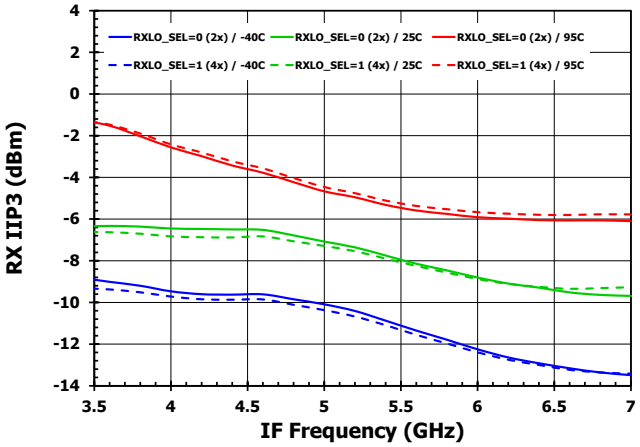

Figure 108. RX IIP3 vs IF

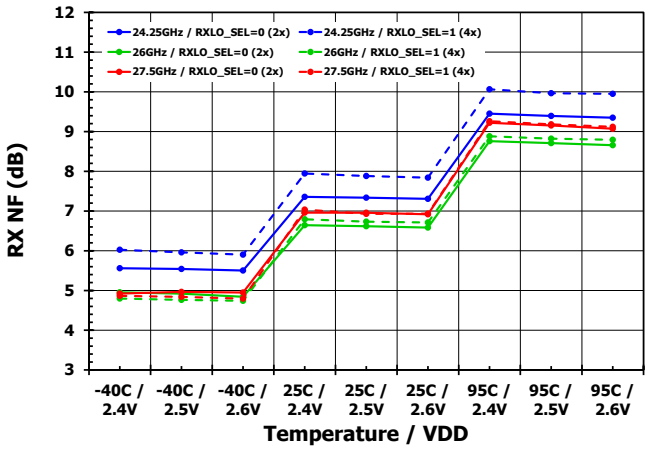

Figure 109. RX NF over VT

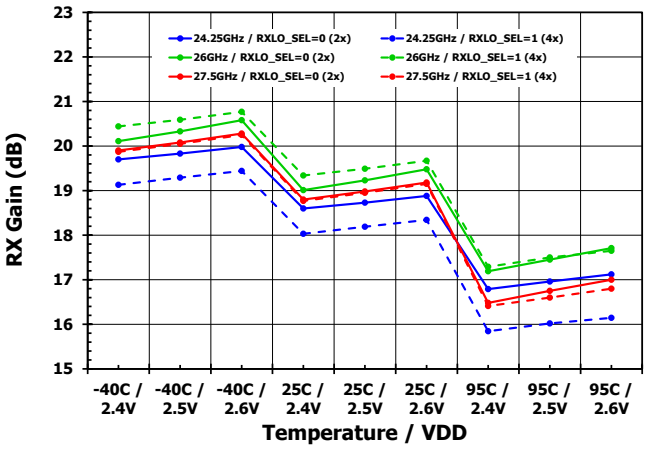

Figure 110. RX Gain over VT

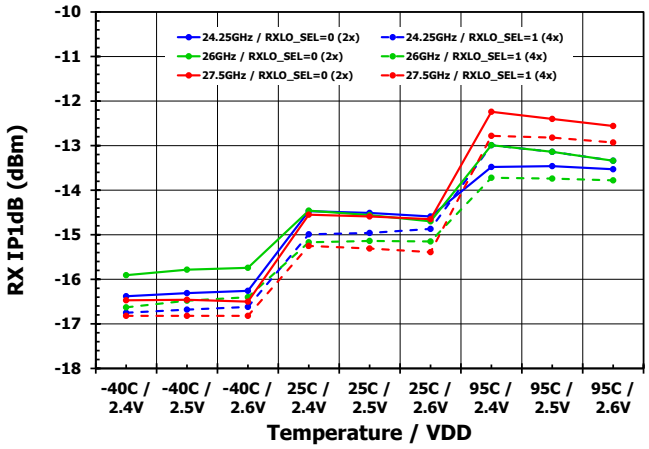

Figure 111. RX IP1dB over VT

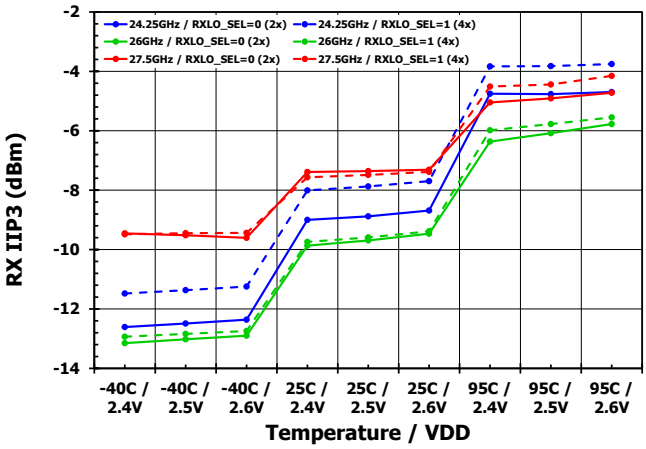

Figure 112. RX IIP3 over VT

4.2.4 RX Performance – RX2 Path

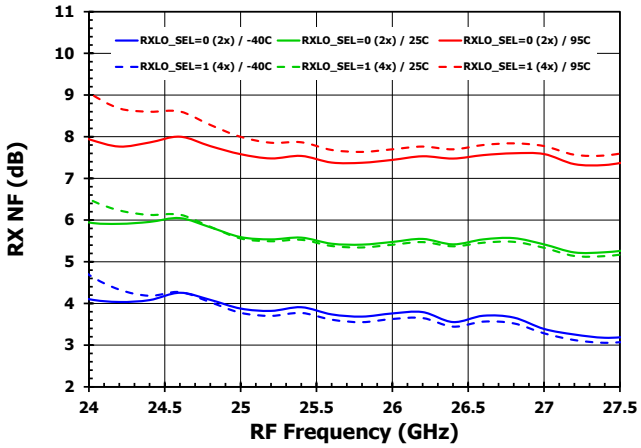

Figure 113. RX2 NF

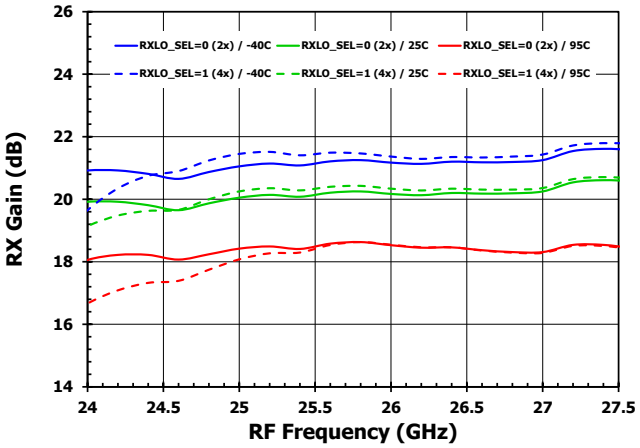

Figure 114. RX2 Gain

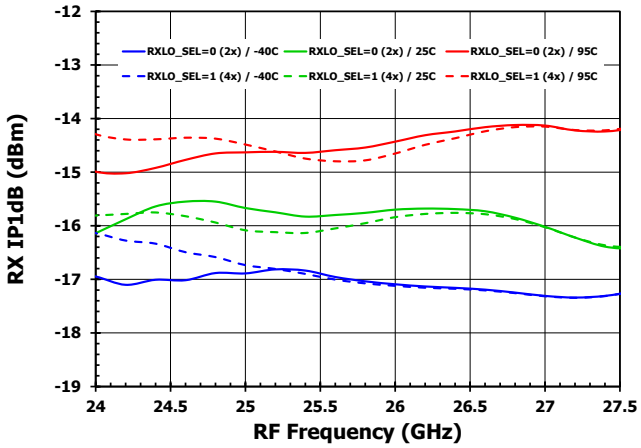

Figure 115. RX2 IP1dB

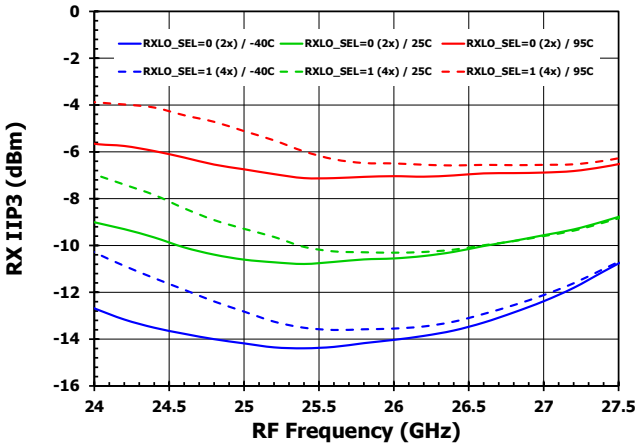

Figure 116. RX2 IIP3

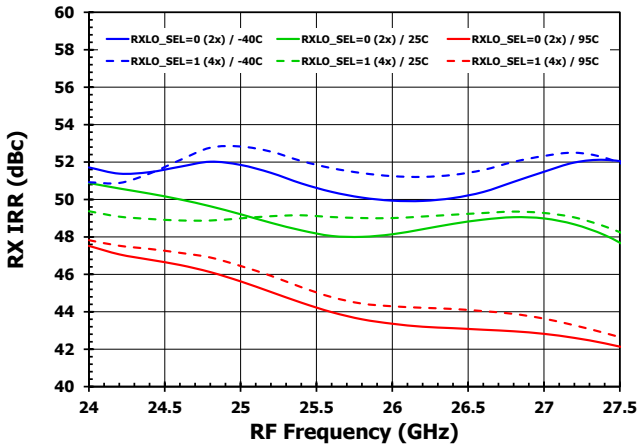

Figure 117. RX2 Image Rejection Ratio (uncalibrated)

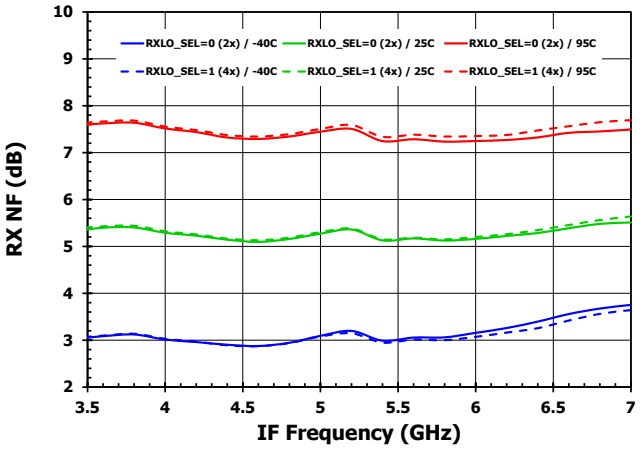

Figure 118. RX2 NF vs IF

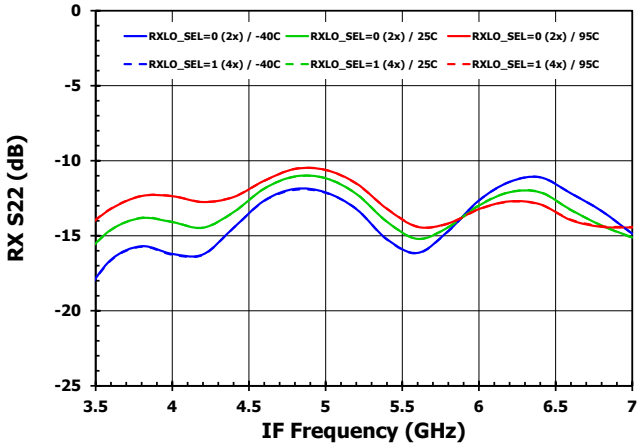

Figure 119. RX2 S22 vs IF

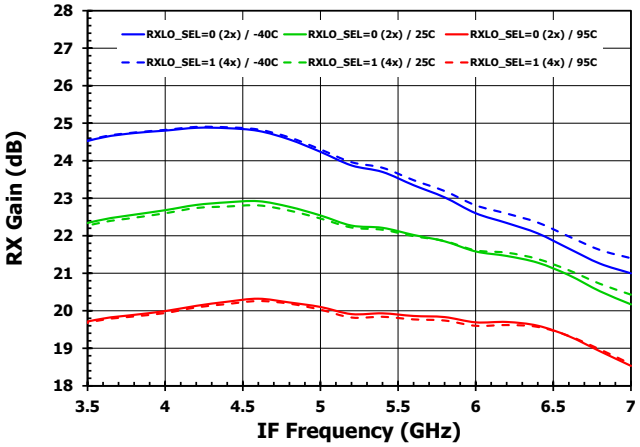

Figure 120. RX2 Gain vs IF

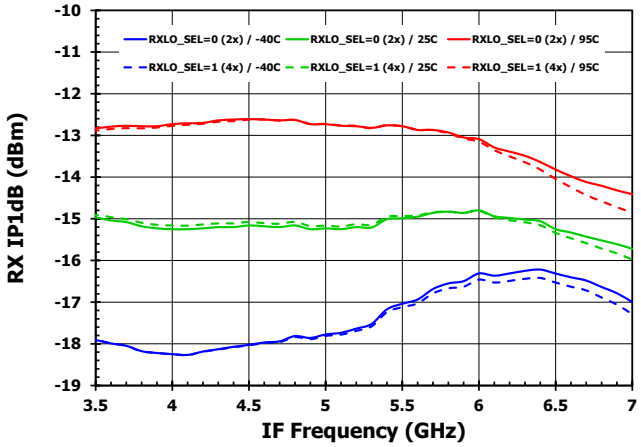

Figure 121. RX2 IP1dB vs IF

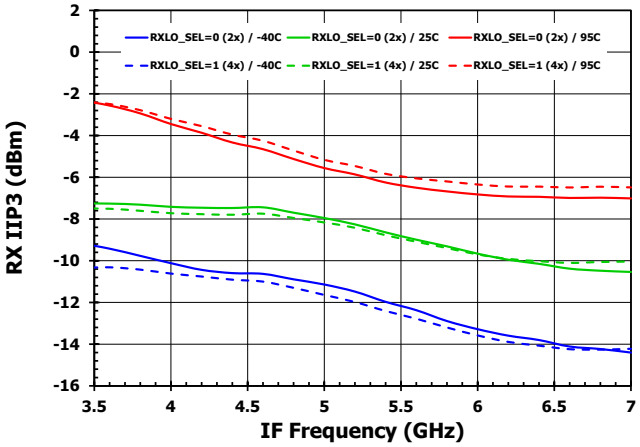

Figure 122. RX2 IIP3 vs IF

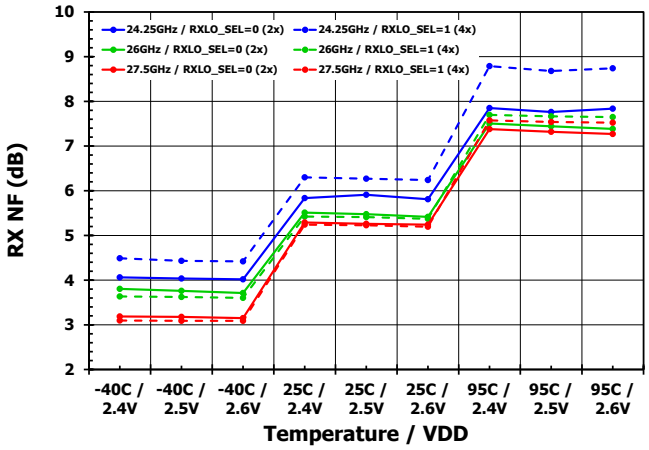

Figure 123. RX2 NF over VT

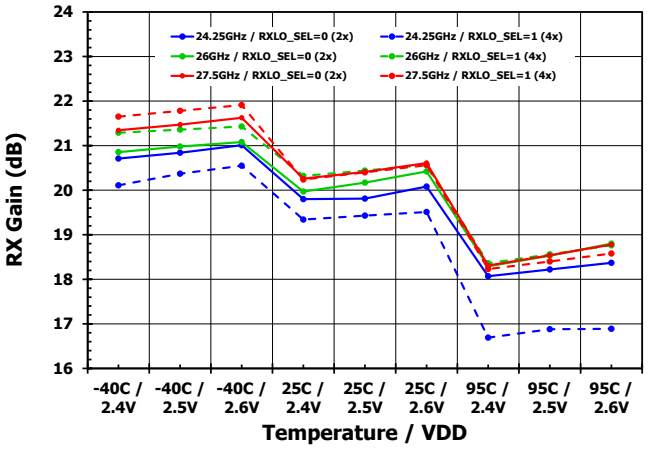

Figure 124. RX2 Gain over VT

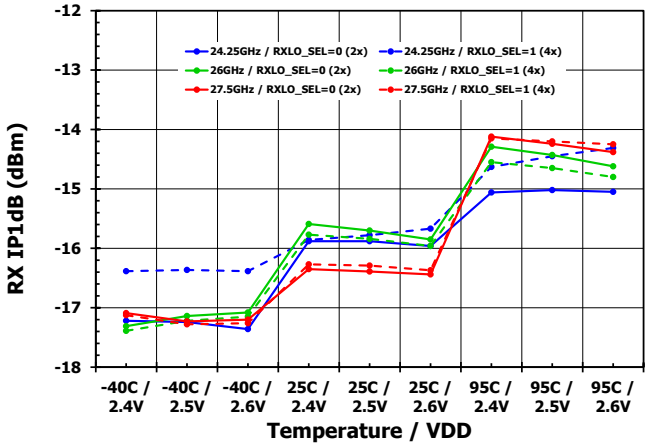

Figure 125. RX2 IP1dB over VT

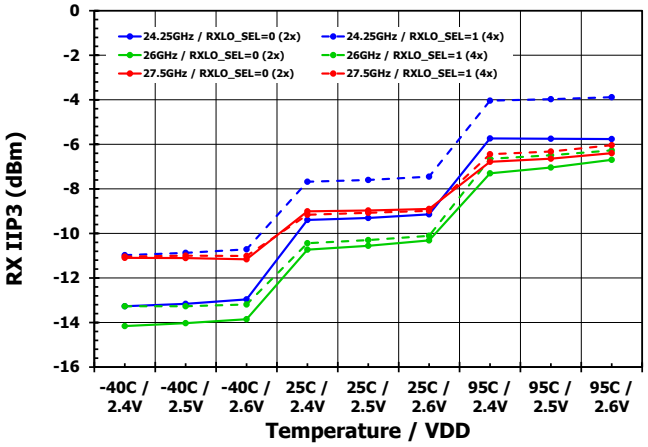

Figure 126. RX2 IIP3 over VT

4.3 5GHz IF/28GHz RF (Band H8)

4.3.1 TX Performance

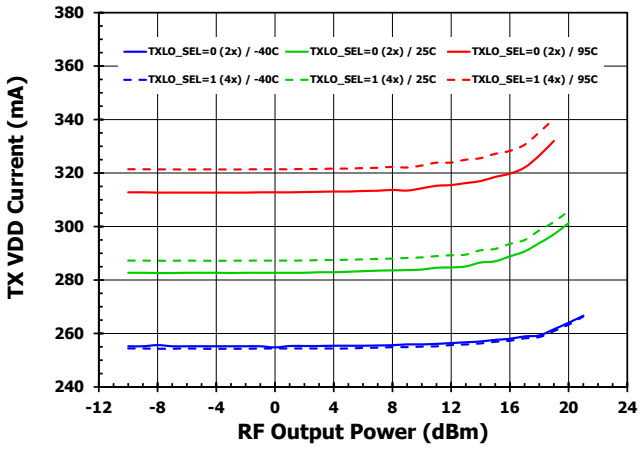

Figure 127. TX VDD Current

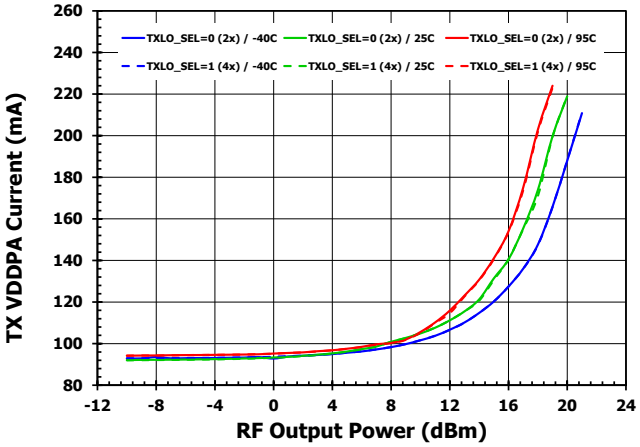

Figure 128. TX VDDPA Current

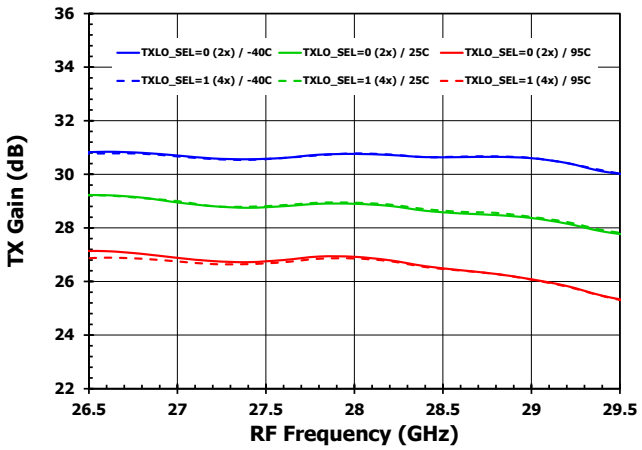

Figure 129. TX Gain

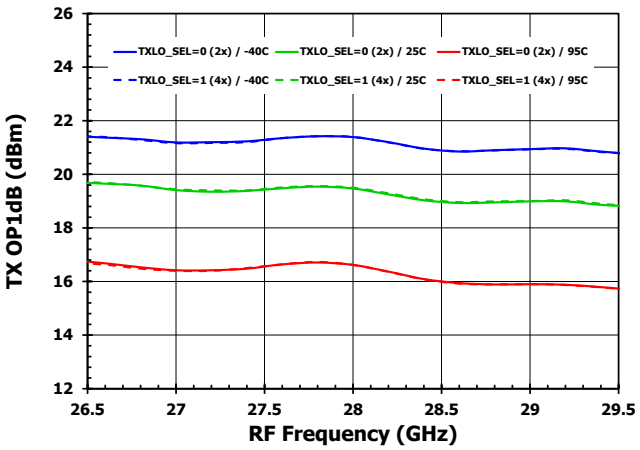

Figure 130. TX OP1dB

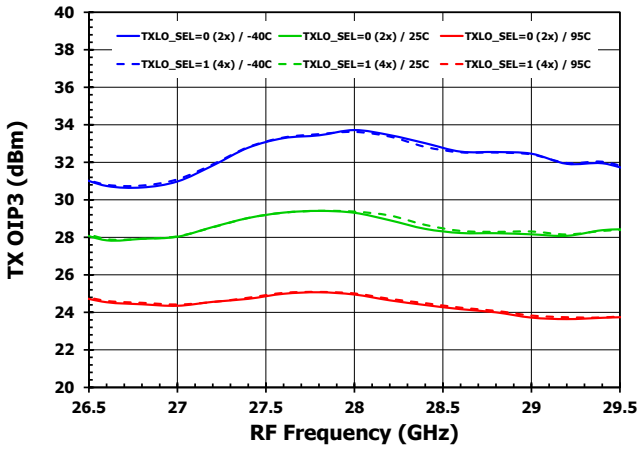

Figure 131. TX OIP3

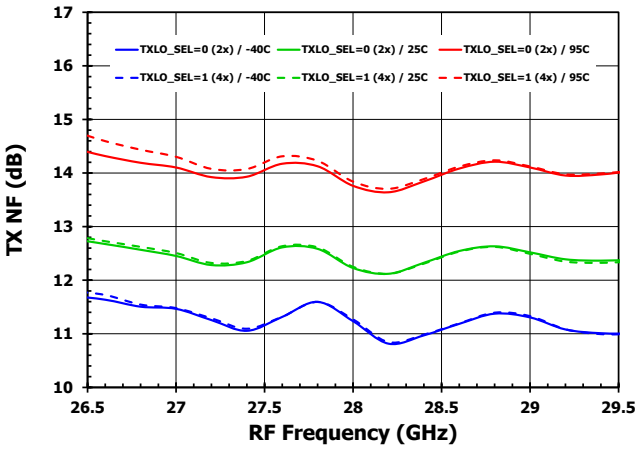

Figure 132. TX NF

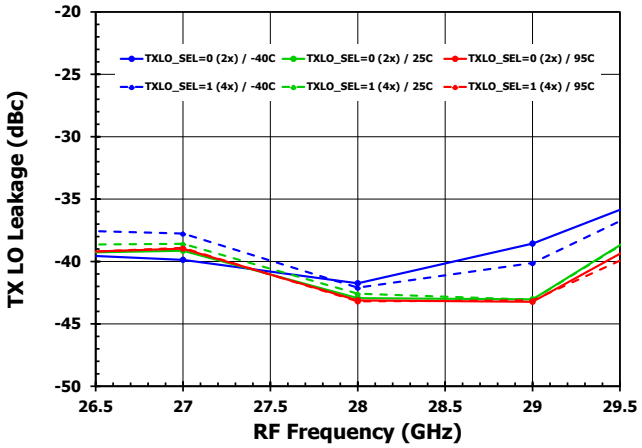

Figure 133. TX LO Leakage (uncalibrated)

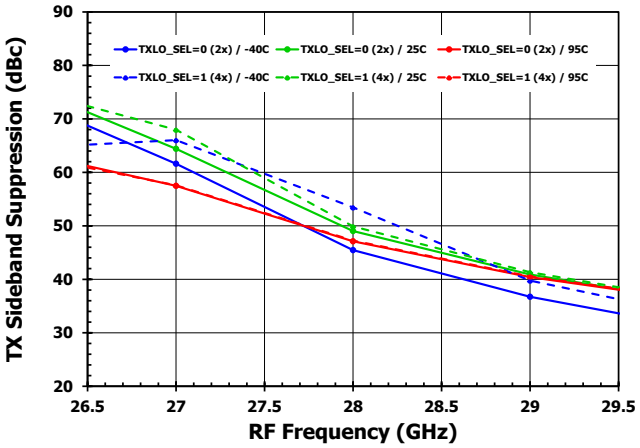

Figure 134. TX Sideband Suppression (uncalibrated)

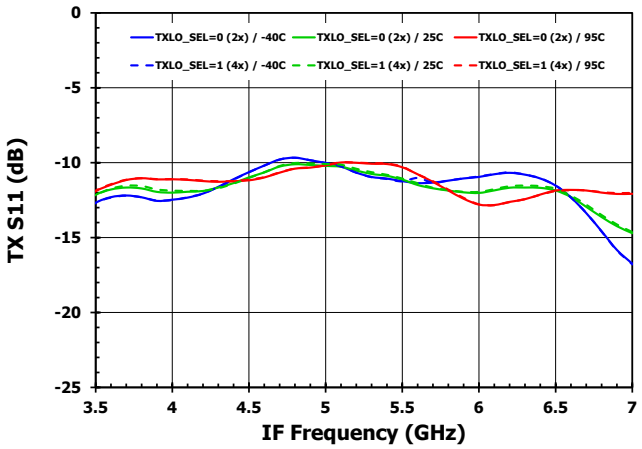

Figure 135. TX S11

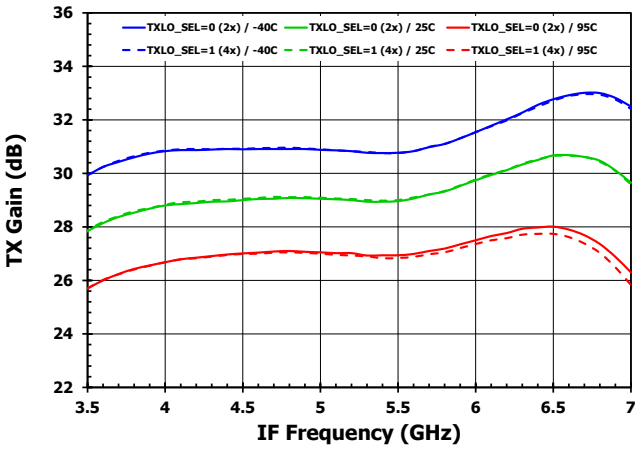

Figure 136. TX Gain vs IF

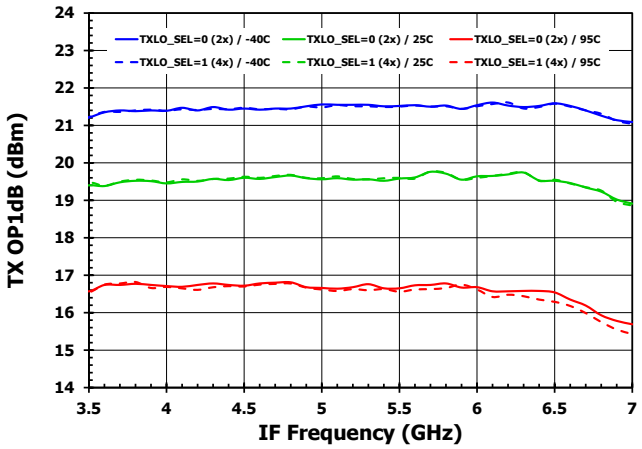

Figure 137. TX OP1dB vs IF

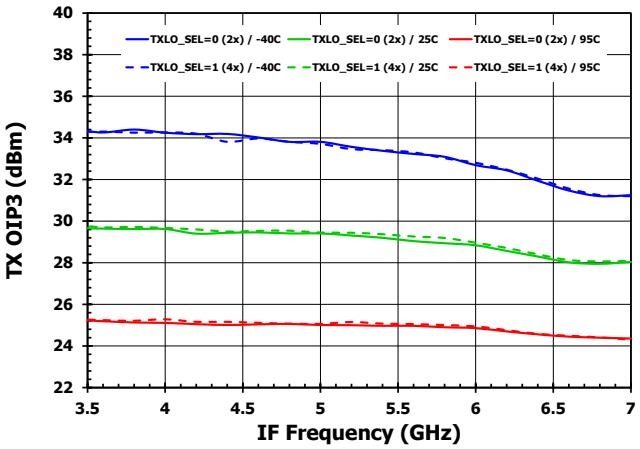

Figure 138. TX OIP3 vs IF

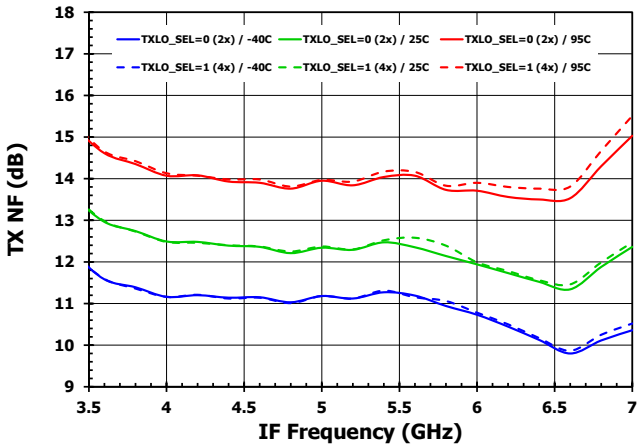

Figure 139. TX NF vs IF

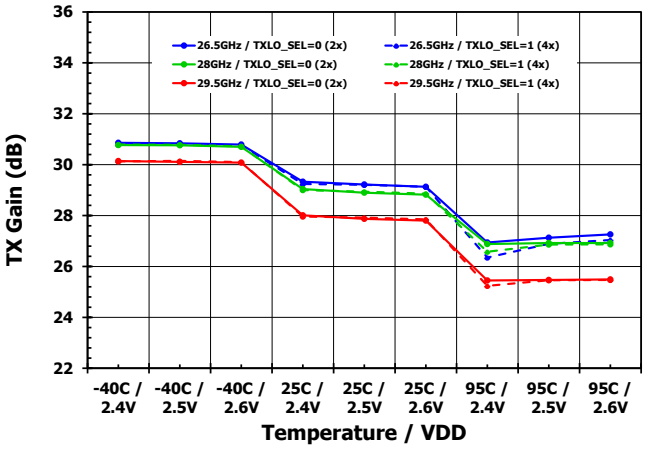

Figure 140. TX Gain over VT

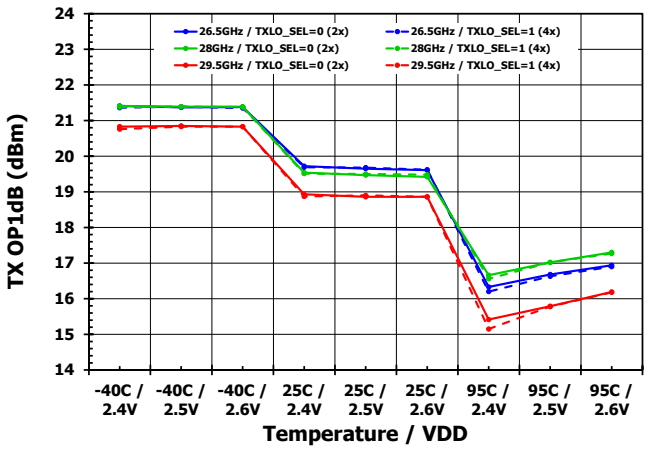

Figure 141. TX OP1dB over VT

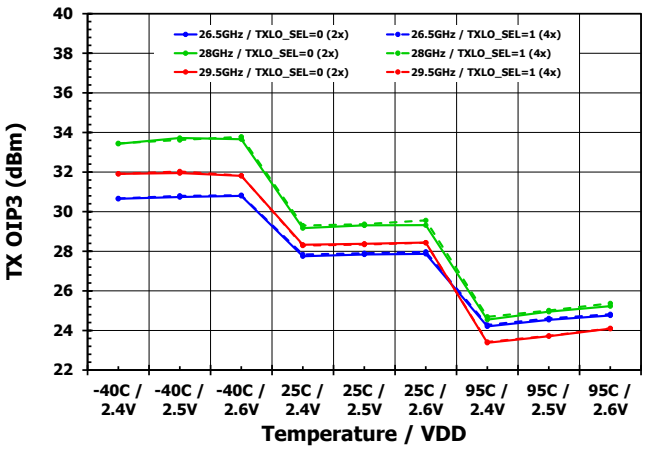

Figure 142. TX OIP3 over VT

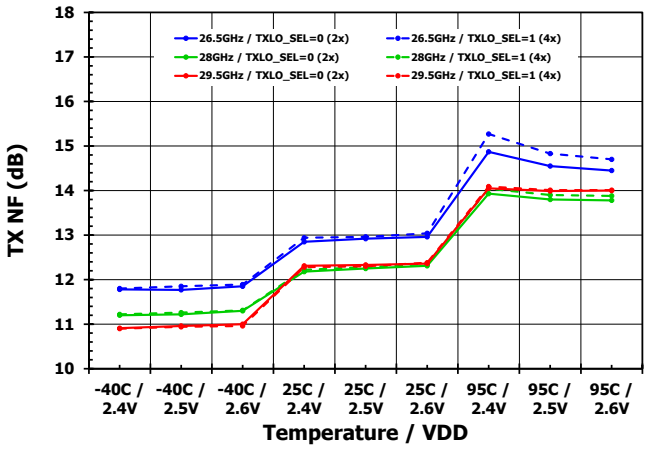

Figure 143. TX NF over VT

4.3.2 TX Performance – V_{DDPA} = 3.3V

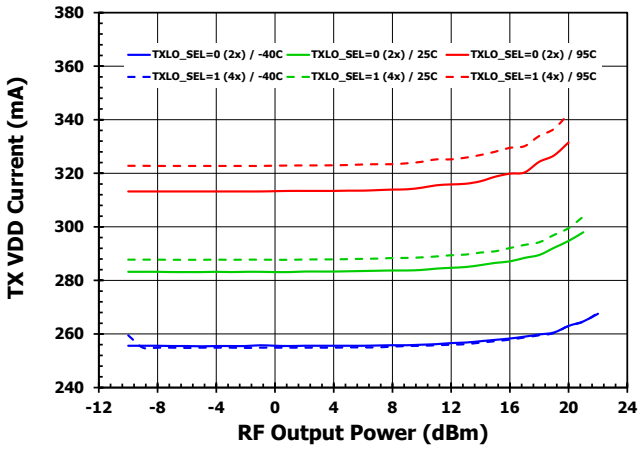

Figure 144. TX VDD Current

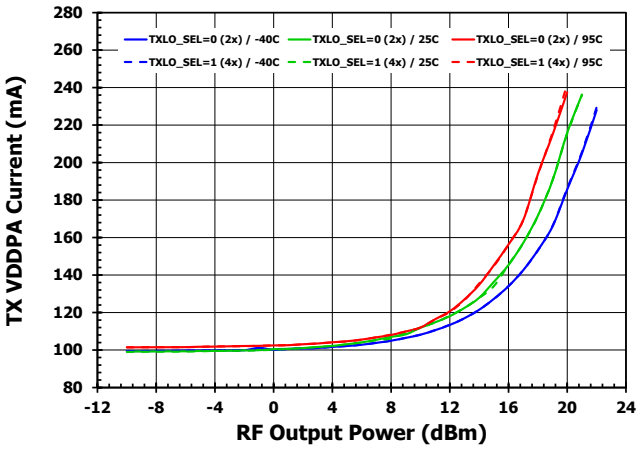

Figure 145. TX VDDPA Current

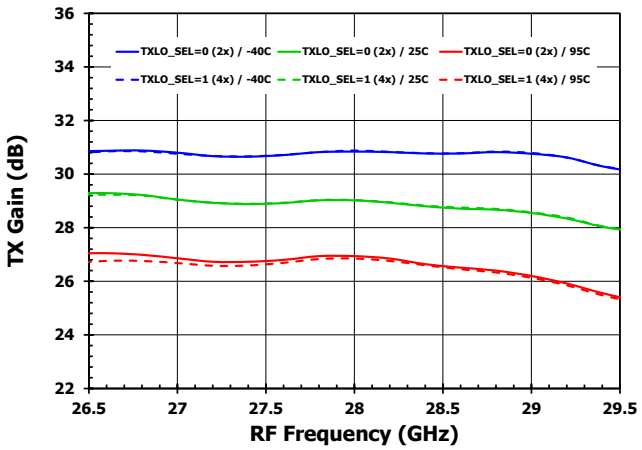

Figure 146. TX Gain

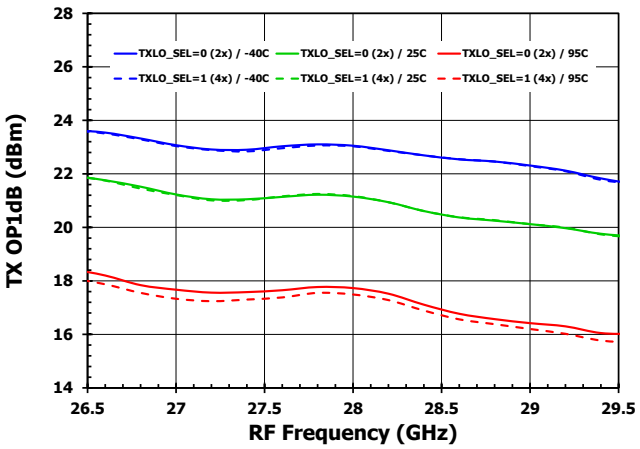

Figure 147. TX OP1dB

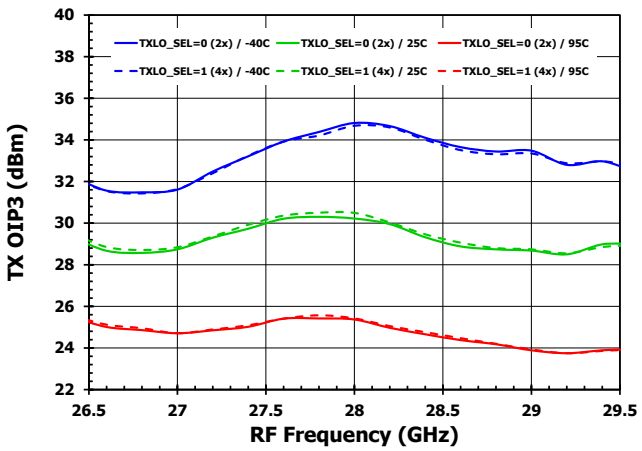

Figure 148. TX OIP3

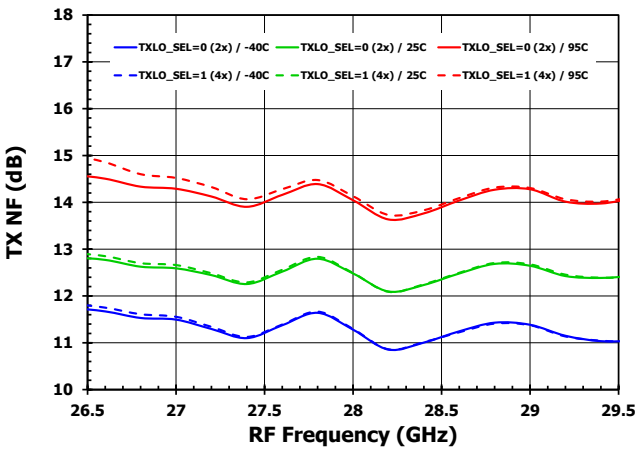

Figure 149. TX NF

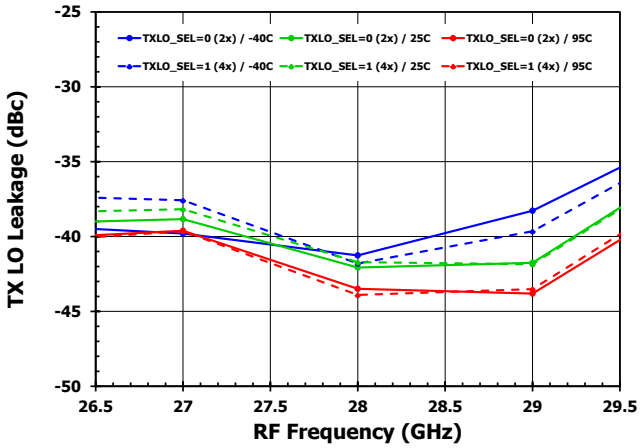

Figure 150. TX LO Leakage (uncalibrated)

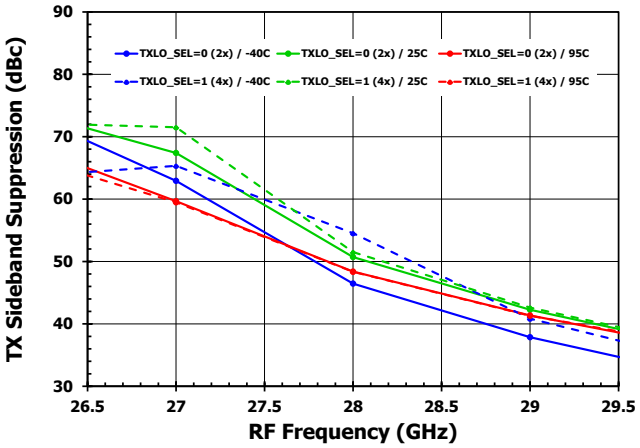

Figure 151. TX Sideband Suppression (uncalibrated)

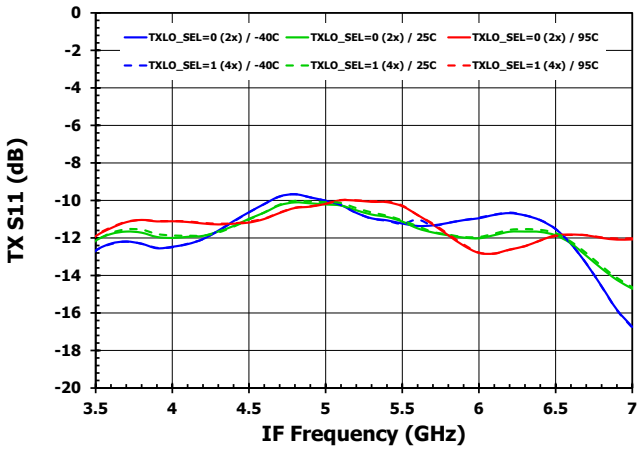

Figure 152. TX S11

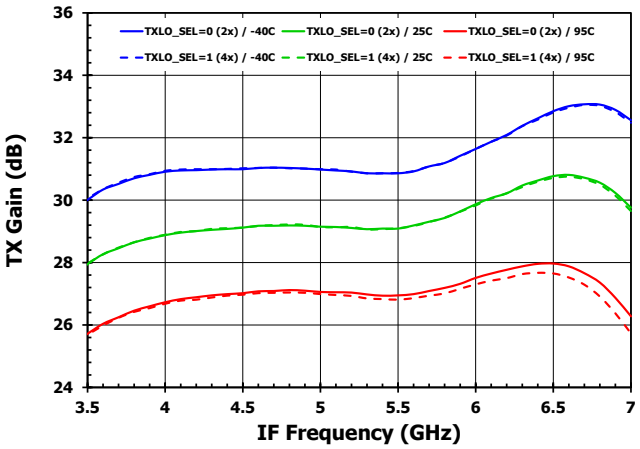

Figure 153. TX Gain vs IF

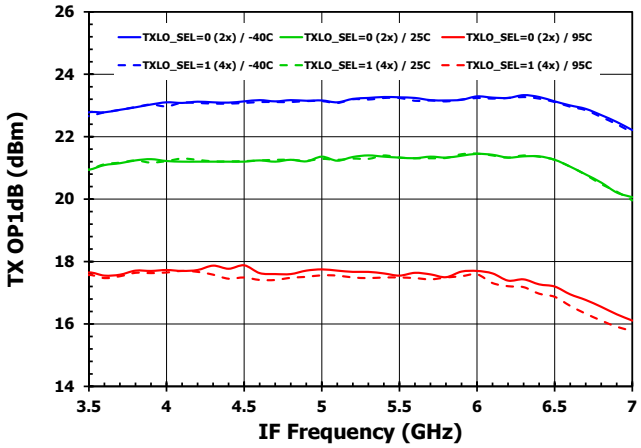

Figure 154. TX OP1dB vs IF

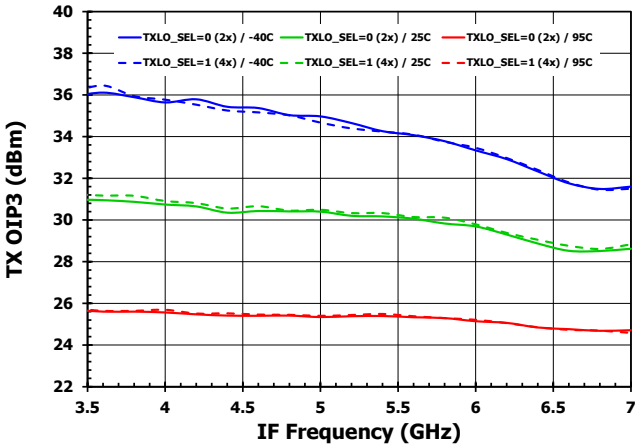

Figure 155. TX OIP3 vs IF

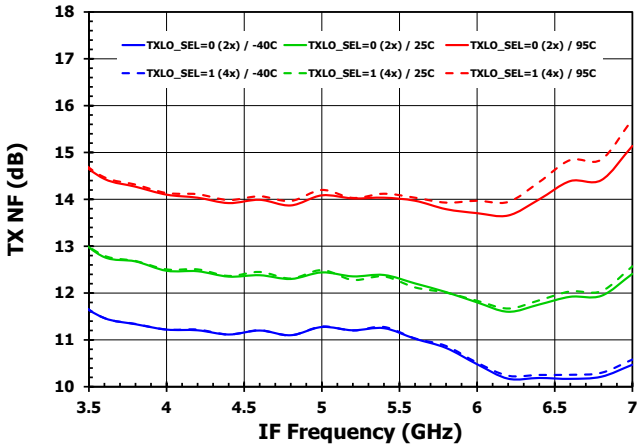

Figure 156. TX NF vs IF

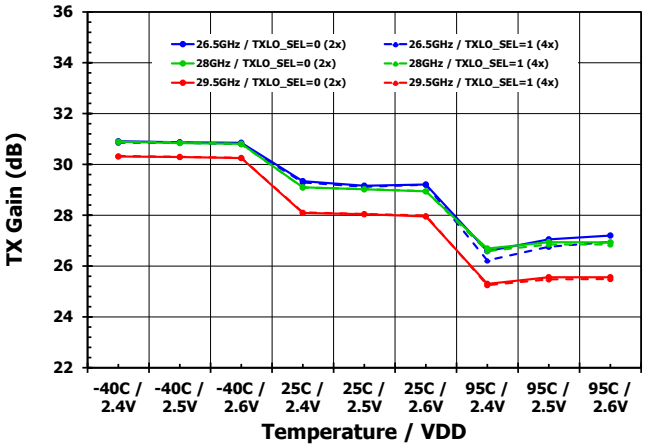

Figure 157. TX Gain over VT

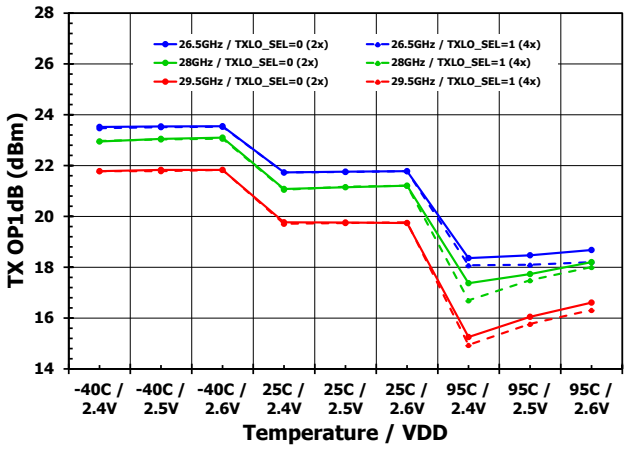

Figure 158. TX OP1dB over VT

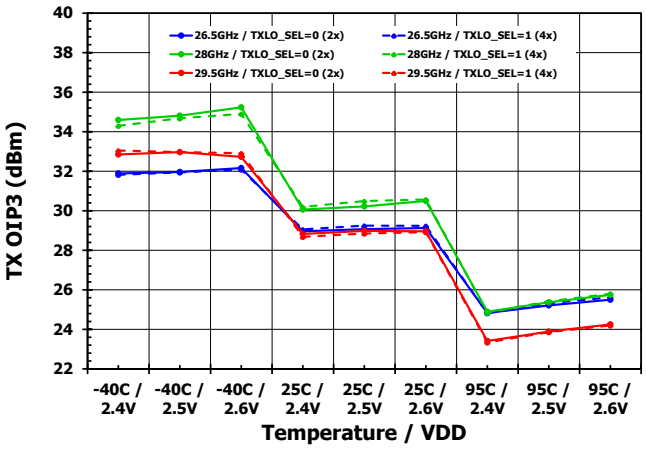

Figure 159. TX OIP3 over VT

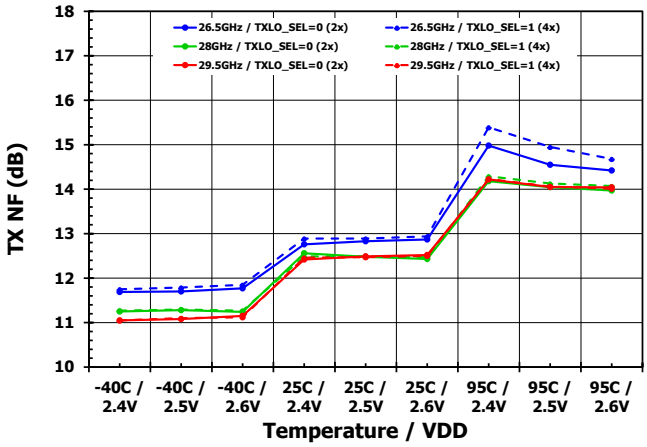

Figure 160. TX NF over VT

4.3.3 RX Performance

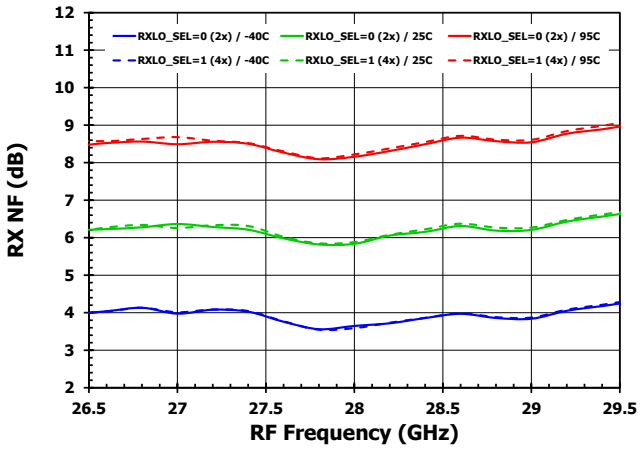

Figure 161. RX NF

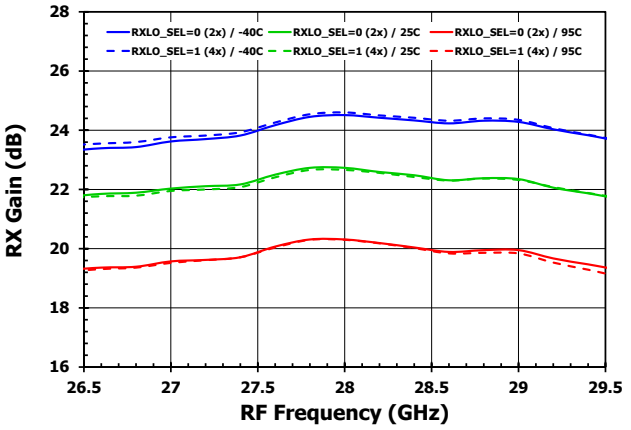

Figure 162. RX Gain

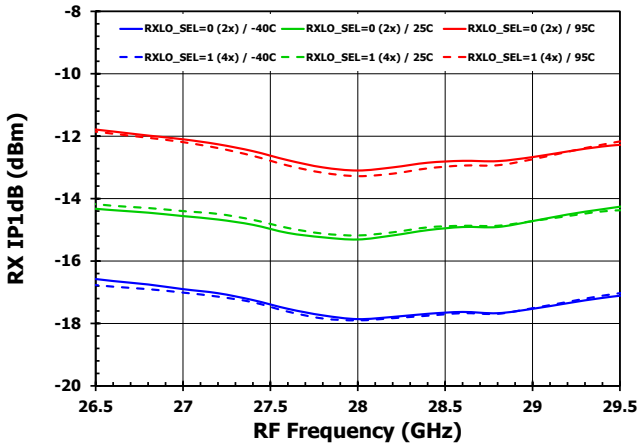

Figure 163. RX IP1dB

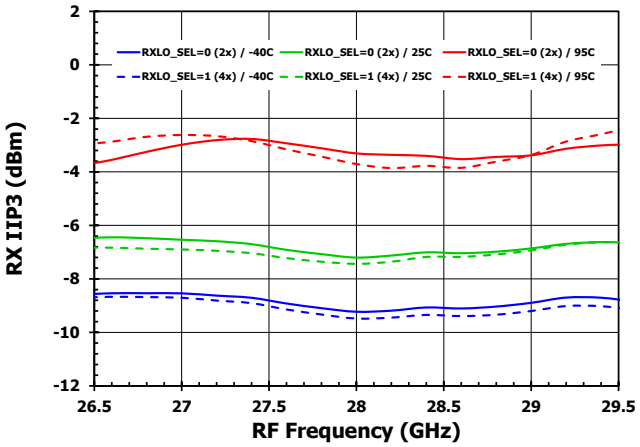

Figure 164. RX IIP3

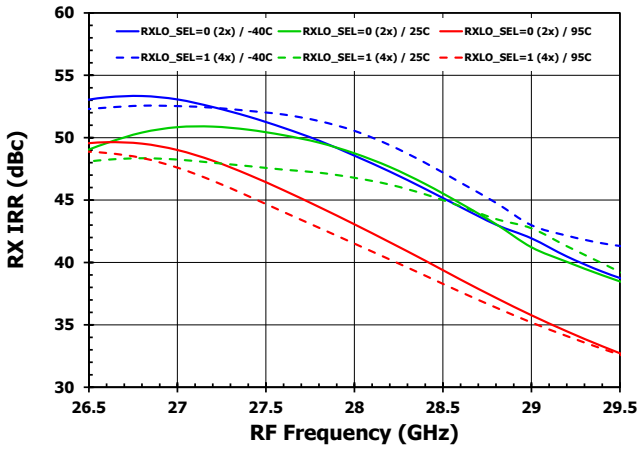

Figure 165. RX Image Rejection Ratio (uncalibrated)

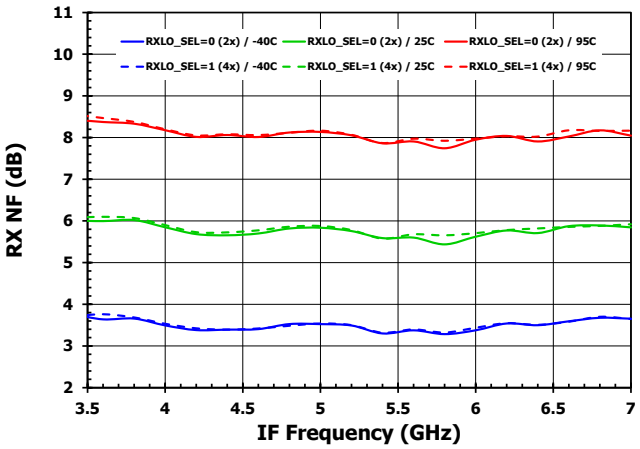

Figure 166. RX NF vs IF

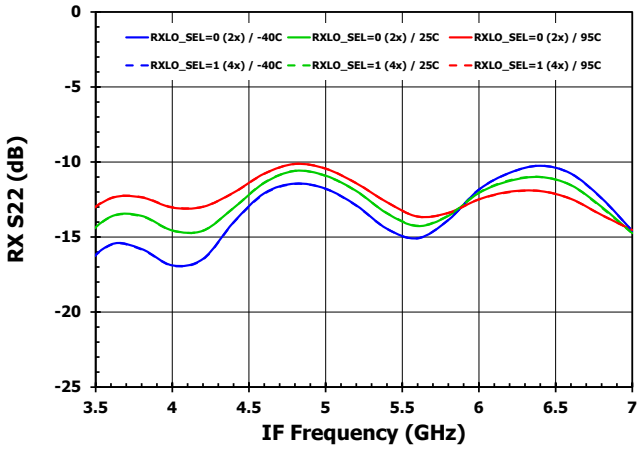

Figure 167. RX S22 vs IF

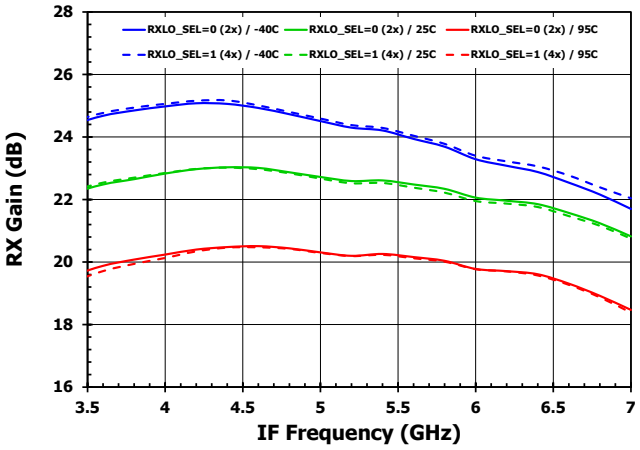

Figure 168. RX Gain vs IF

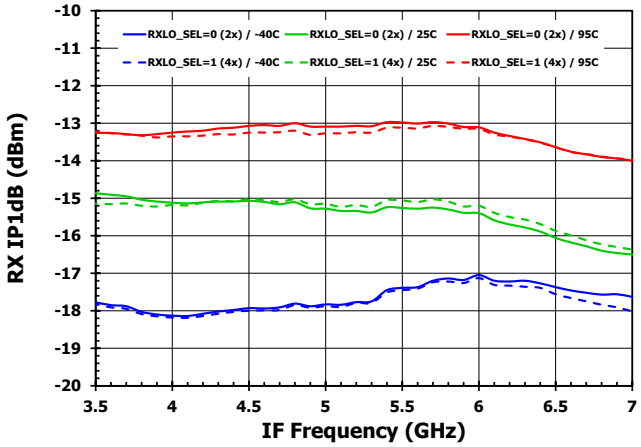

Figure 169. RX IP1dB vs IF

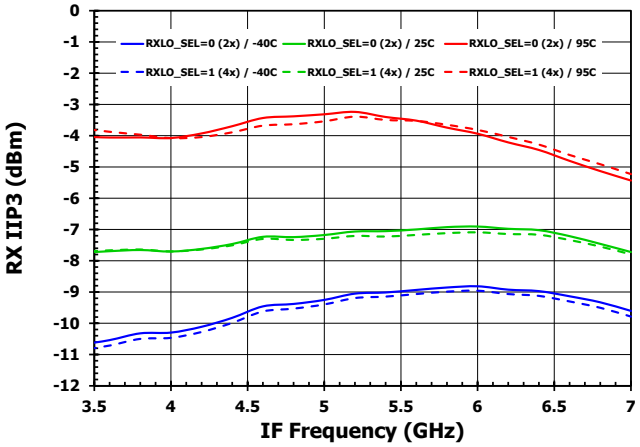

Figure 170. RX IIP3 vs IF

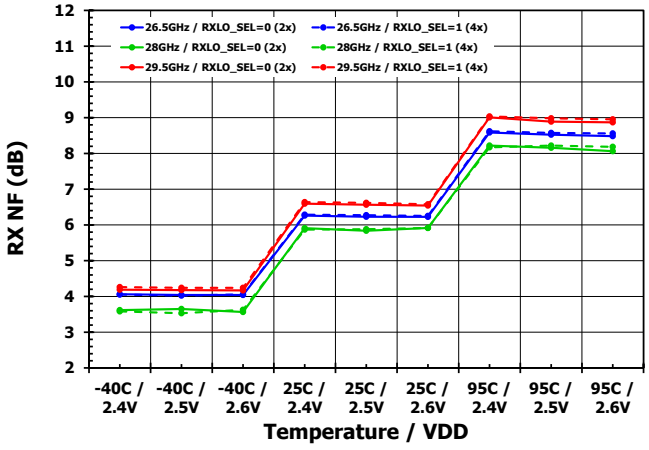

Figure 171. RX NF over VT

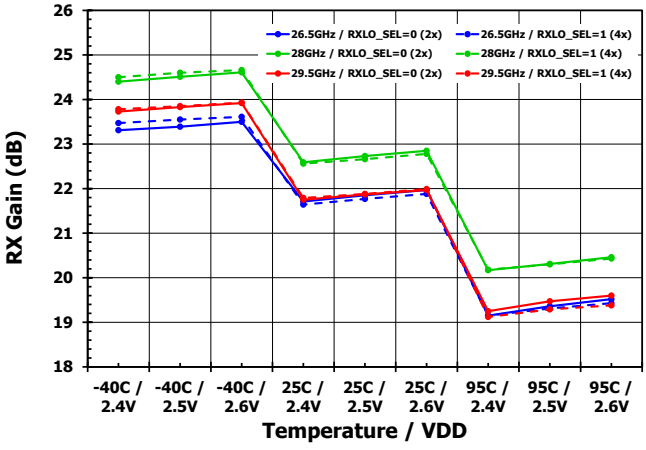

Figure 172. RX Gain over VT

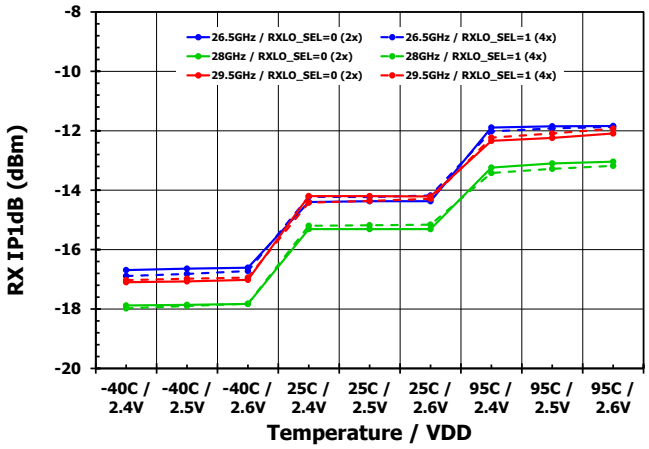

Figure 173. RX IP1dB over VT

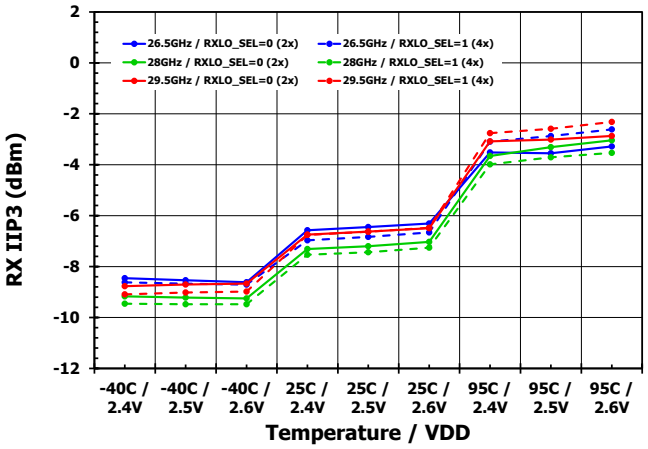

Figure 174. RX IIP3 over VT

4.3.4 RX Performance – RX2 Path

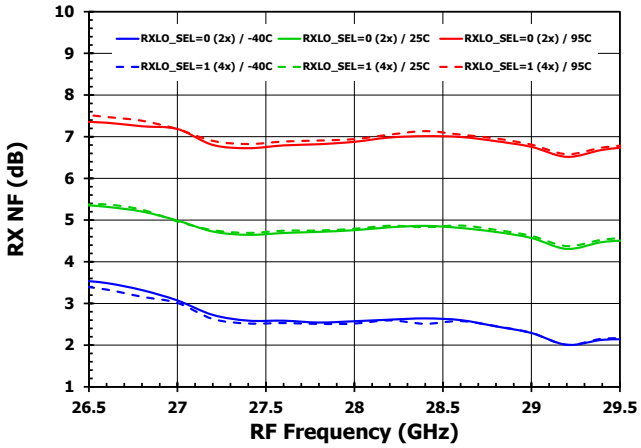

Figure 175. RX2 NF

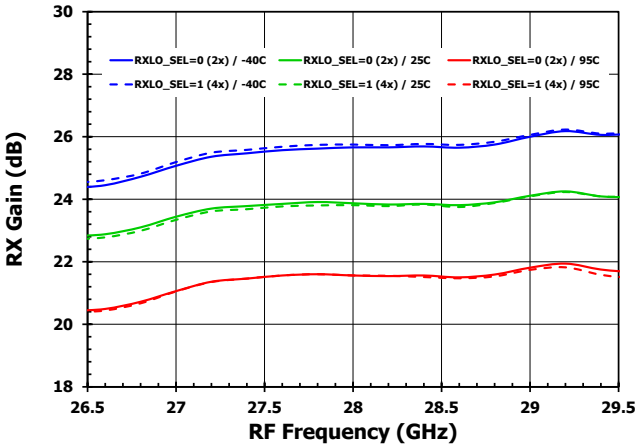

Figure 176. RX2 Gain

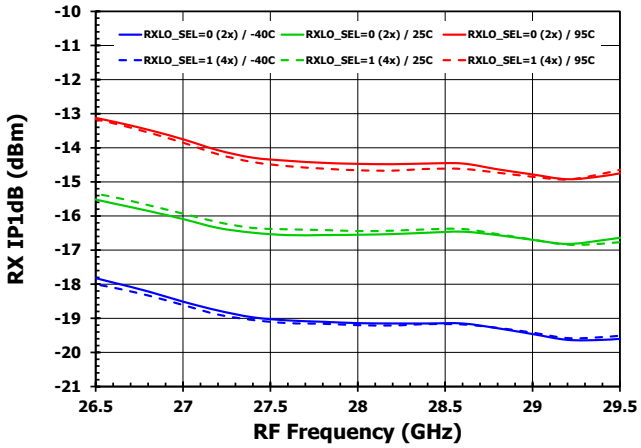

Figure 177. RX2 IP1dB

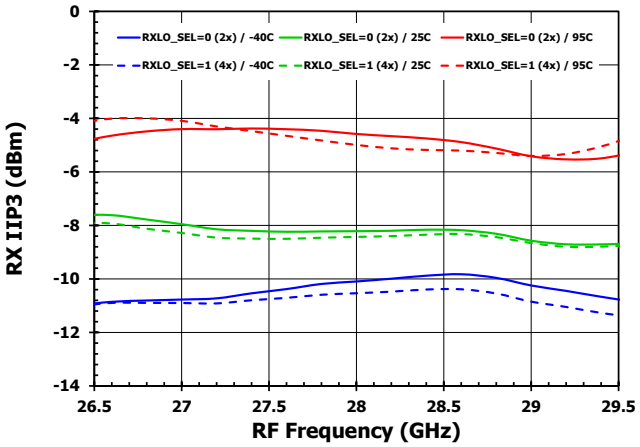

Figure 178. RX2 IIP3

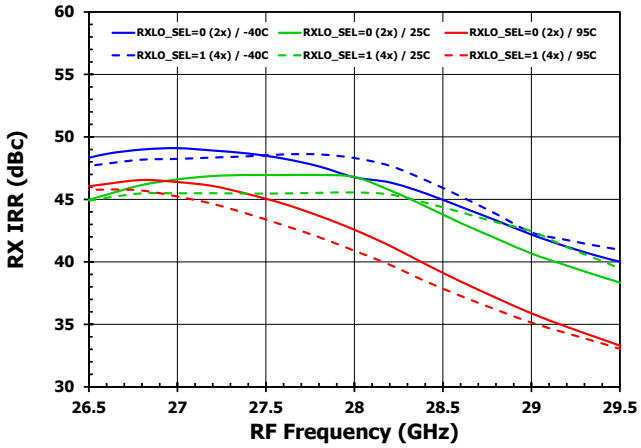

Figure 179. RX2 Image Rejection Ratio (uncalibrated)

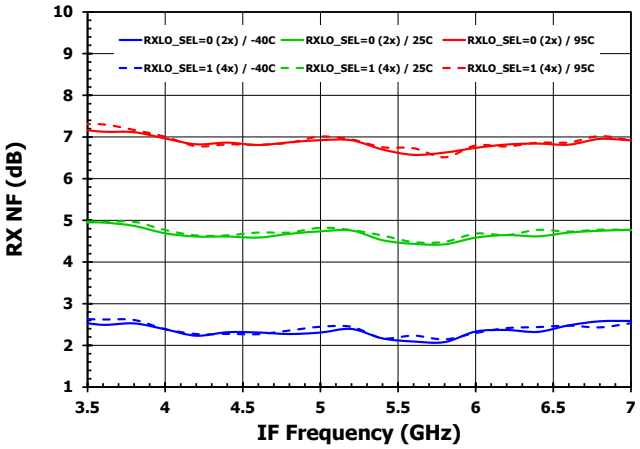

Figure 180. RX2 NF vs IF

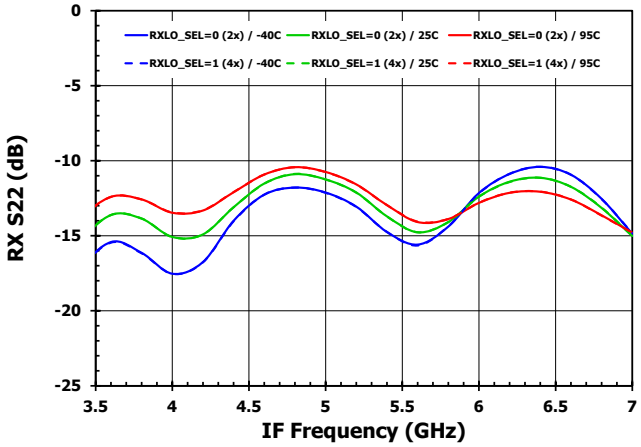

Figure 181. RX2 S22 vs IF

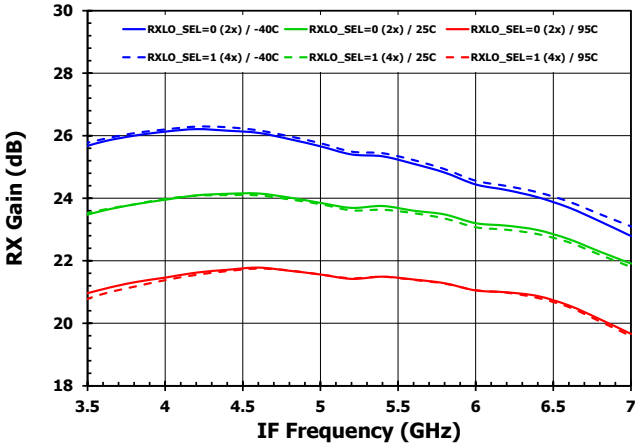

Figure 182. RX2 Gain vs IF

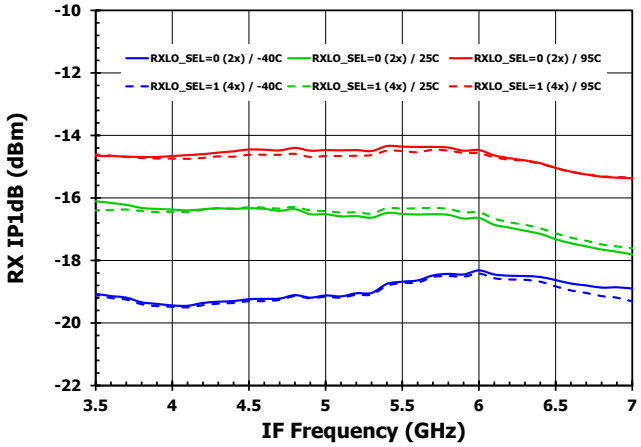

Figure 183. RX2 IP1dB vs IF

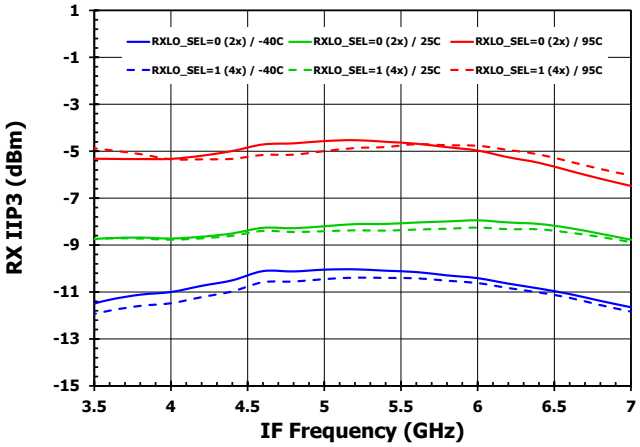

Figure 184. RX2 IIP3 vs IF

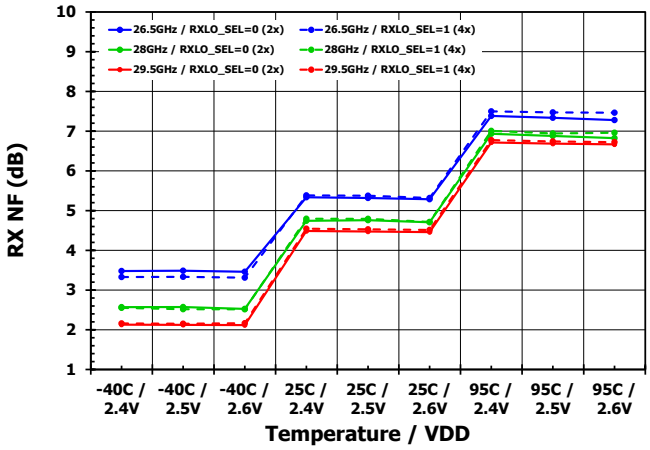

Figure 185. RX2 NF over VT

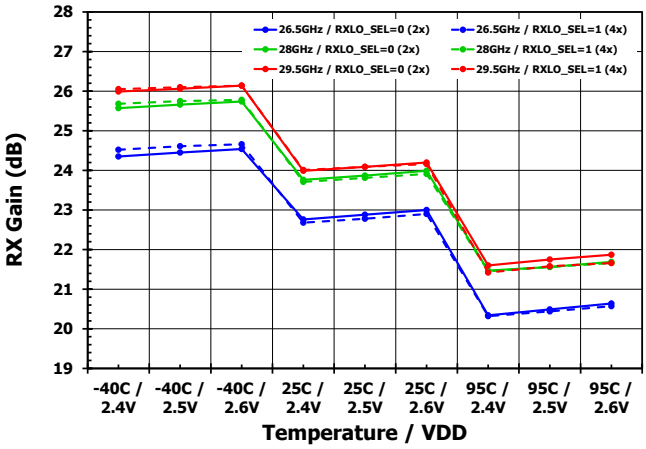

Figure 186. RX2 Gain over VT

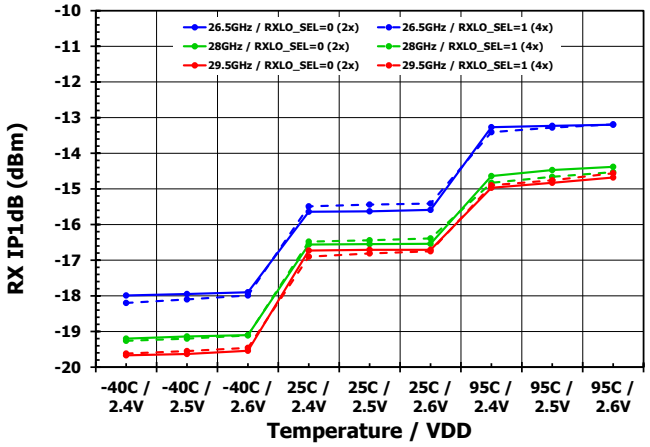

Figure 187. RX2 IP1dB over VT

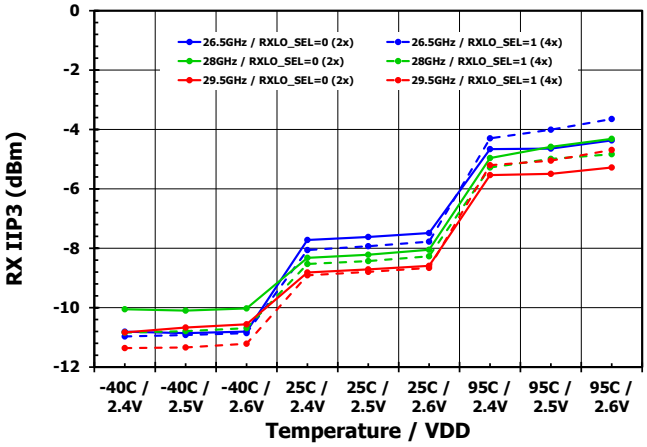

Figure 188. RX2 IIP3 over VT

4.4 5GHz IF/26GHz RF (Band H6)

4.4.1 TX Performance

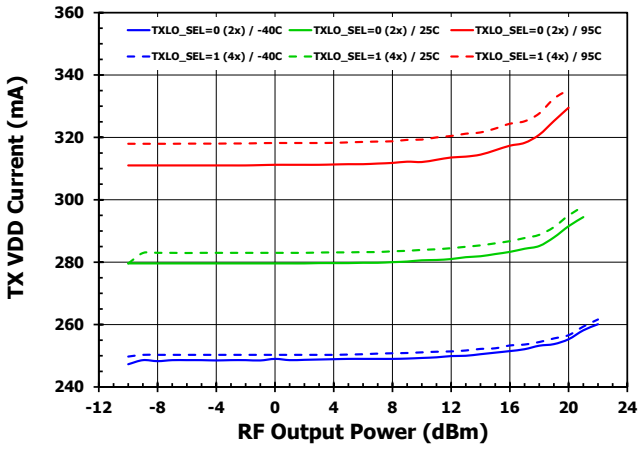

Figure 189. TX VDD Current

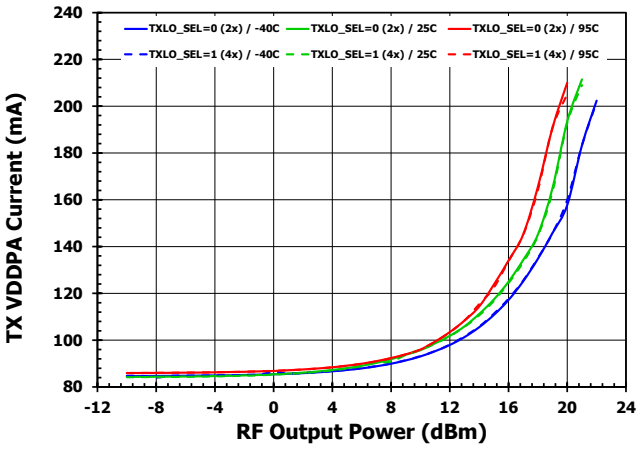

Figure 190. TX VDDPA Current

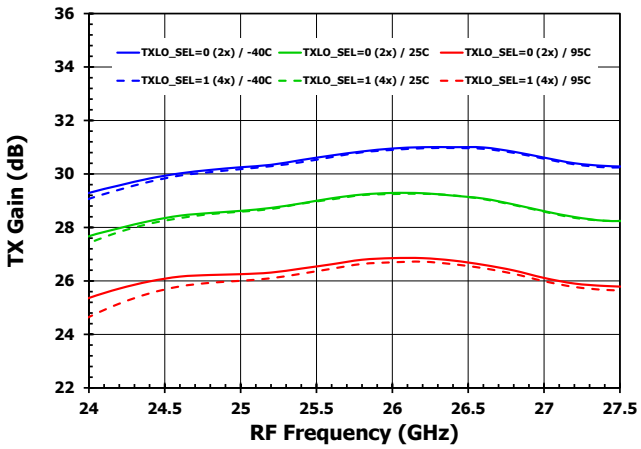

Figure 191. TX Gain

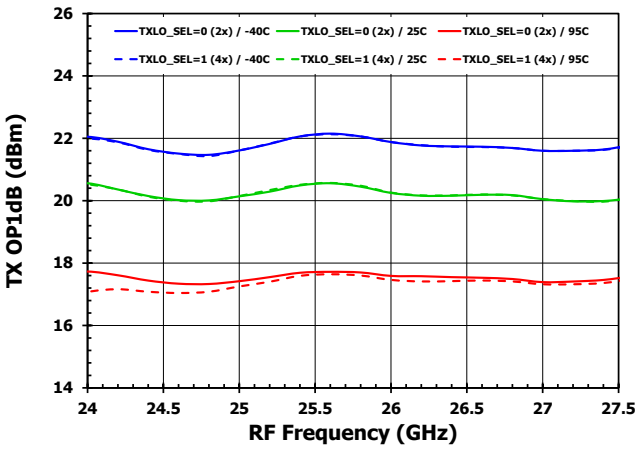

Figure 192. TX OP1dB

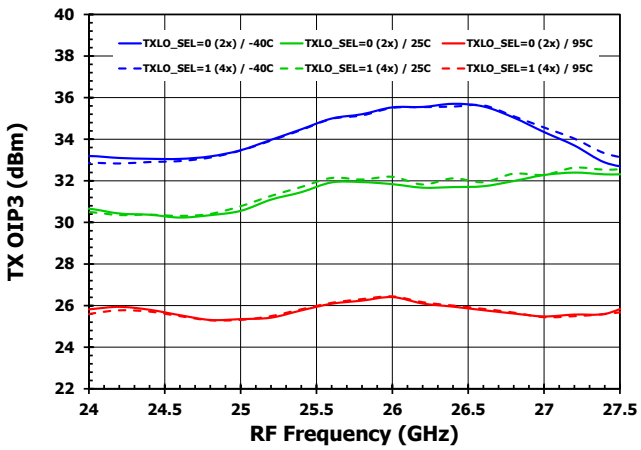

Figure 193. TX OIP3

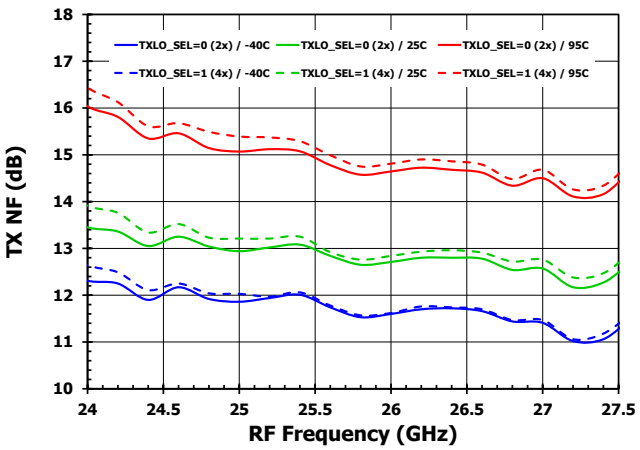

Figure 194. TX NF

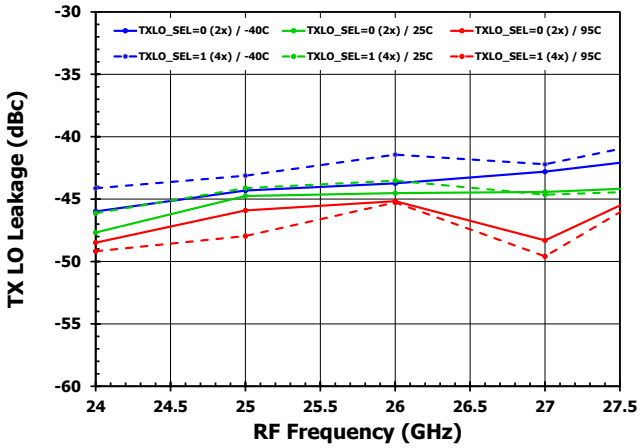

Figure 195. TX LO Leakage (uncalibrated)

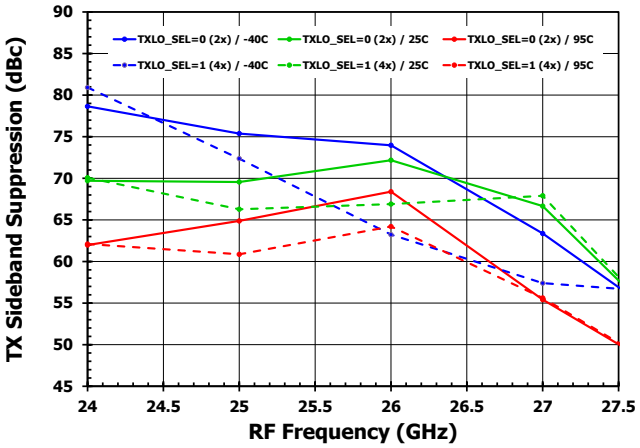

Figure 196. TX Sideband Suppression (uncalibrated)

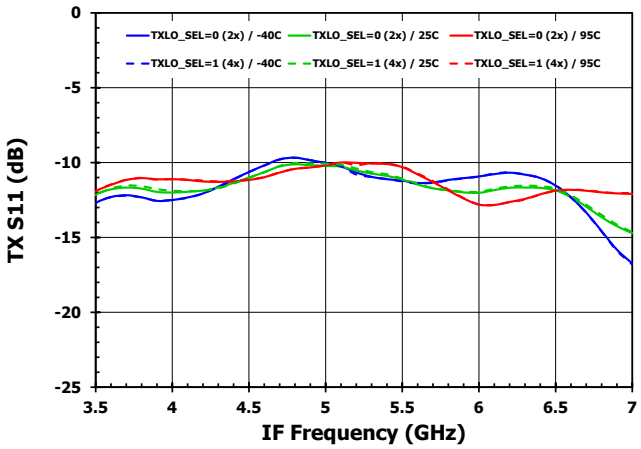

Figure 197. TX S11

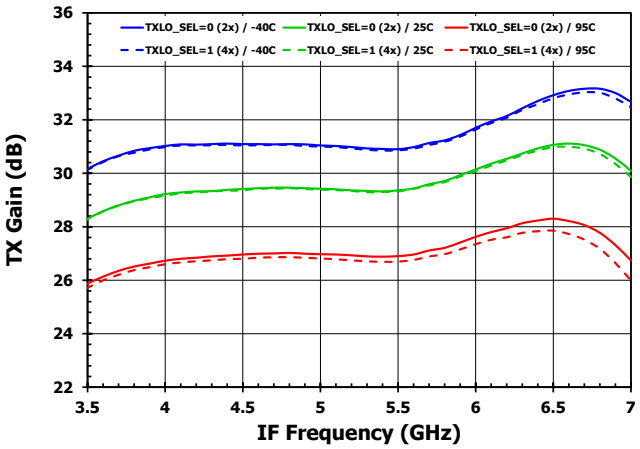

Figure 198. TX Gain vs IF

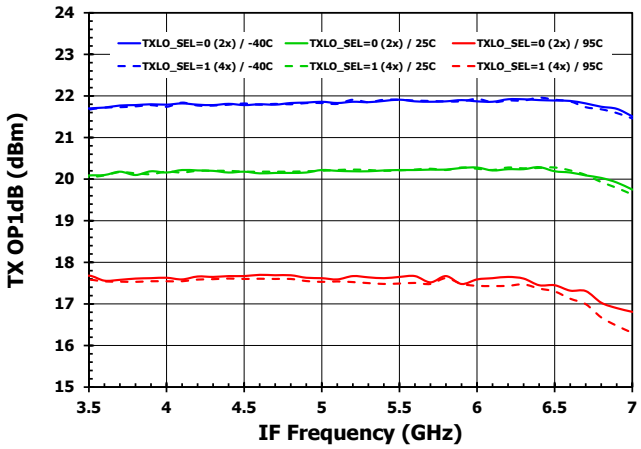

Figure 199. TX OP1dB vs IF

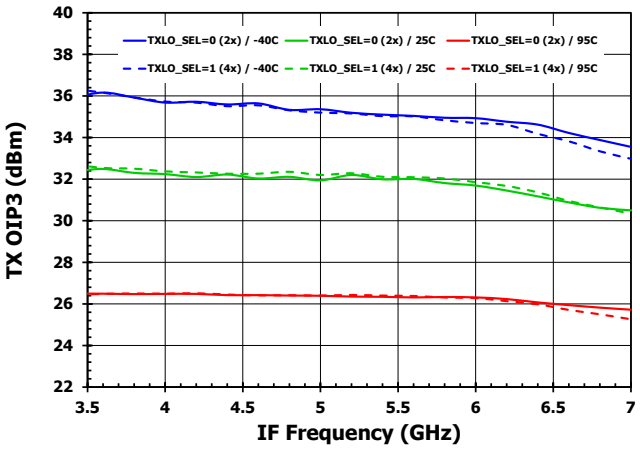

Figure 200. TX OIP3 vs IF

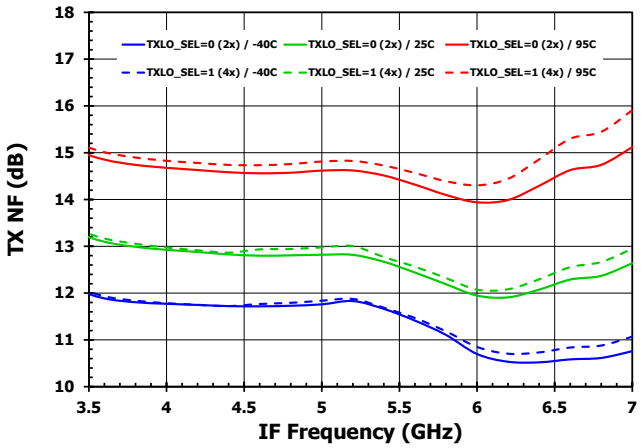

Figure 201. TX NF vs IF

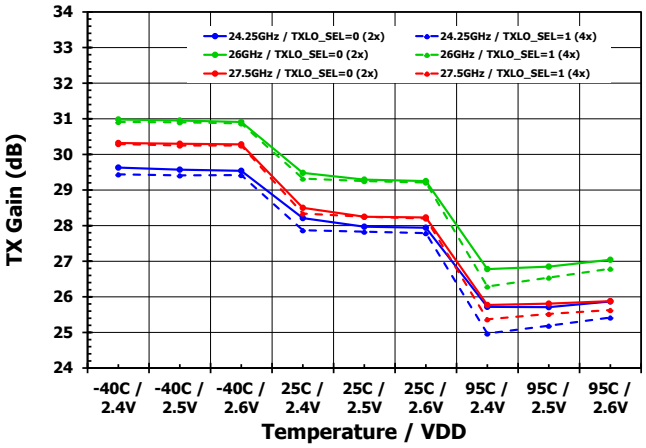

Figure 202. TX Gain over VT

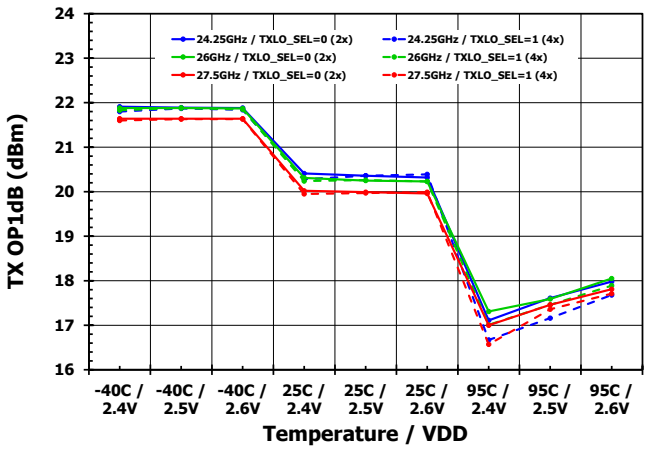

Figure 203. TX OP1dB over VT

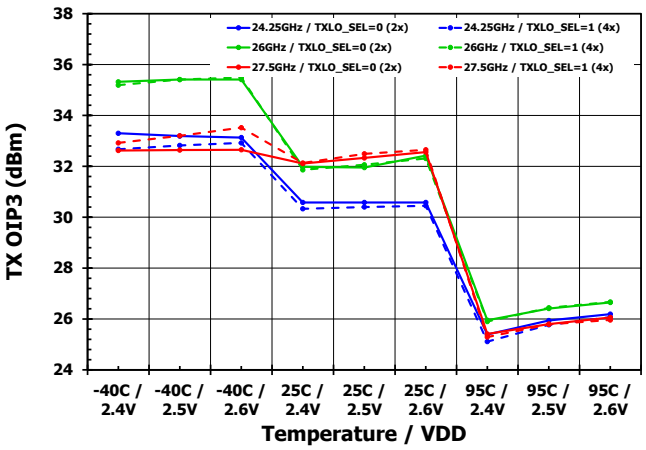

Figure 204. TX OIP3 over VT

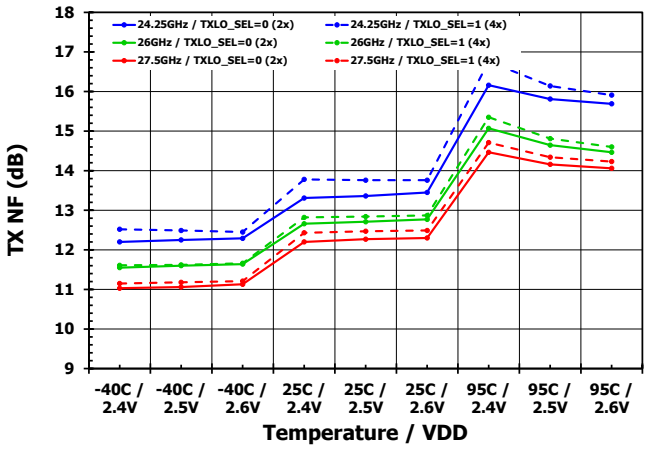

Figure 205. TX NF over VT

4.4.2 TX Performance – V_{DDPA} = 3.3V

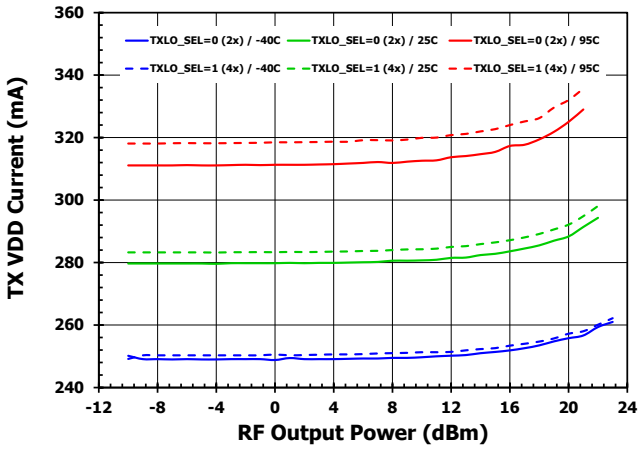

Figure 206. TX VDD Current

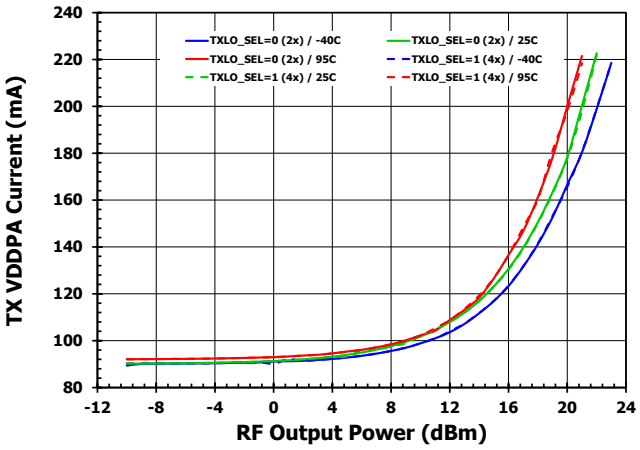

Figure 207. TX VDDPA Current

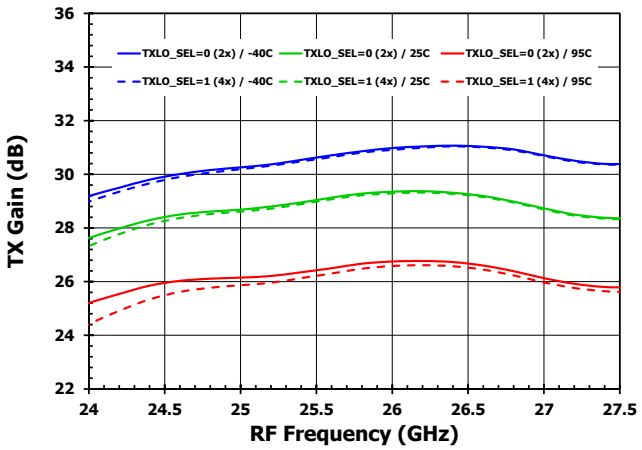

Figure 208. TX Gain

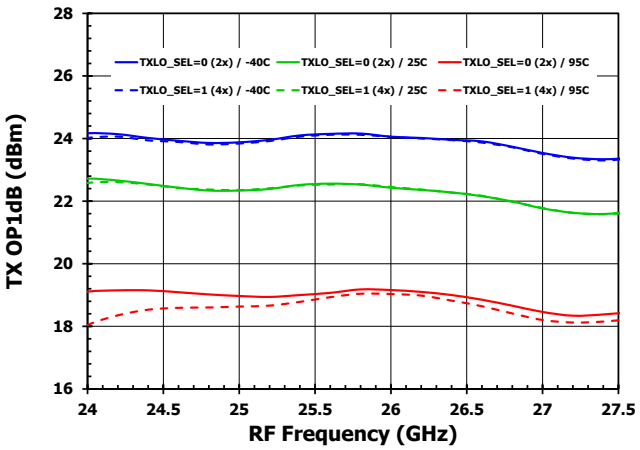

Figure 209. TX OP1dB

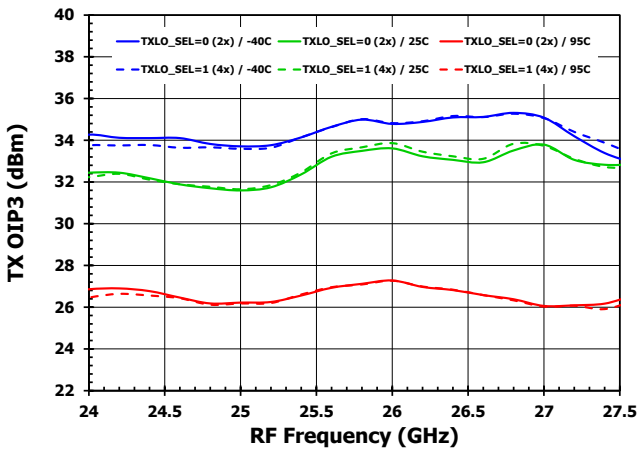

Figure 210. TX OIP3

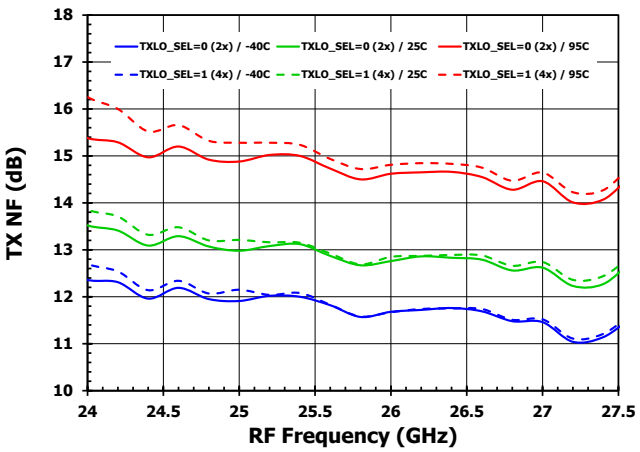

Figure 211. TX NF

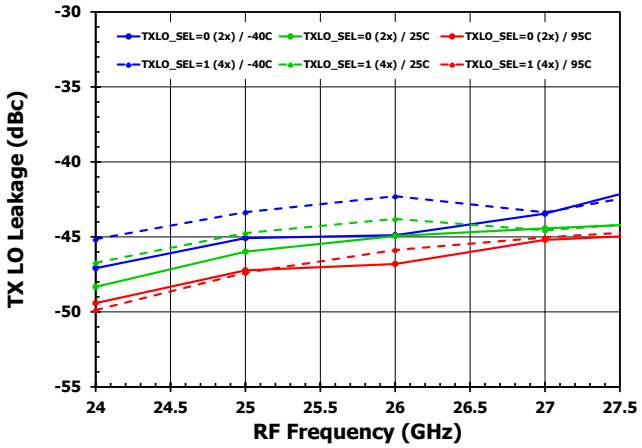

Figure 212. TX LO Leakage (uncalibrated)

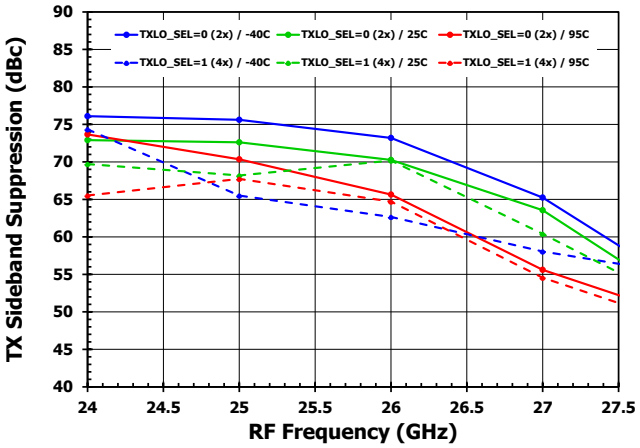

Figure 213. TX Sideband Suppression (uncalibrated)

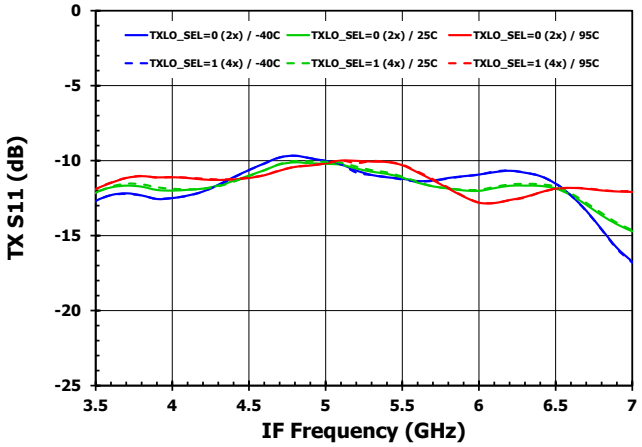

Figure 214. TX S11

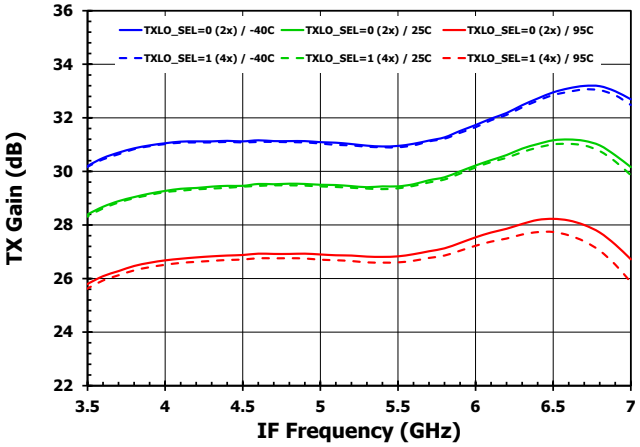

Figure 215. TX Gain vs IF

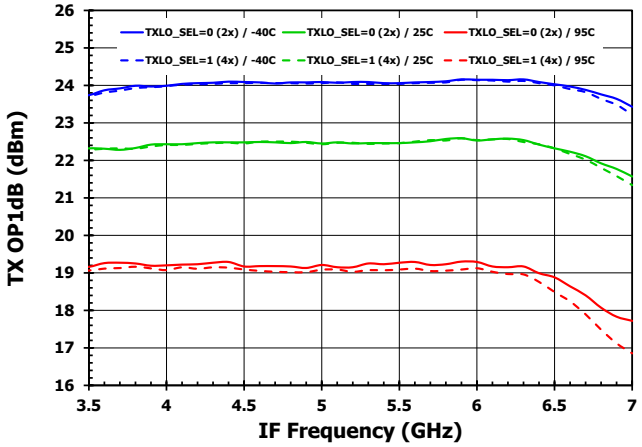

Figure 216. TX OP1dB vs IF

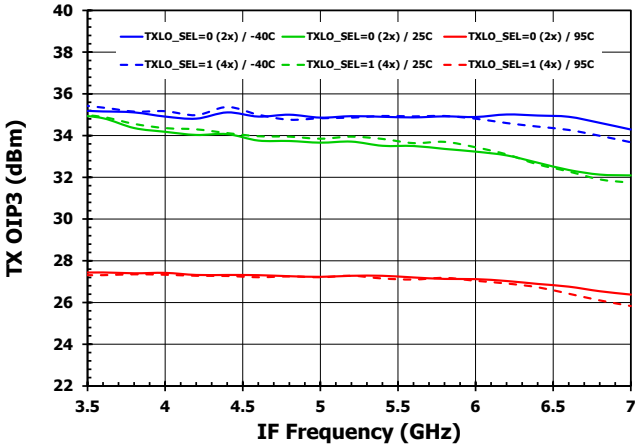

Figure 217. TX OIP3 vs IF

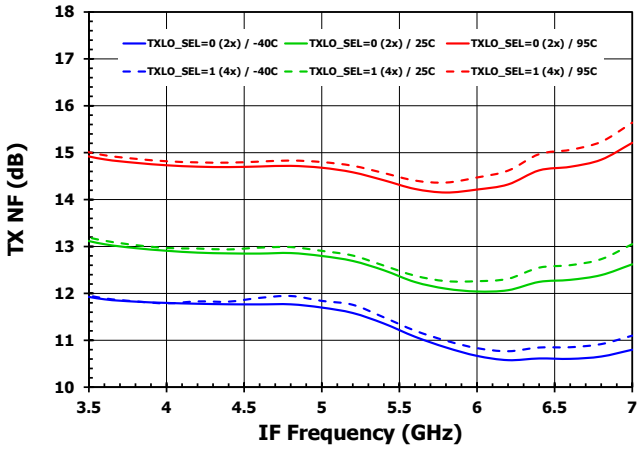

Figure 218. TX NF vs IF

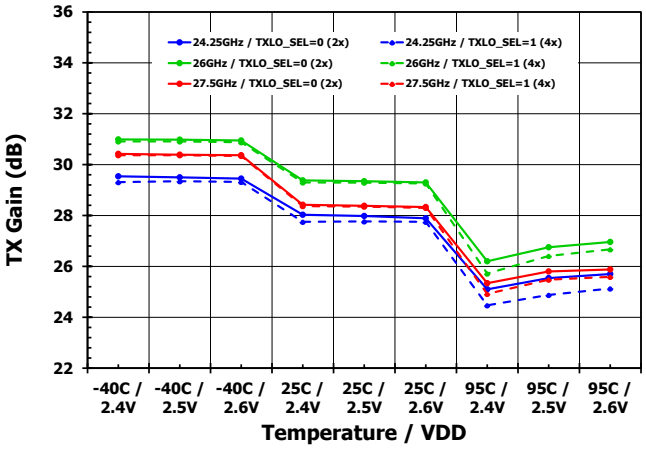

Figure 219. TX Gain over VT

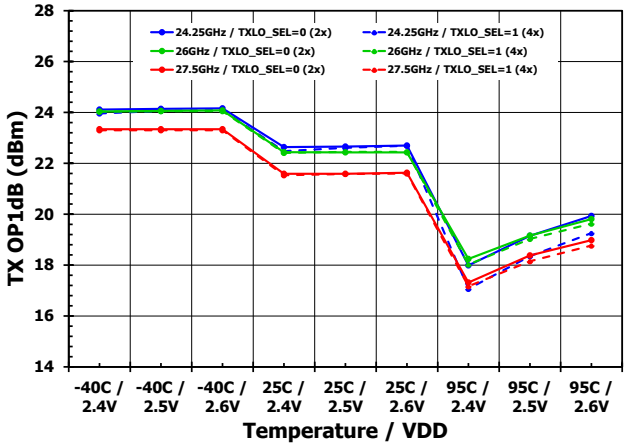

Figure 220. TX OP1dB over VT

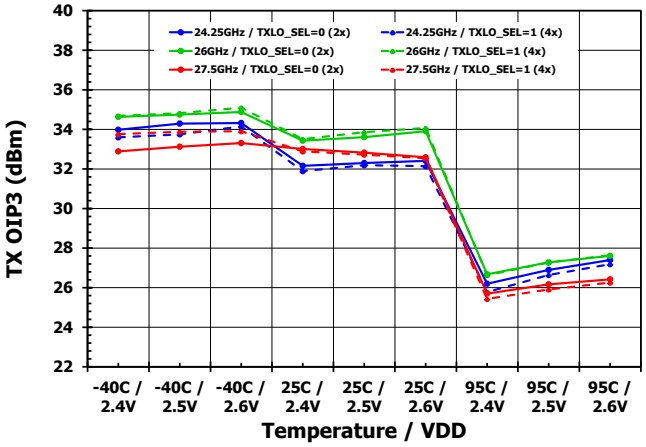

Figure 221. TX OIP3 over VT

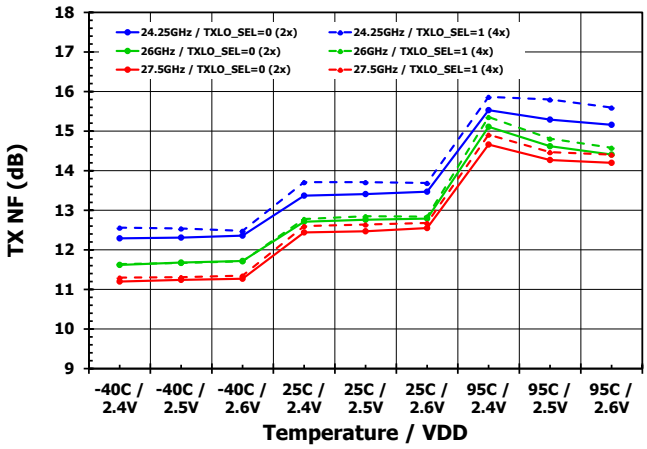

Figure 222. TX NF over VT

4.4.3 RX Performance

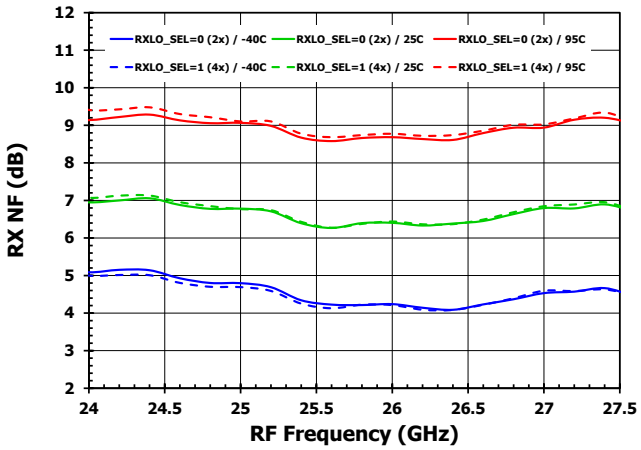

Figure 223. RX NF

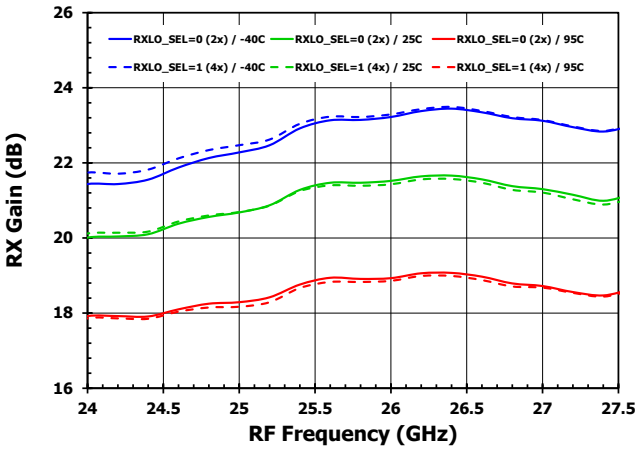

Figure 224. RX Gain

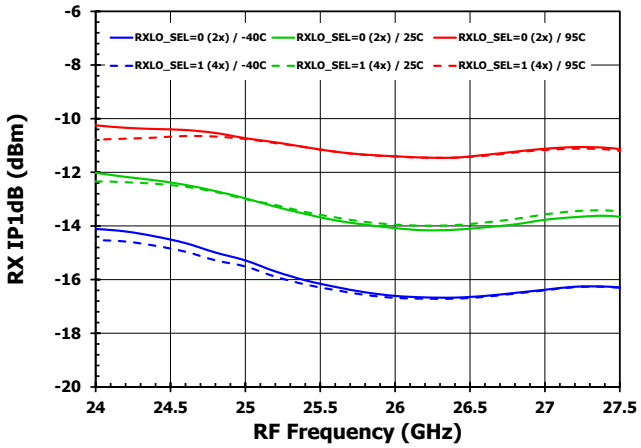

Figure 225. RX IP1dB

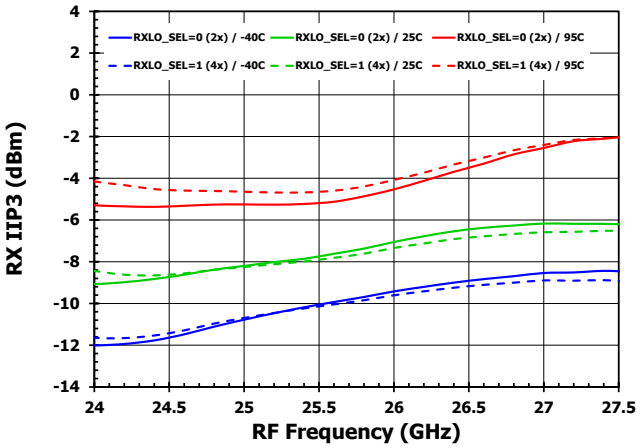

Figure 226. RX IIP3

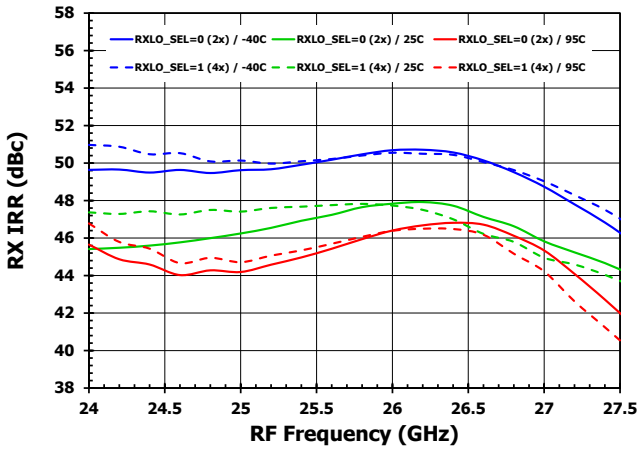

Figure 227. RX Image Rejection Ratio (uncalibrated)

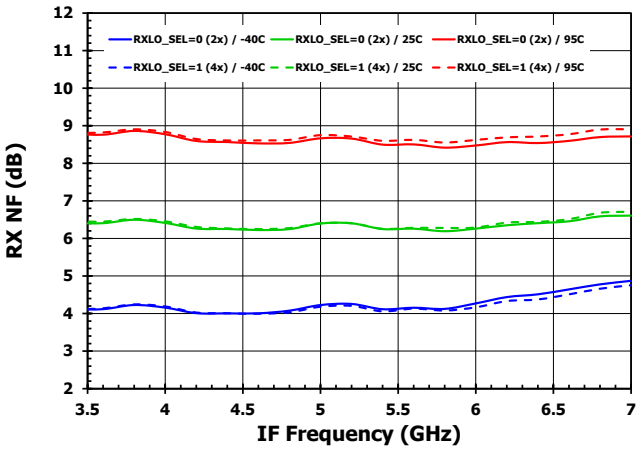

Figure 228. RX NF vs IF

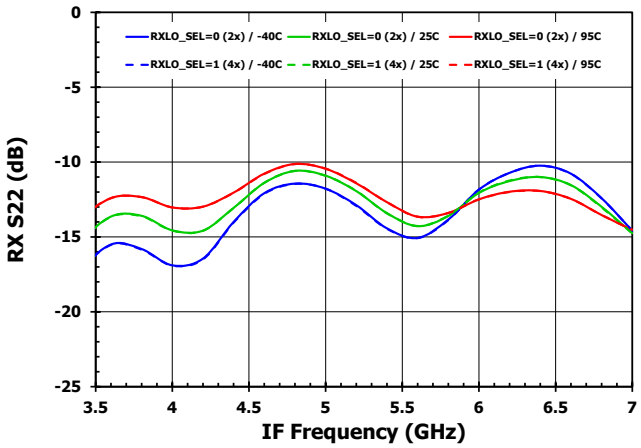

Figure 229. RX S22 vs IF

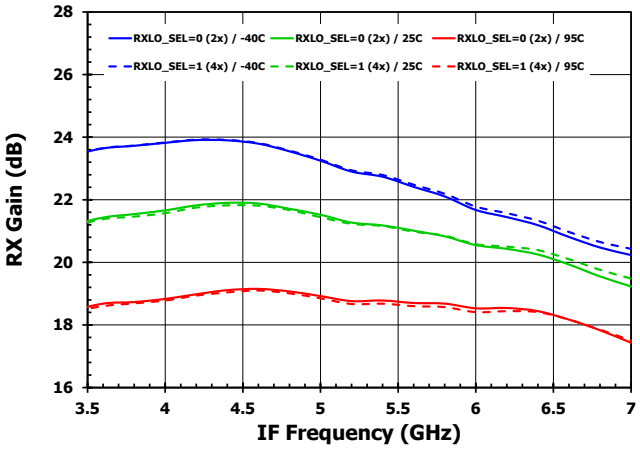

Figure 230. RX Gain vs IF

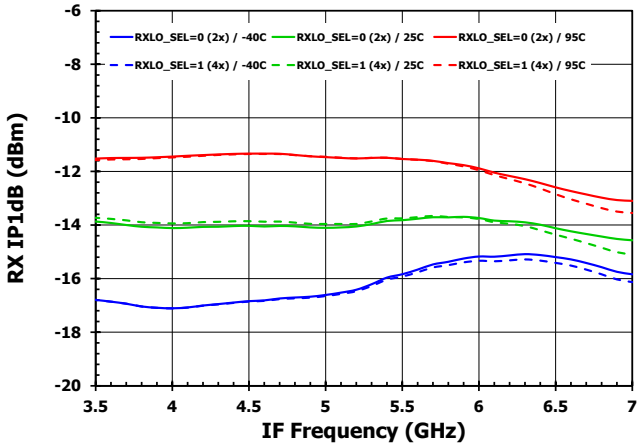

Figure 231. RX IP1dB vs IF

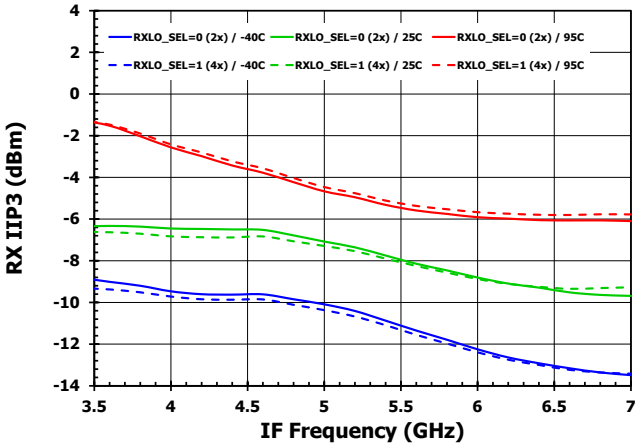

Figure 232. RX IIP3 vs IF

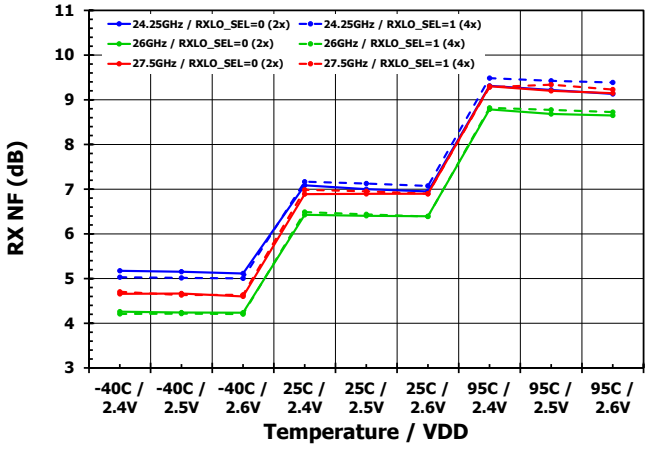

Figure 233. RX NF over VT

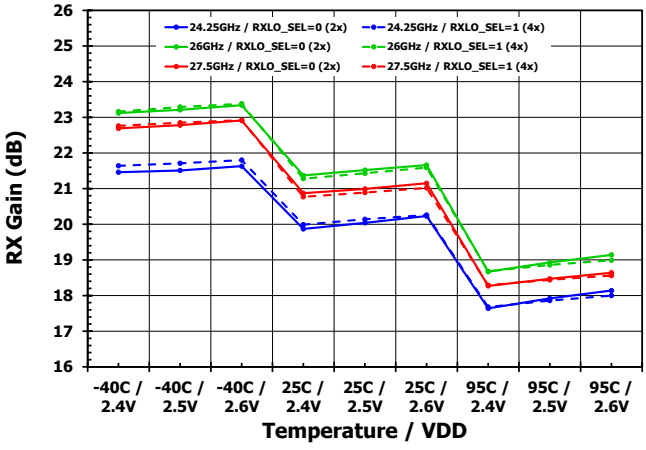

Figure 234. RX Gain over VT

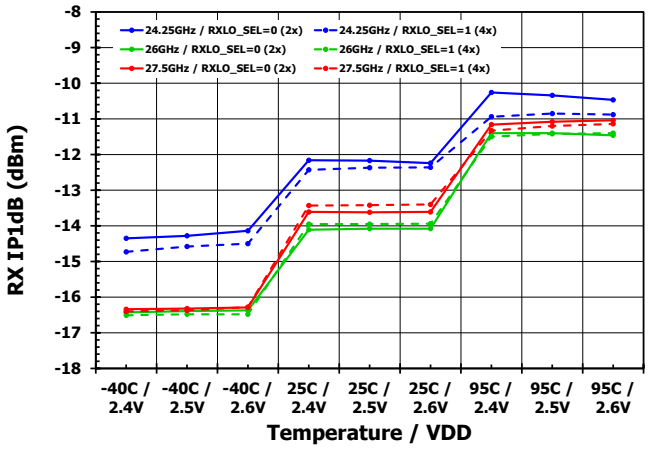

Figure 235. RX IP1dB over VT

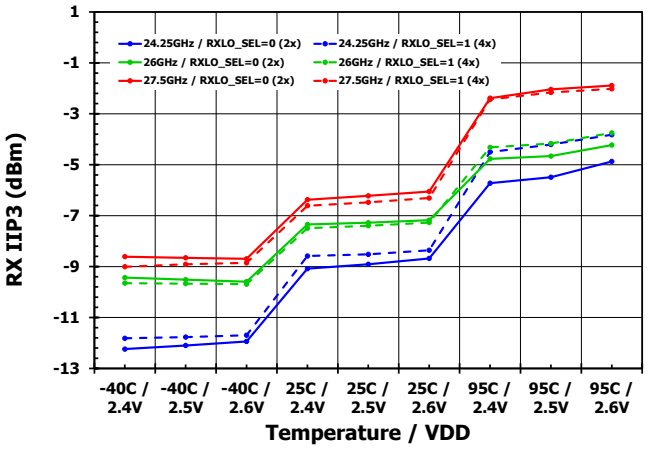

Figure 236. RX IIP3 over VT

4.4.4 RX Performance – High Linearity Mode (Band H6h)

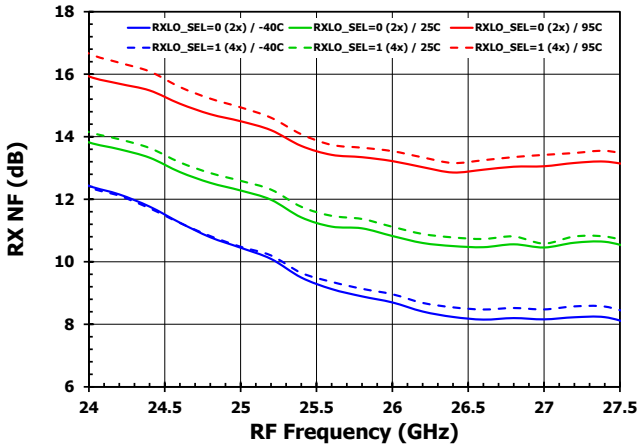

Figure 237. RX NF

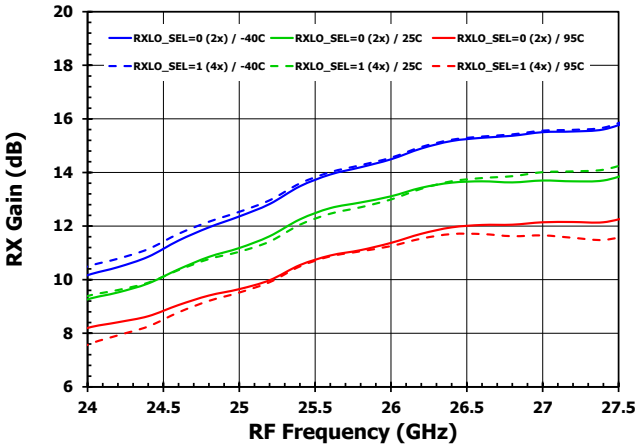

Figure 238. RX Gain

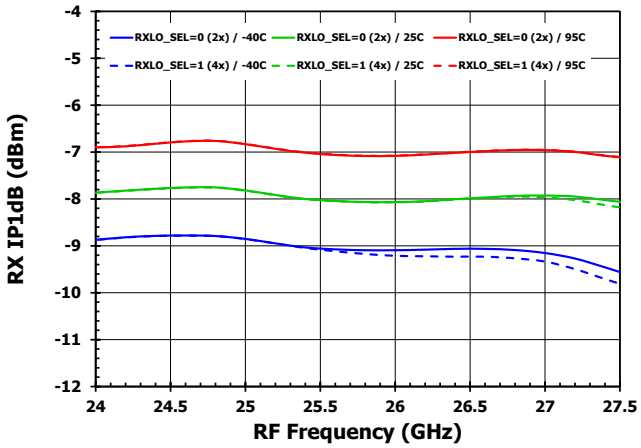

Figure 239. RX IP1dB

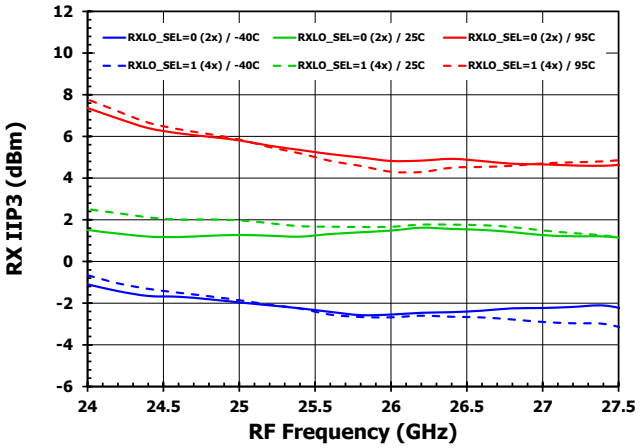

Figure 240. RX IIP3

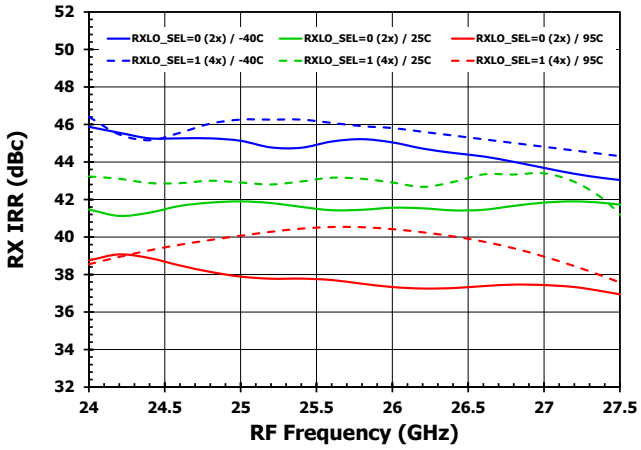

Figure 241. RX Image Rejection Ratio (uncalibrated)

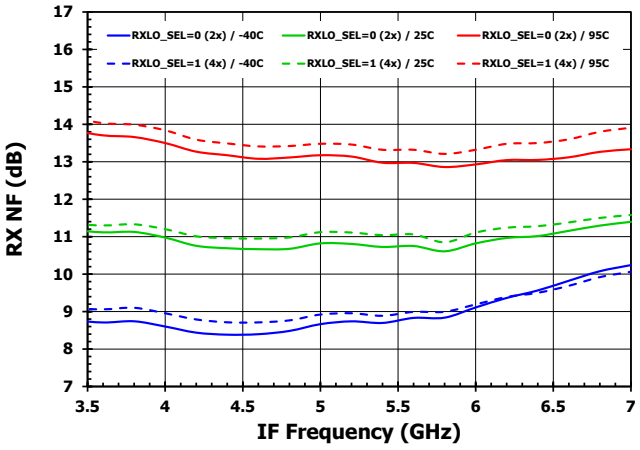

Figure 242. RX NF vs IF

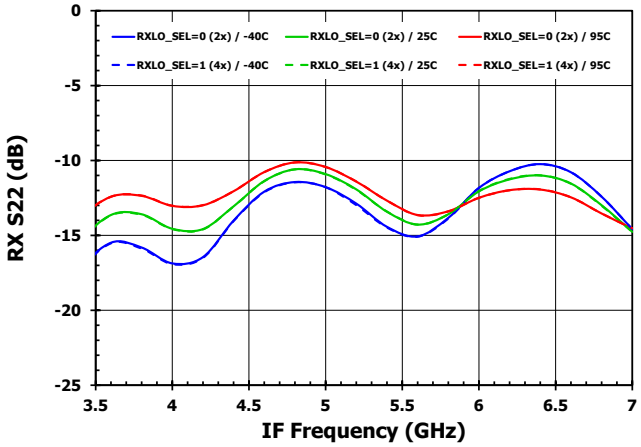

Figure 243. RX S22 vs IF

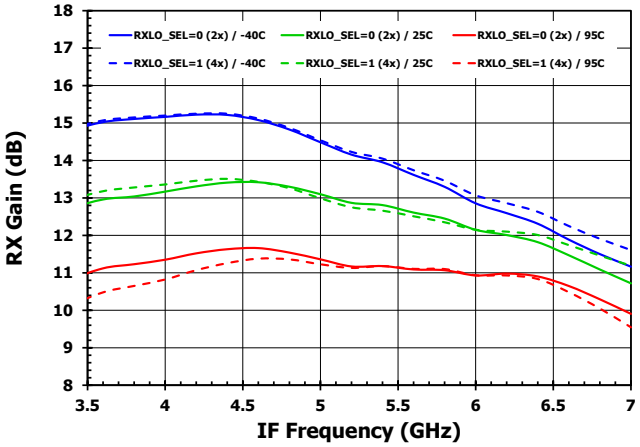

Figure 244. RX Gain vs IF

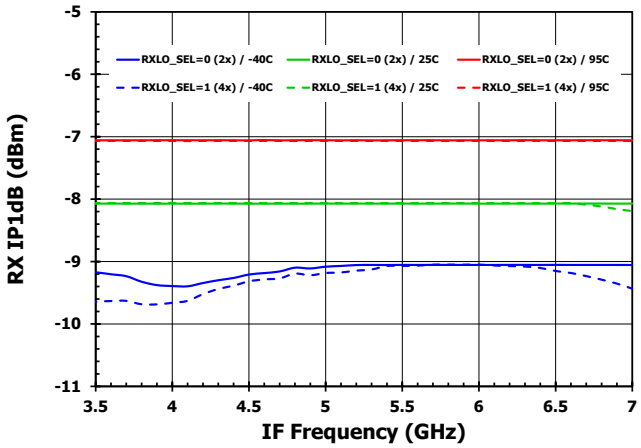

Figure 245. RX IP1dB vs IF

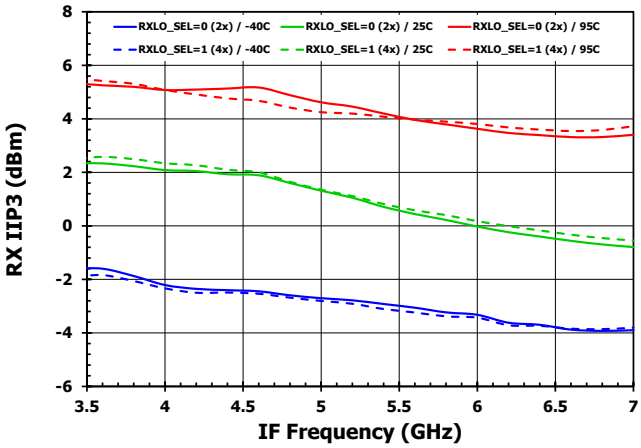

Figure 246. RX IIP3 vs IF

4.4.5 RX Performance – RX2 Path

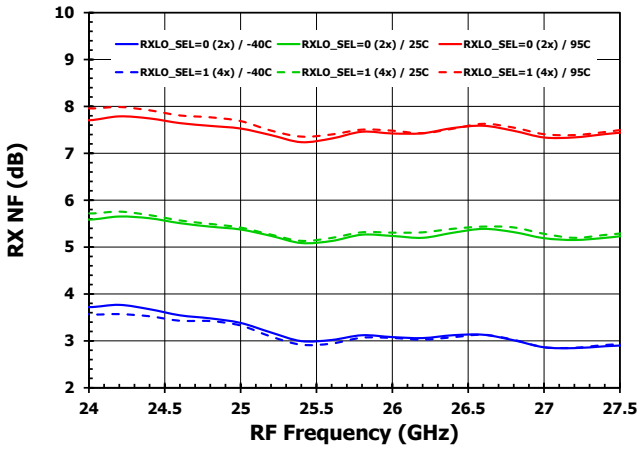

Figure 247. RX2 NF

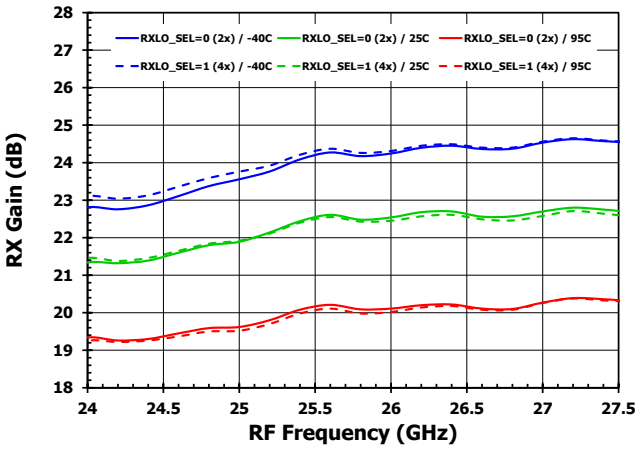

Figure 248. RX2 Gain

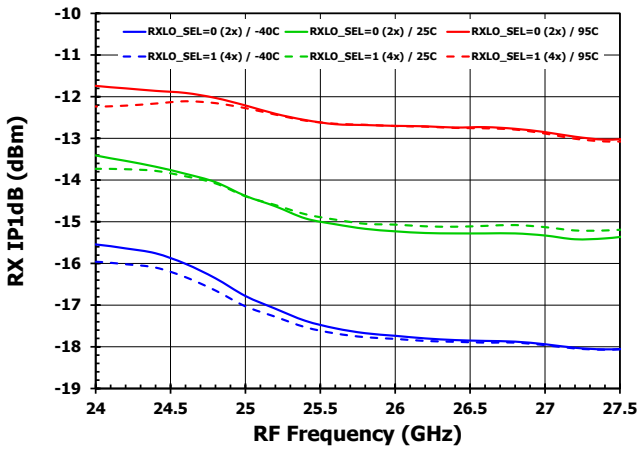

Figure 249. RX2 IP1dB

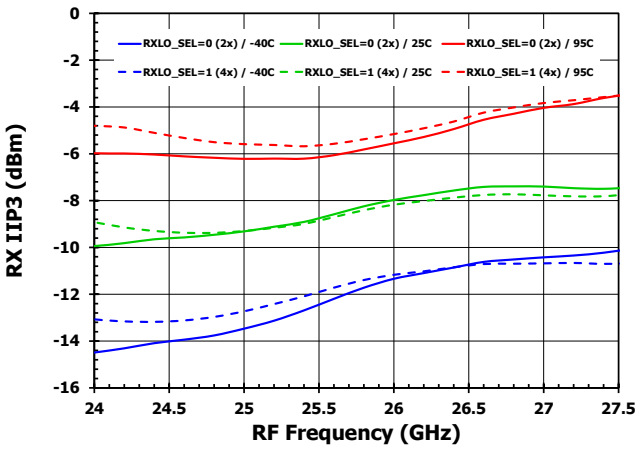

Figure 250. RX2 IIP3

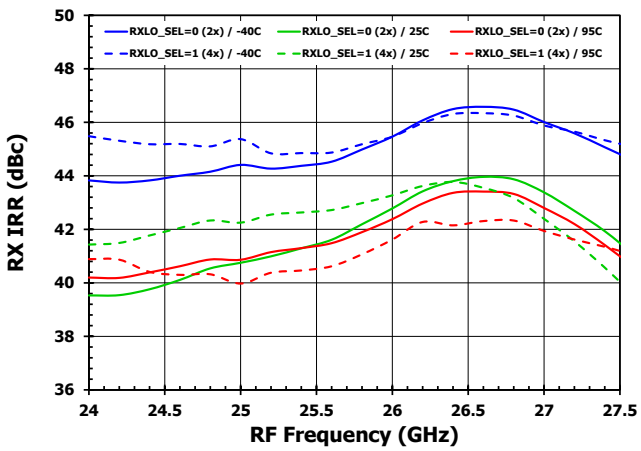

Figure 251. RX2 Image Rejection Ratio (uncalibrated)

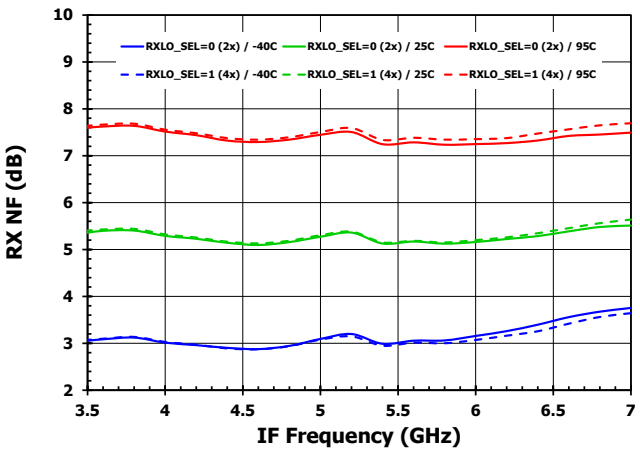

Figure 252. RX2 NF vs IF

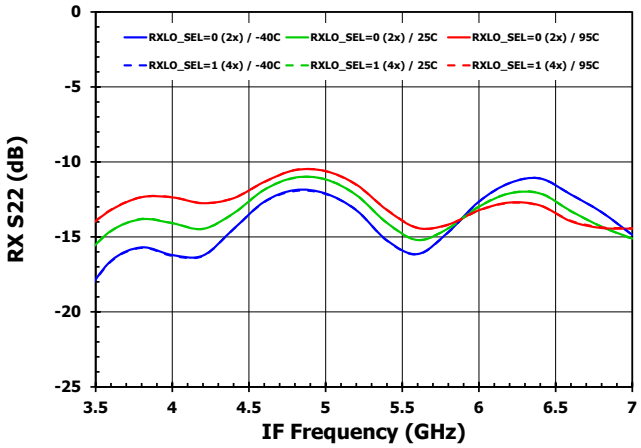

Figure 253. RX2 S22 vs IF

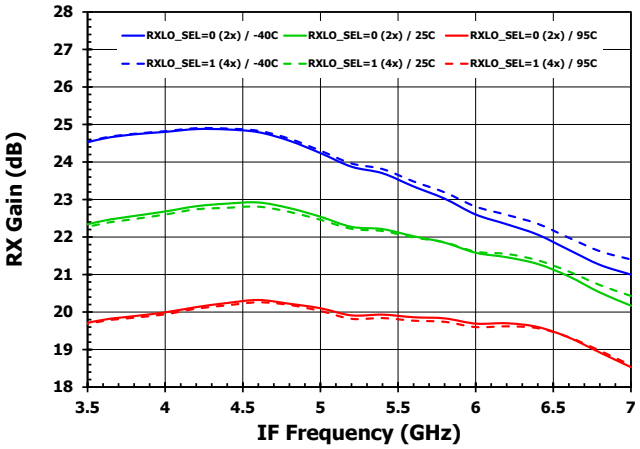

Figure 254. RX2 Gain vs IF

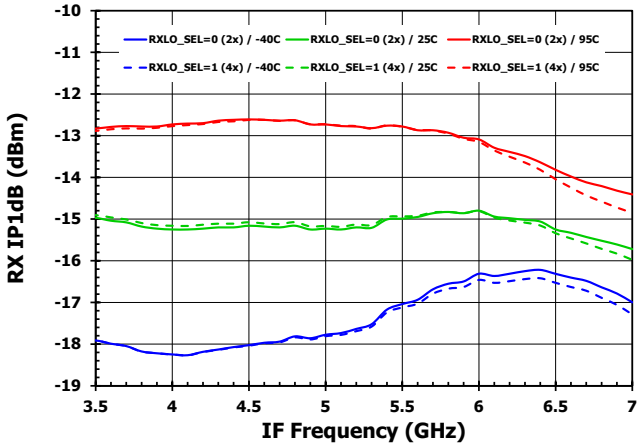

Figure 255. RX2 IP1dB vs IF

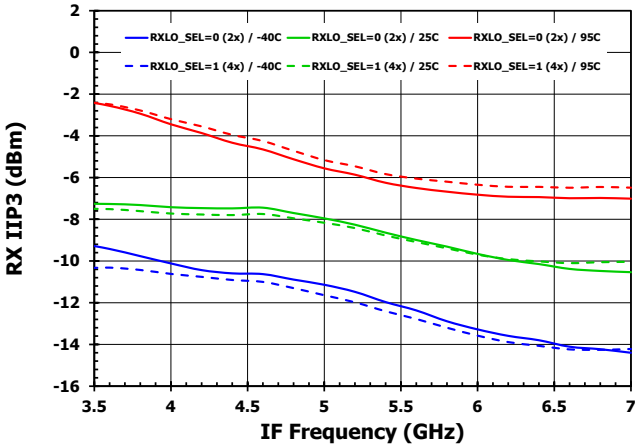

Figure 256. RX2 IIP3 vs IF

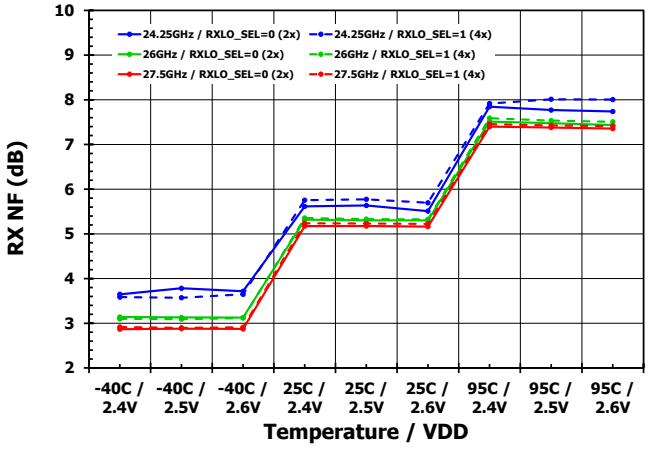

Figure 257. RX2 NF over VT

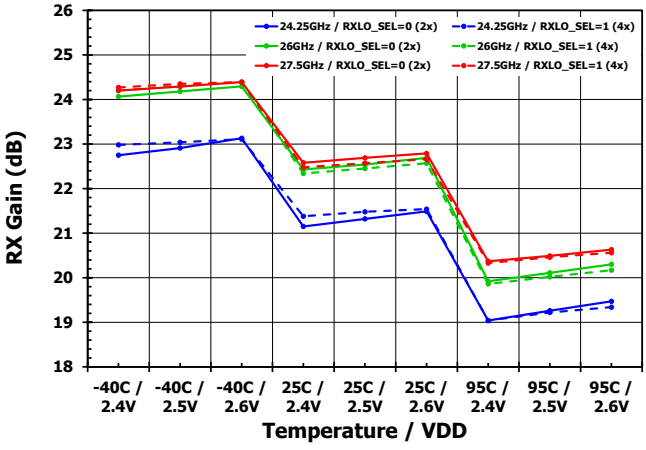

Figure 258. RX2 Gain over VT

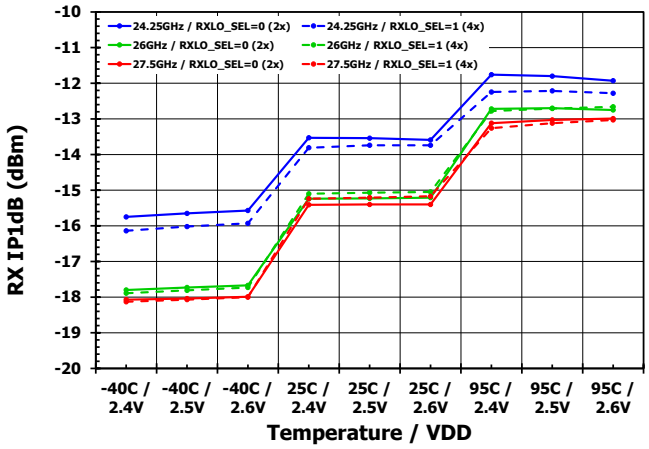

Figure 259. RX2 IP1dB over VT

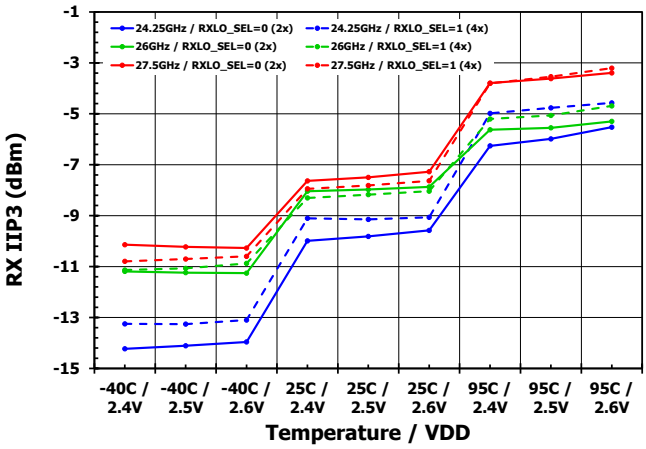

Figure 260. RX2 IIP3 over VT

4.5 3GHz IF/28GHz RF (Band L8)

4.5.1 TX Performance

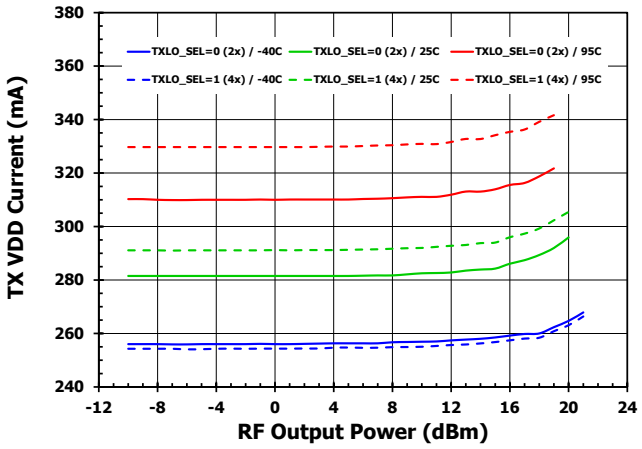

Figure 261. TX VDD Current

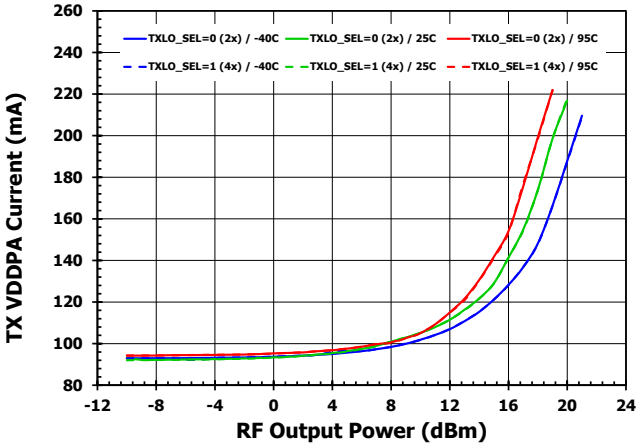

Figure 262. TX VDDPA Current

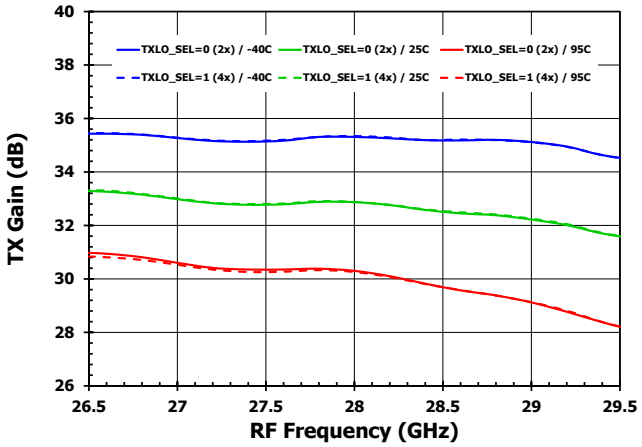

Figure 263. TX Gain

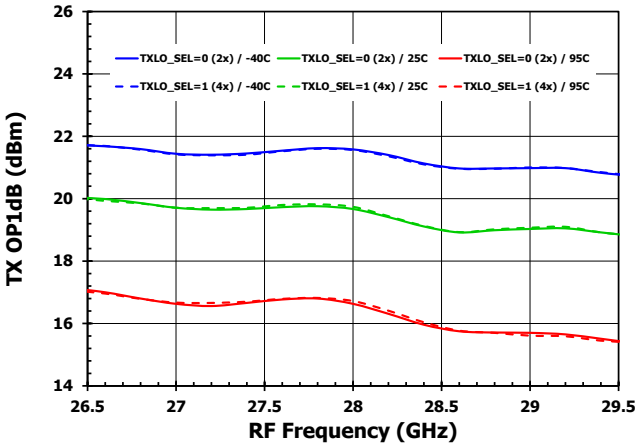

Figure 264. TX OP1dB

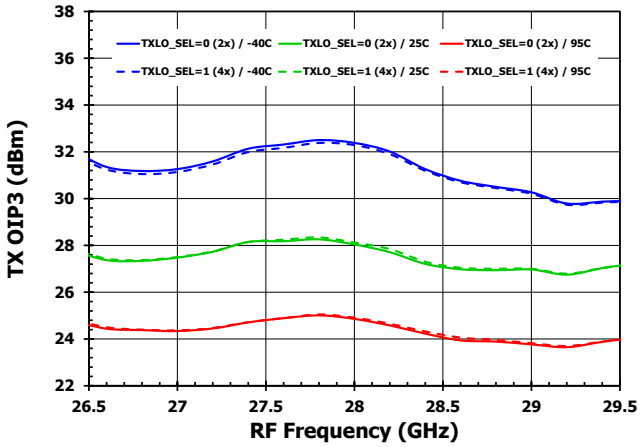

Figure 265. TX OIP3

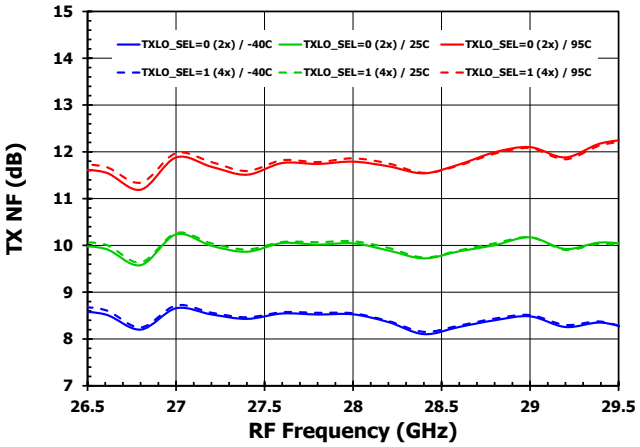

Figure 266. TX NF

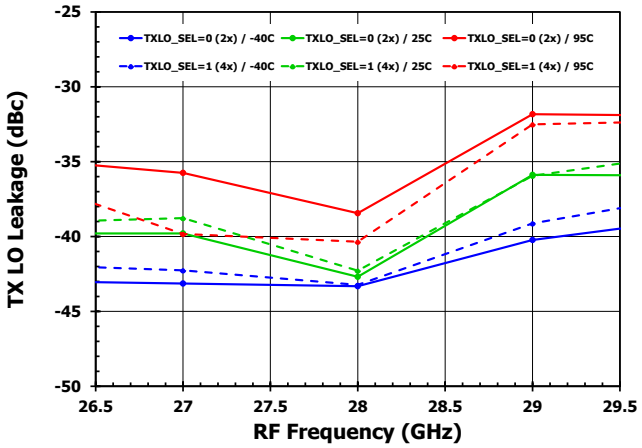

Figure 267. TX LO Leakage (uncalibrated)

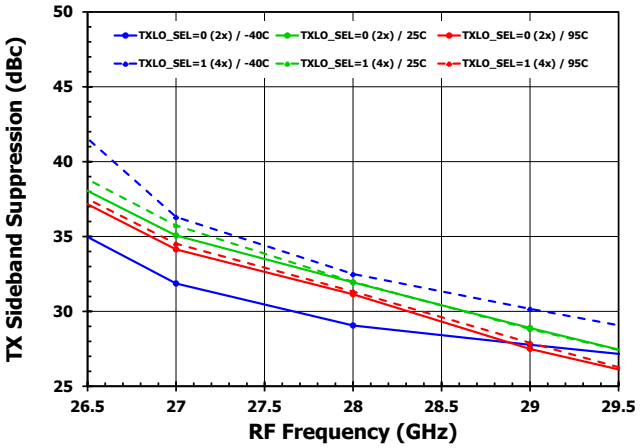

Figure 268. TX Sideband Suppression (uncalibrated)

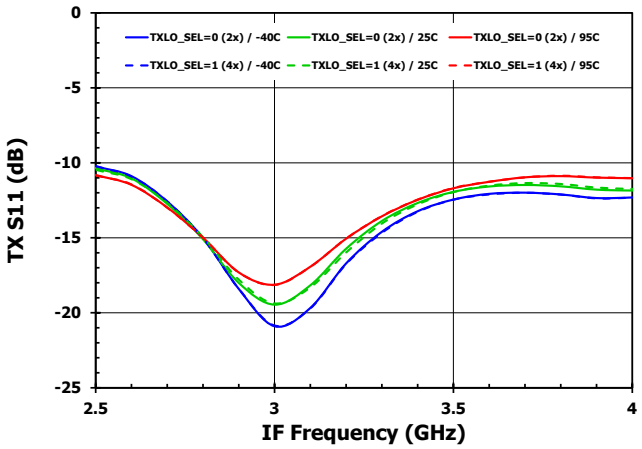

Figure 269. TX S11

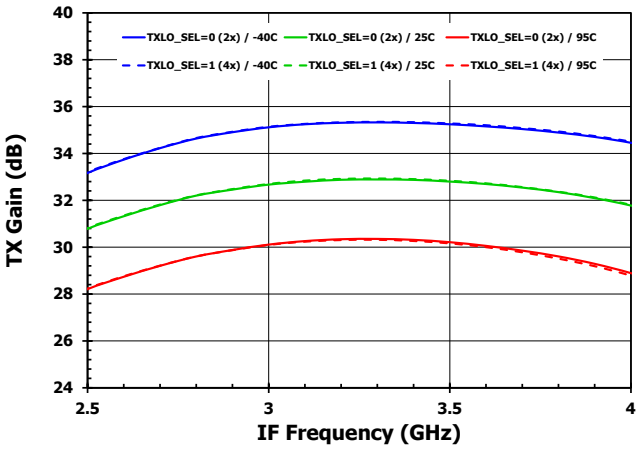

Figure 270. TX Gain vs IF

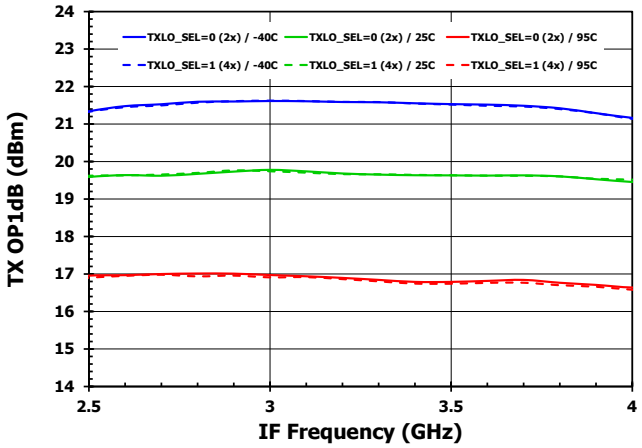

Figure 271. TX OP1dB vs IF

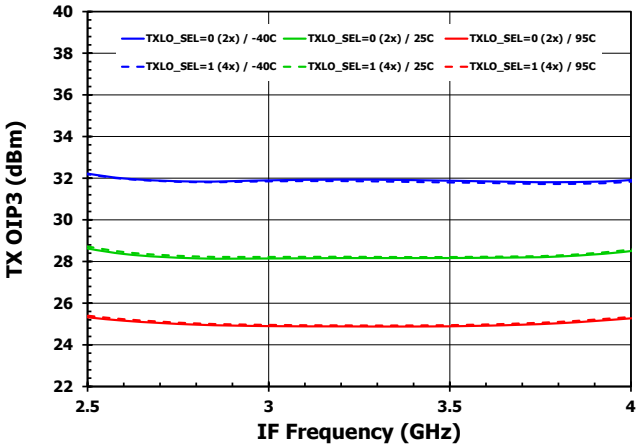

Figure 272. TX OIP3 vs IF

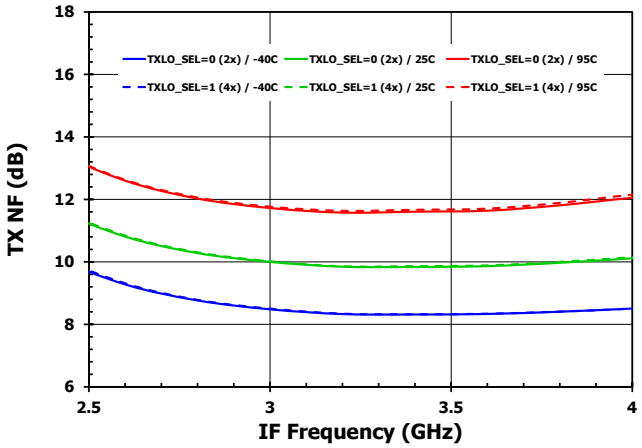

Figure 273. TX NF vs IF

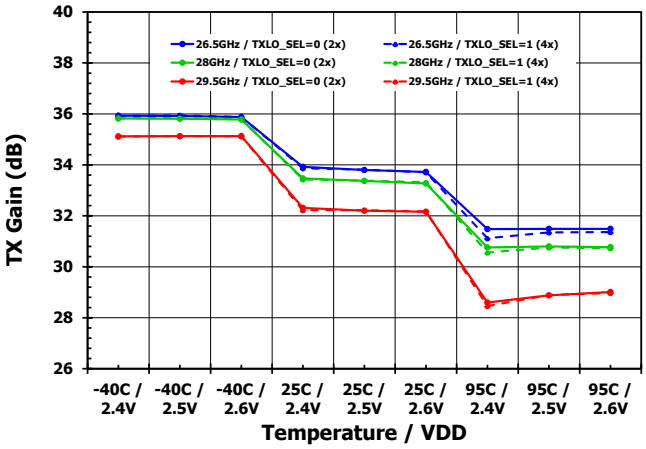

Figure 274. TX Gain over VT

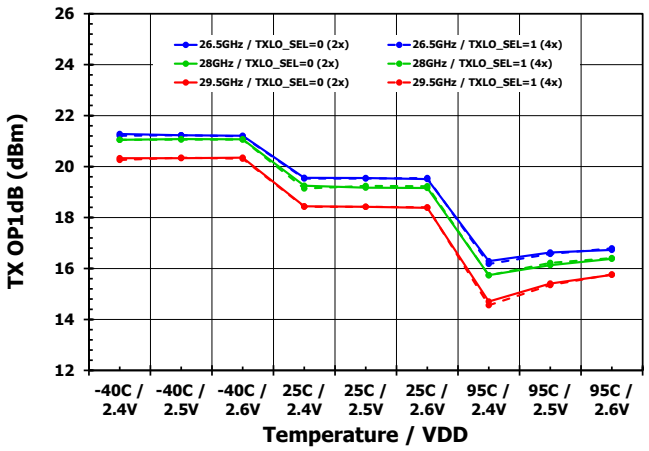

Figure 275. TX OP1dB over VT

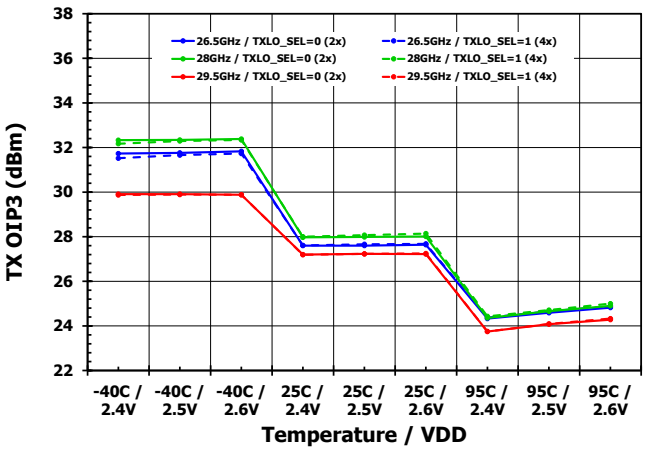

Figure 276. TX OIP3 over VT

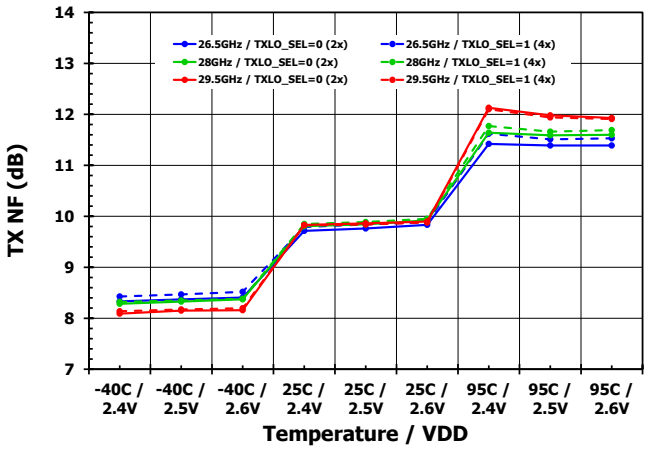

Figure 277. TX NF over VT

4.5.2 TX Performance – V_{DDPA} = 3.3V

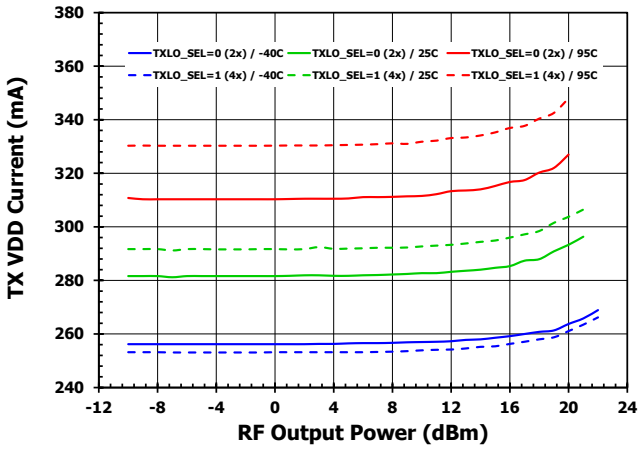

Figure 278. TX VDD Current

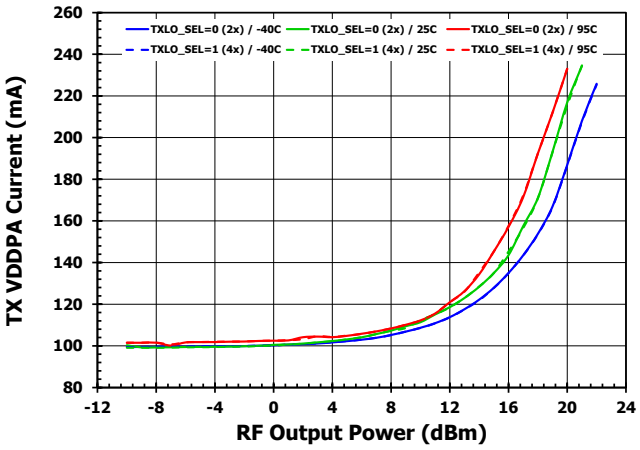

Figure 279. TX VDDPA Current

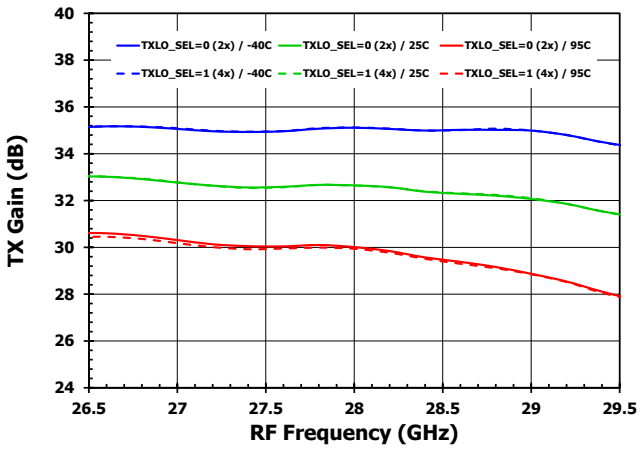

Figure 280. TX Gain

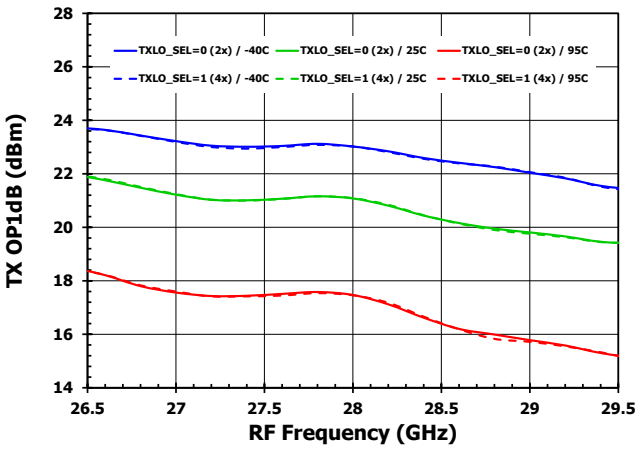

Figure 281. TX OP1dB

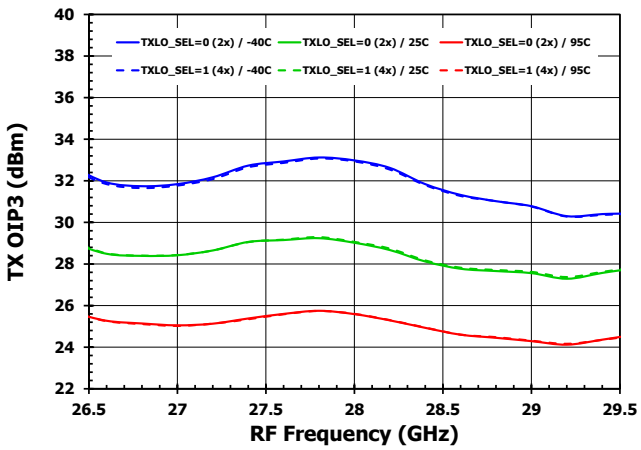

Figure 282. TX OIP3

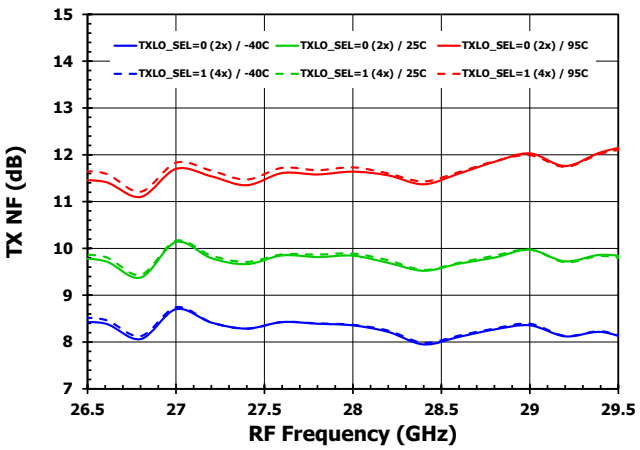

Figure 283. TX NF

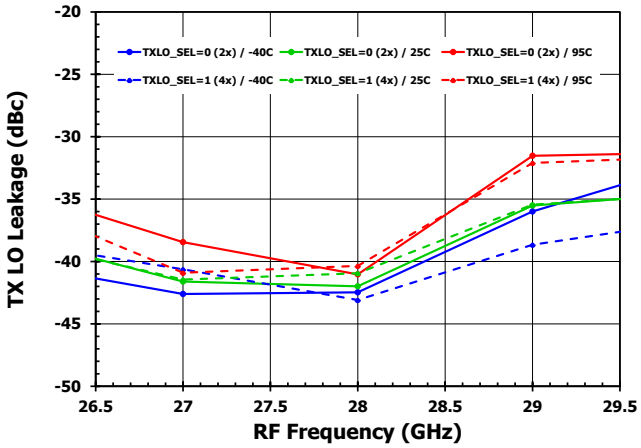

Figure 284. TX LO Leakage (uncalibrated)

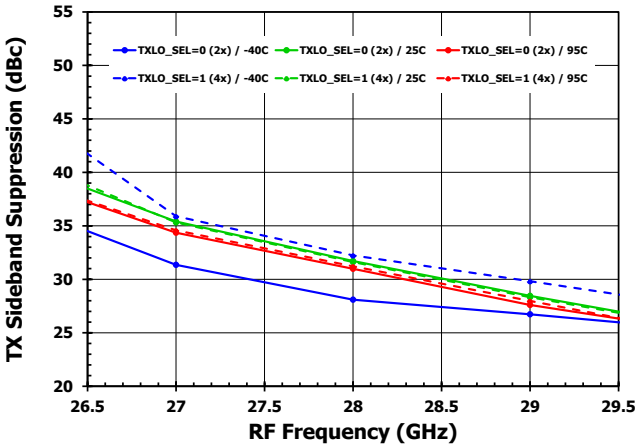

Figure 285. TX Sideband Suppression (uncalibrated)

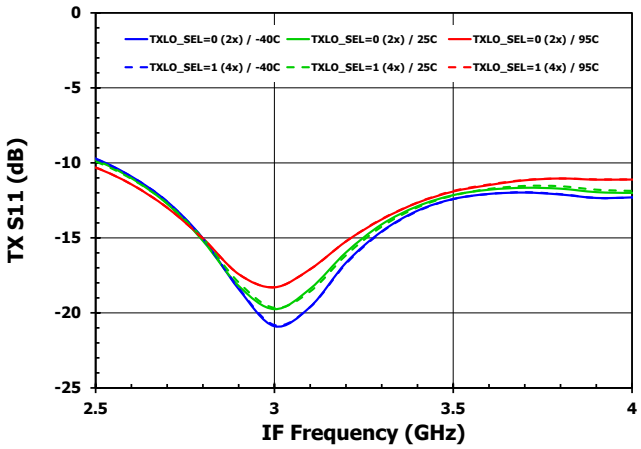

Figure 286. TX S11

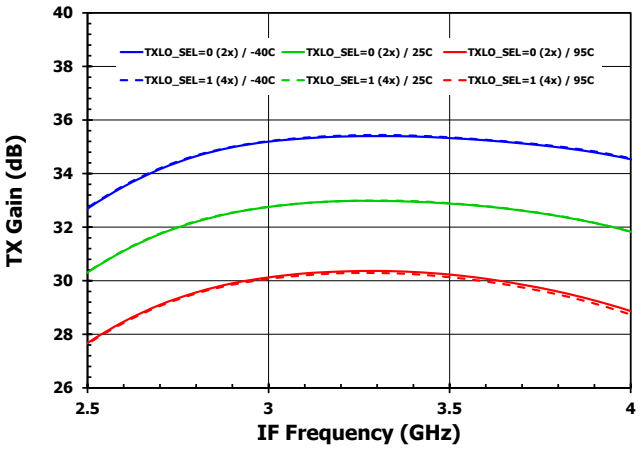

Figure 287. TX Gain vs IF

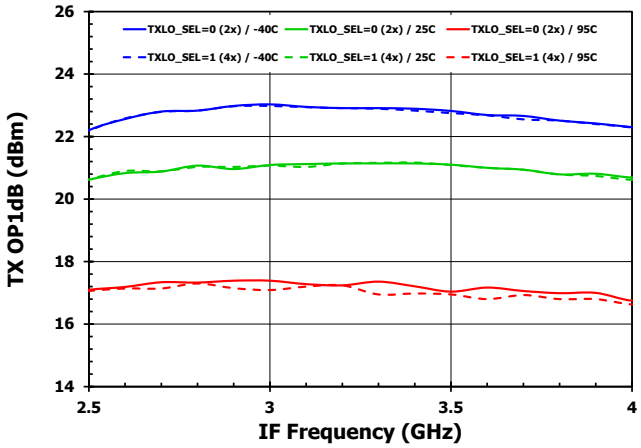

Figure 288. TX OP1dB vs IF

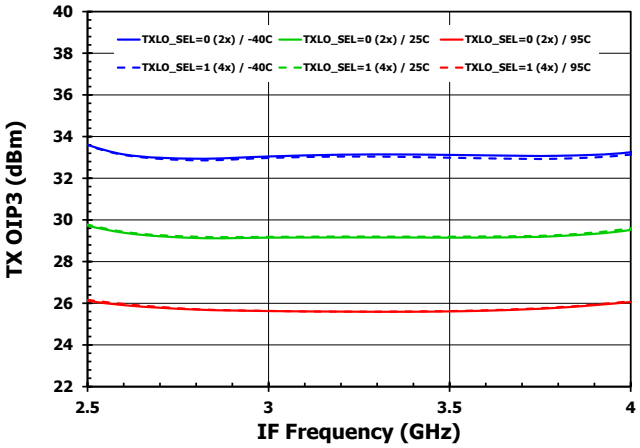

Figure 289. TX OIP3 vs IF

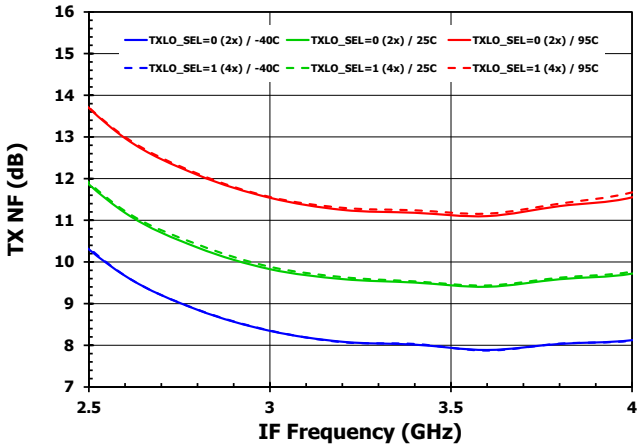

Figure 290. TX NF vs IF

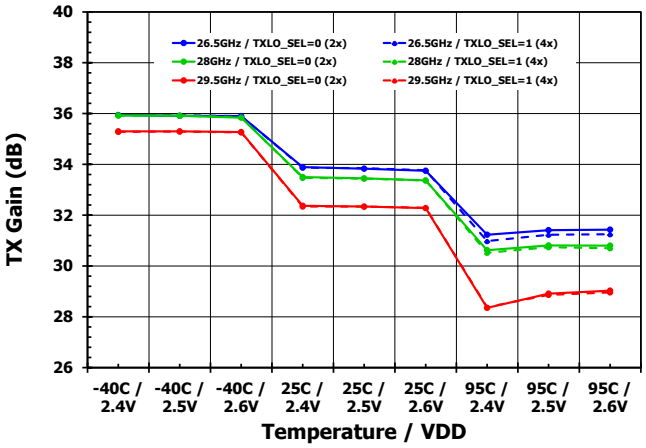

Figure 291. TX Gain over VT

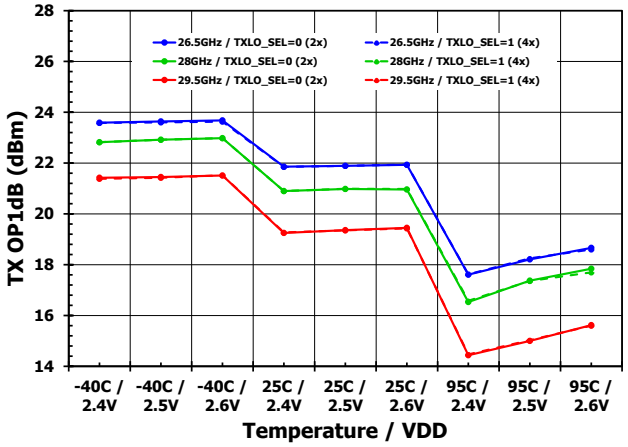

Figure 292. TX OP1dB over VT

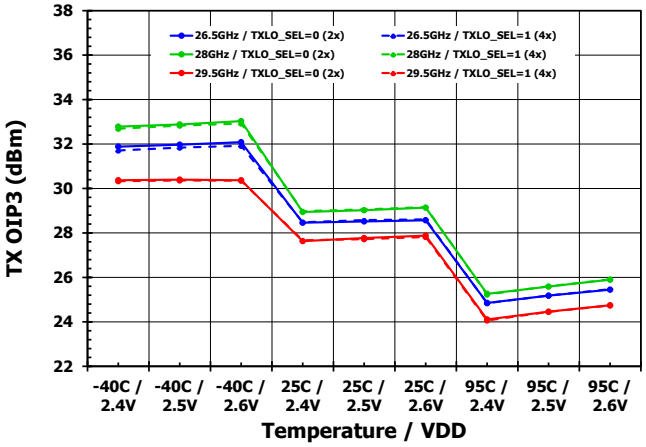

Figure 293. TX OIP3 over VT

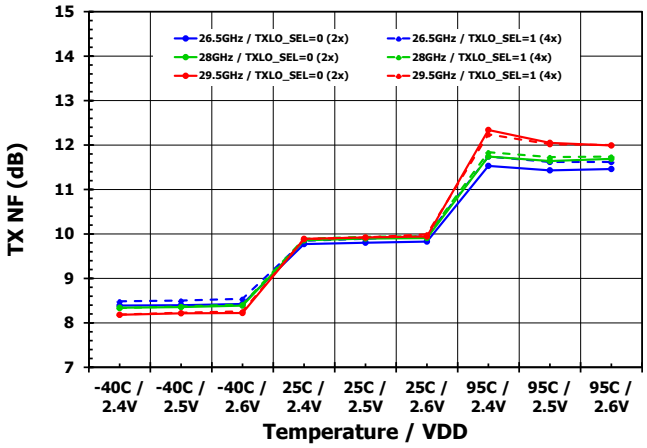

Figure 294. TX NF over VT

4.5.3 RX Performance

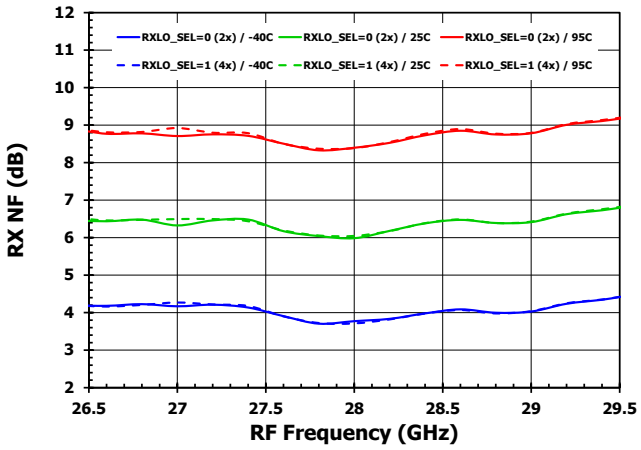

Figure 295. RX NF

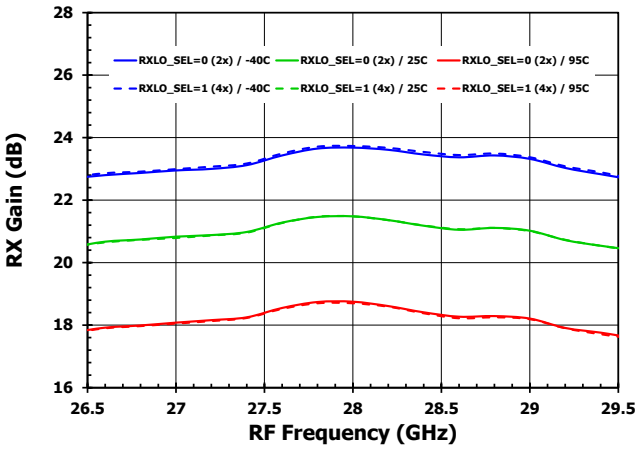

Figure 296. RX Gain

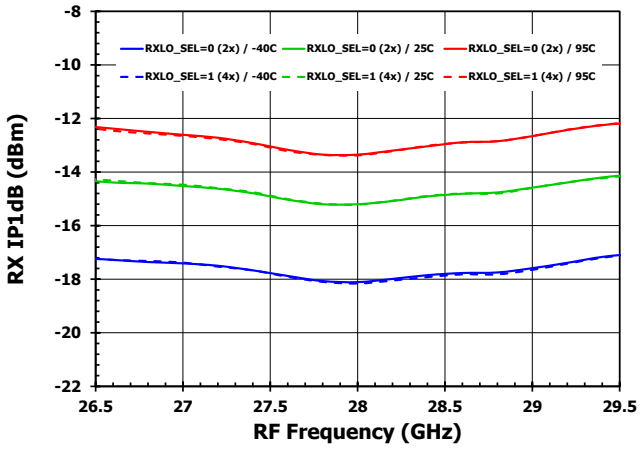

Figure 297. RX IP1dB

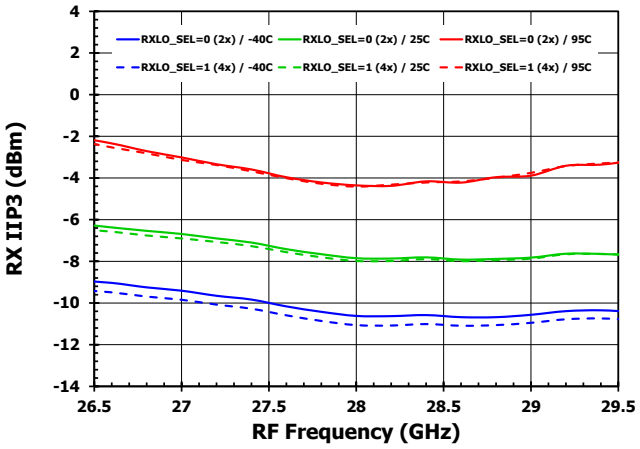

Figure 298. RX IIP3

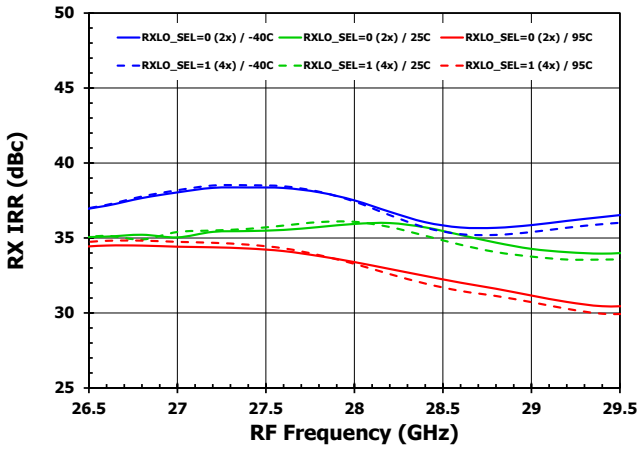

Figure 299. RX Image Rejection Ratio (uncalibrated)

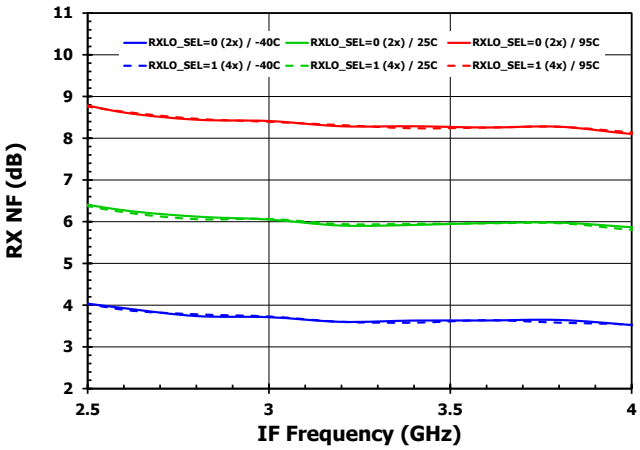

Figure 300. RX NF vs IF

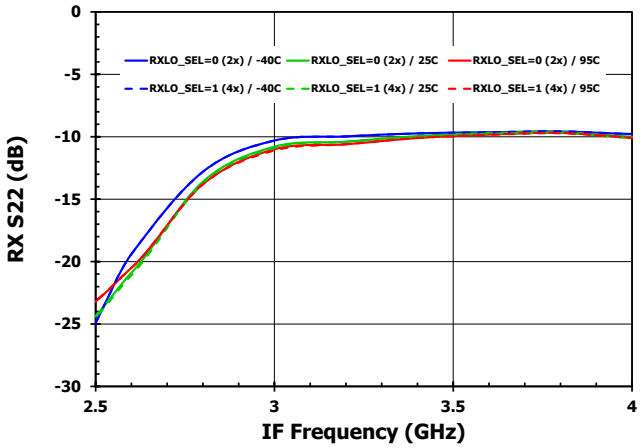

Figure 301. RX S22 vs IF

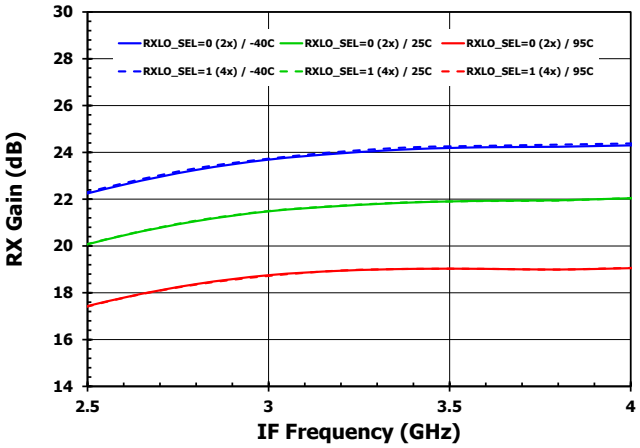

Figure 302. RX Gain vs IF

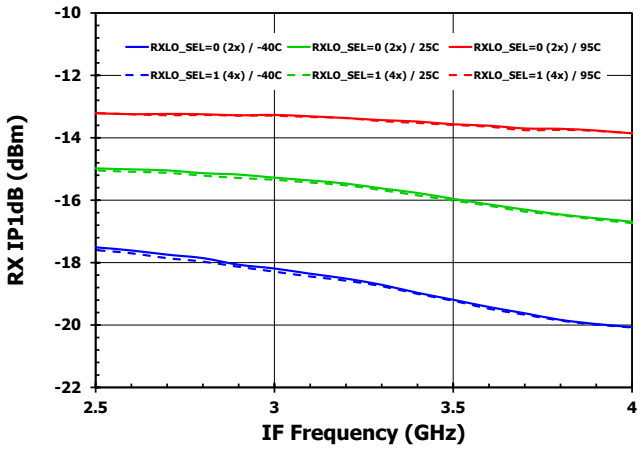

Figure 303. RX IP1dB vs IF

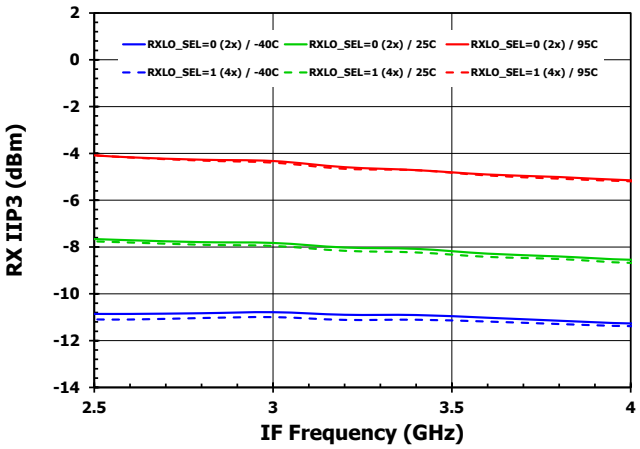

Figure 304. RX IIP3 vs IF

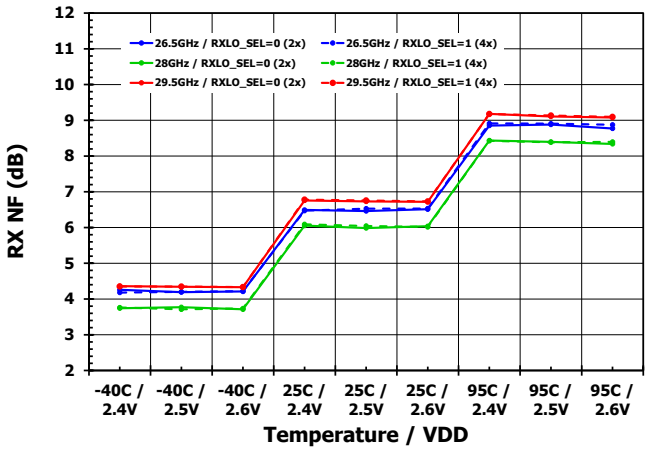

Figure 305. RX NF over VT

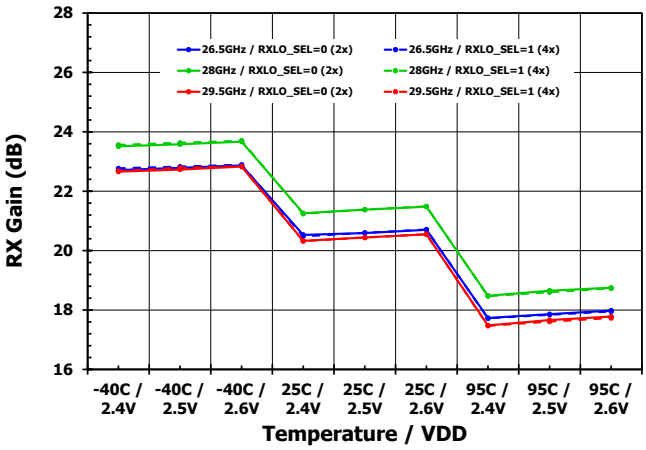

Figure 306. RX Gain over VT

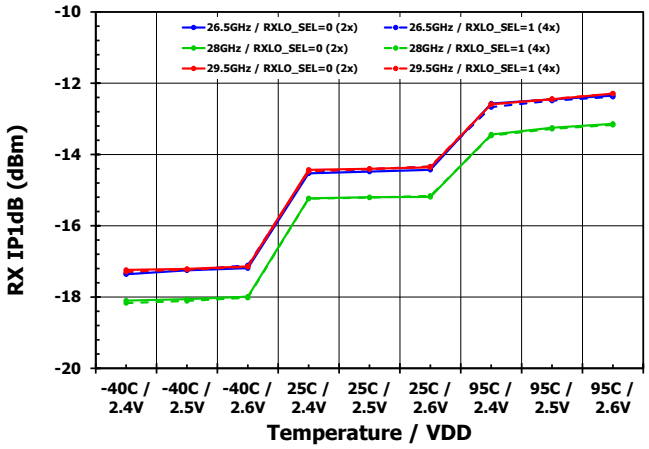

Figure 307. RX IP1dB over VT

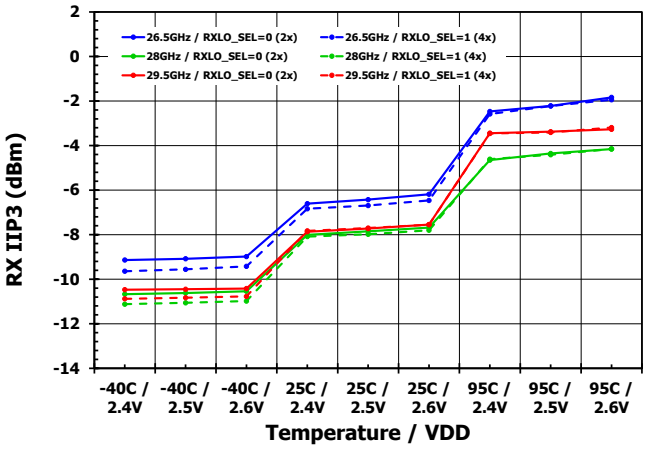

Figure 308. RX IIP3 over VT

4.5.4 RX Performance – RX2 Path

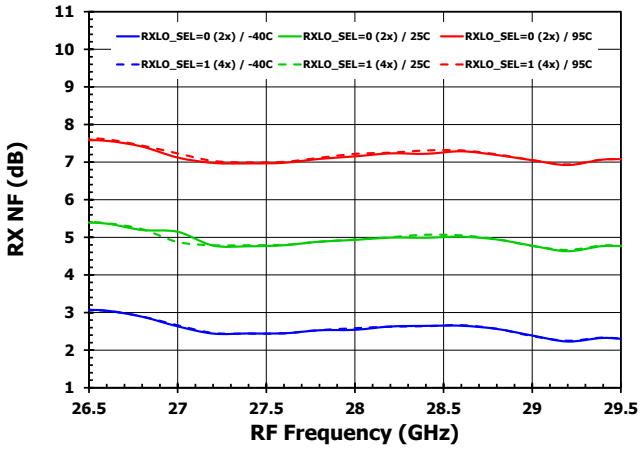

Figure 309. RX2 NF

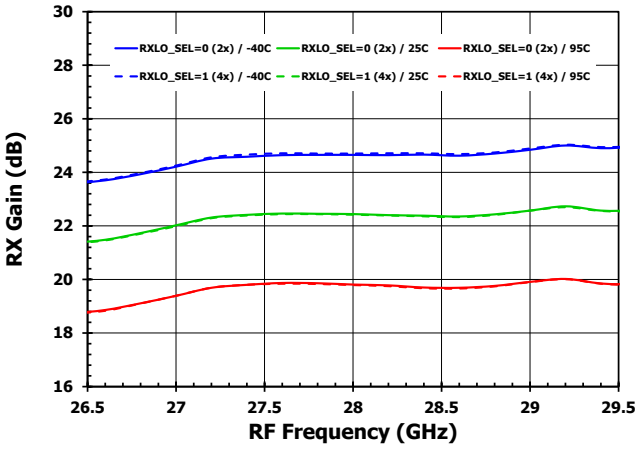

Figure 310. RX2 Gain

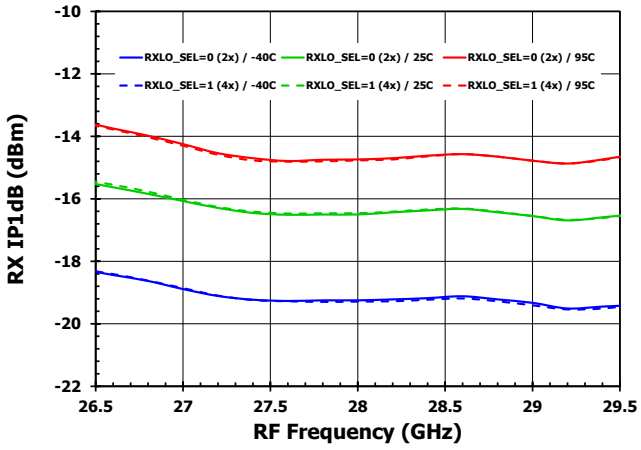

Figure 311. RX2 IP1dB

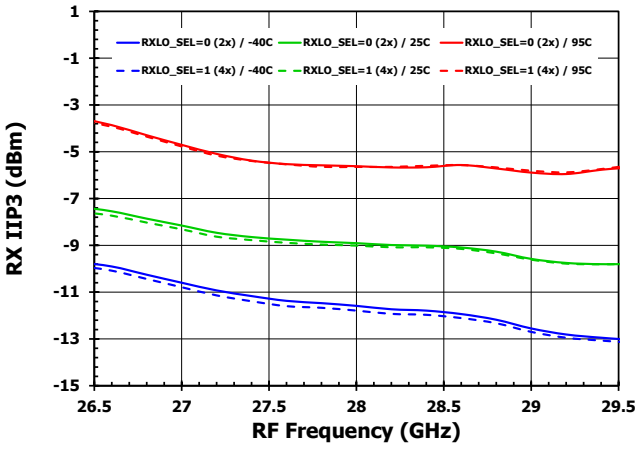

Figure 312. RX2 IIP3

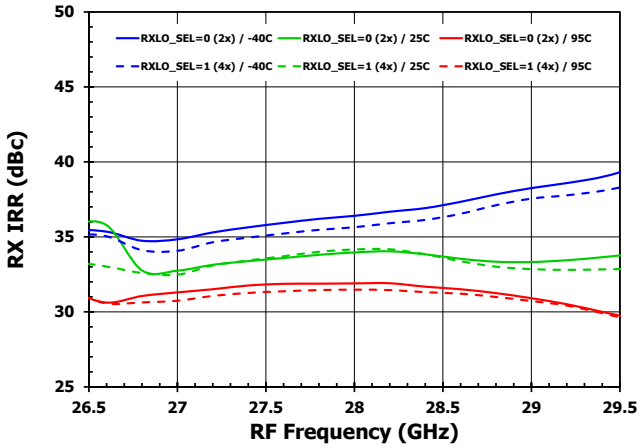

Figure 313. RX2 Image Rejection Ratio (uncalibrated)

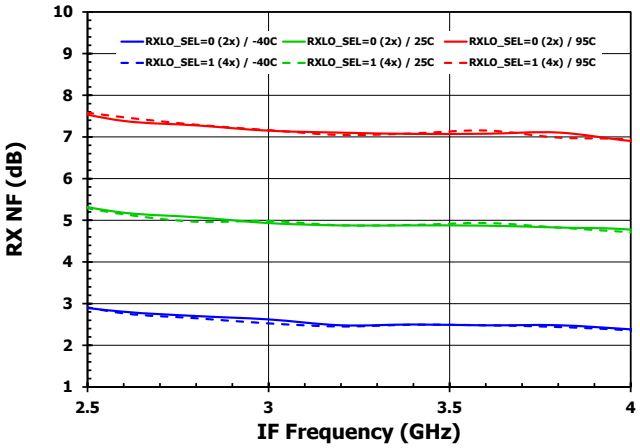

Figure 314. RX2 NF vs IF

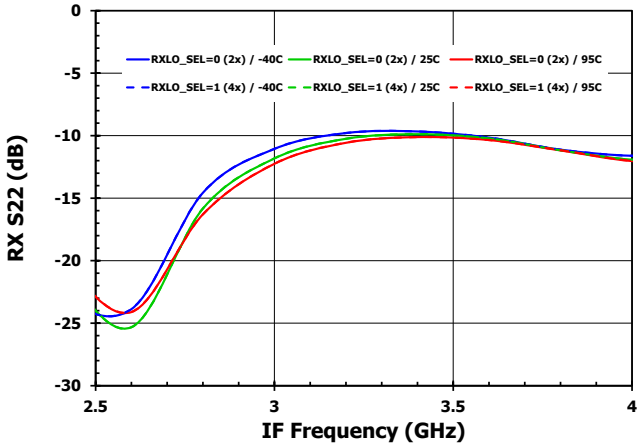

Figure 315. RX2 S22 vs IF

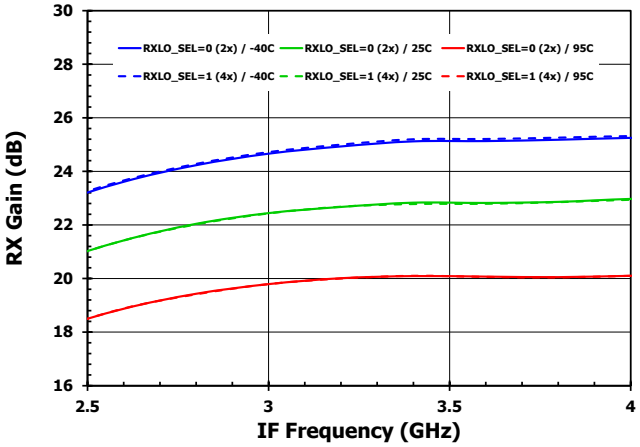

Figure 316. RX2 Gain vs IF

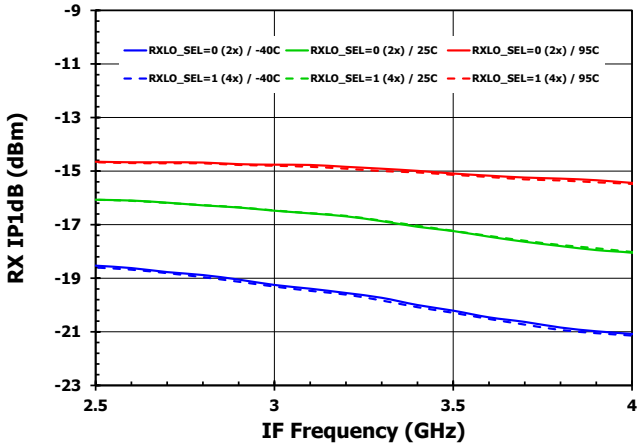

Figure 317. RX2 IP1dB vs IF

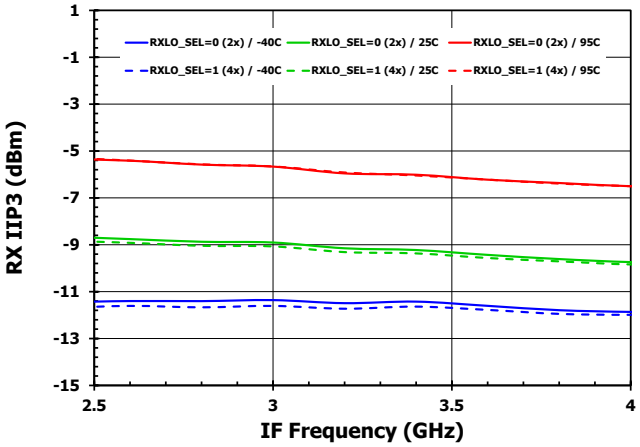

Figure 318. RX2 IIP3 vs IF

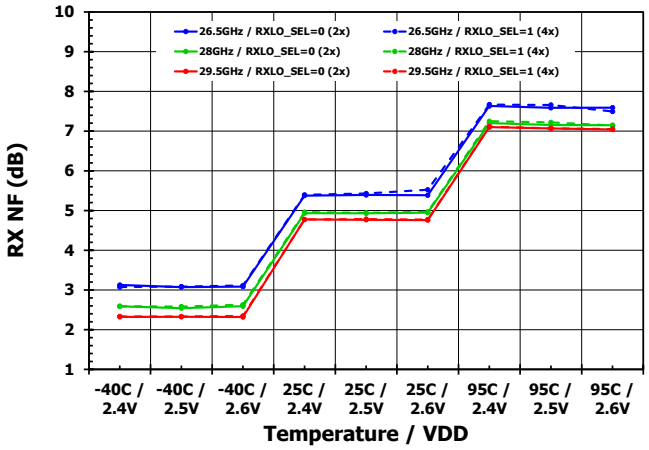

Figure 319. RX2 NF over VT

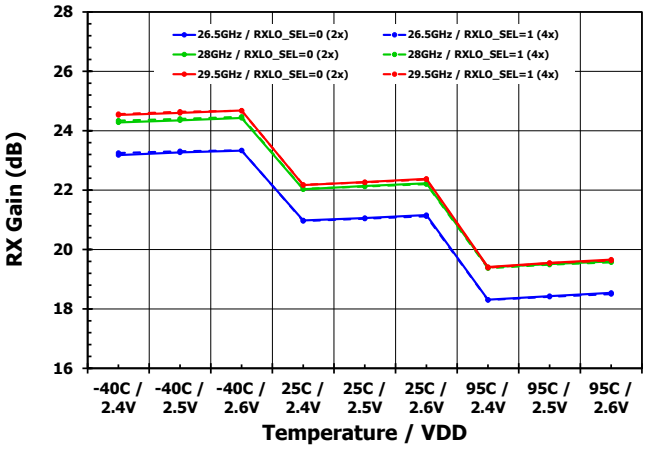

Figure 320. RX2 Gain over VT

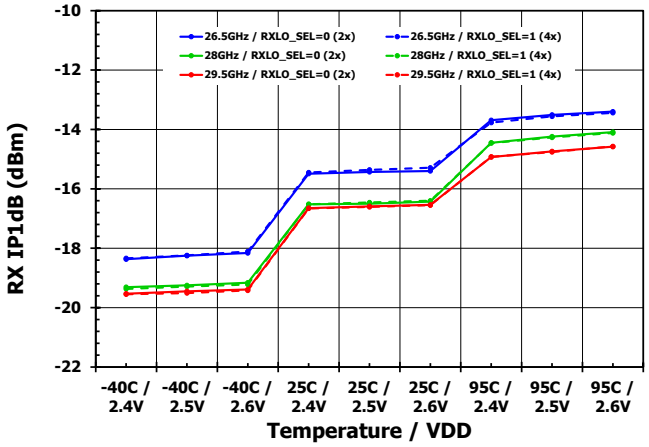

Figure 321. RX2 IP1dB over VT

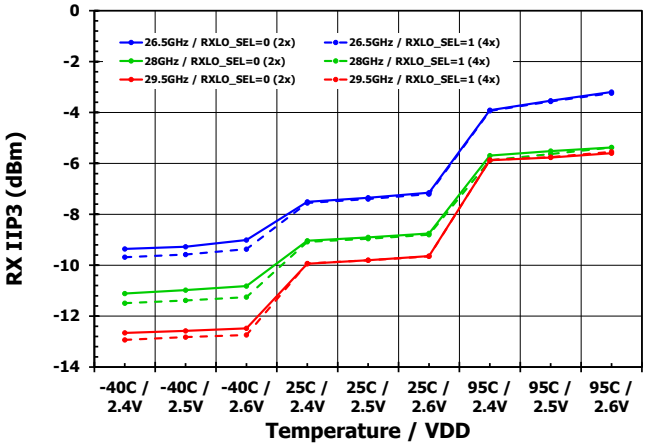

Figure 322. RX2 IIP3 over VT

4.6 3GHz IF/26GHz RF (Band L6)

4.6.1 TX Performance

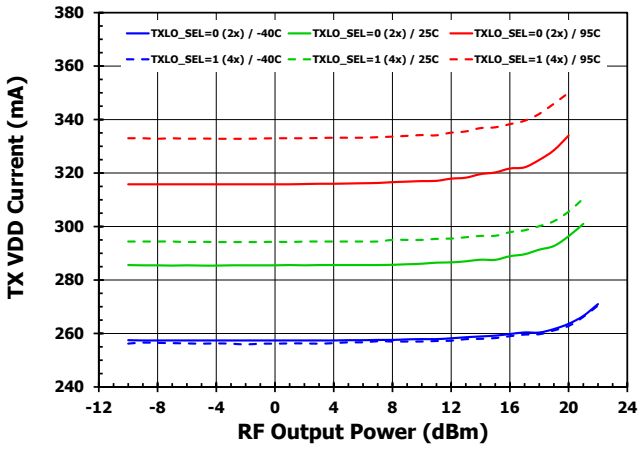

Figure 323. TX VDD Current

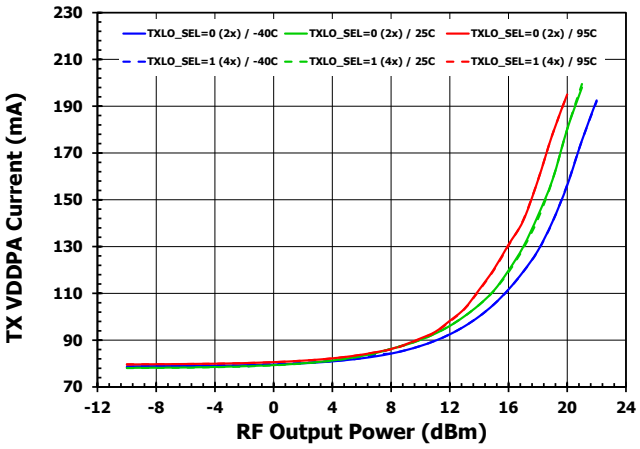

Figure 324. TX VDDPA Current

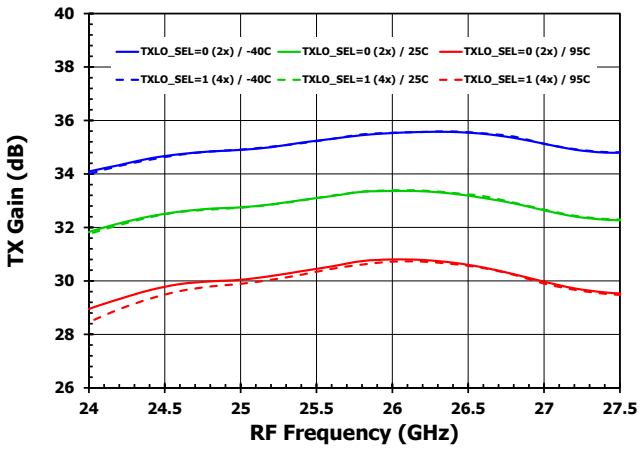

Figure 325. TX Gain

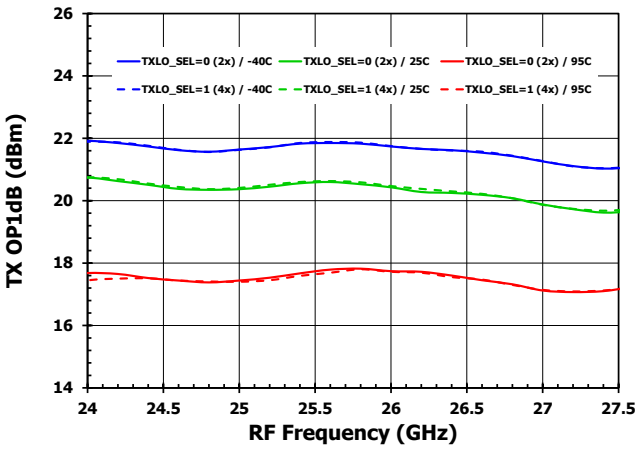

Figure 326. TX OP1dB

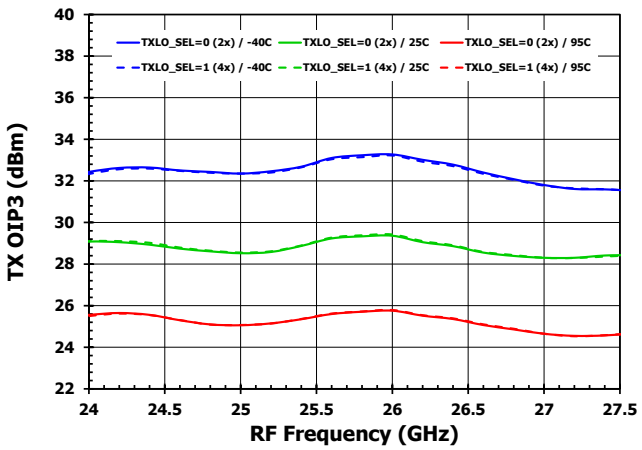

Figure 327. TX OIP3

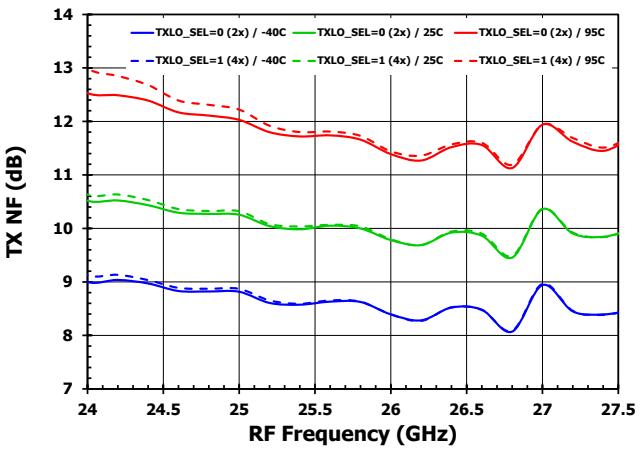

Figure 328. TX NF

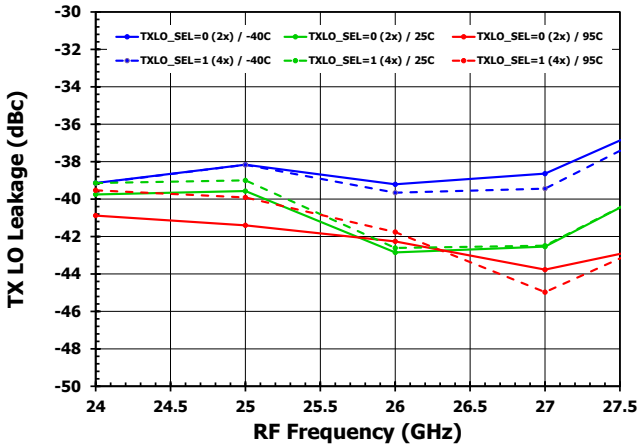

Figure 329. TX LO Leakage (uncalibrated)

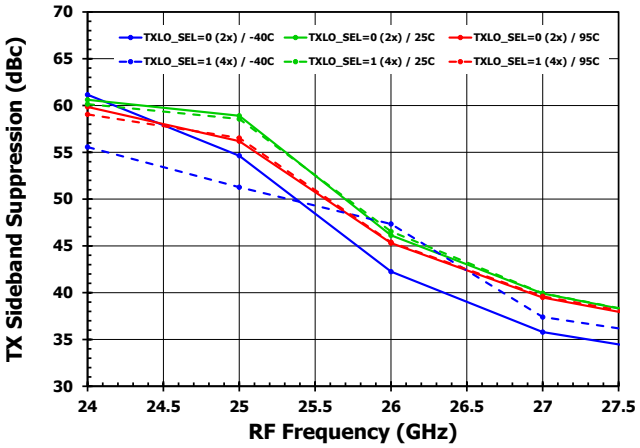

Figure 330. TX Sideband Suppression (uncalibrated)

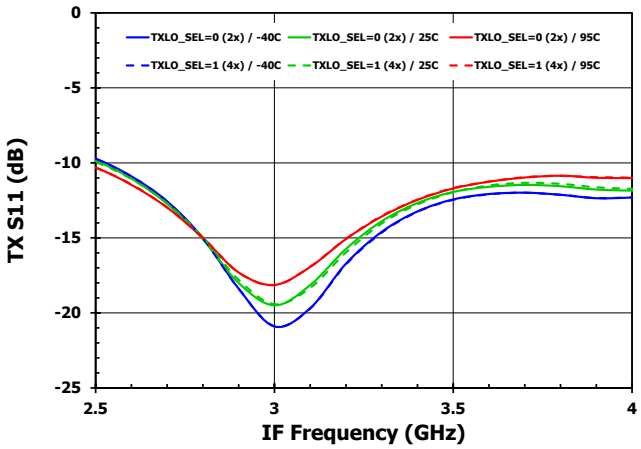

Figure 331. TX S11

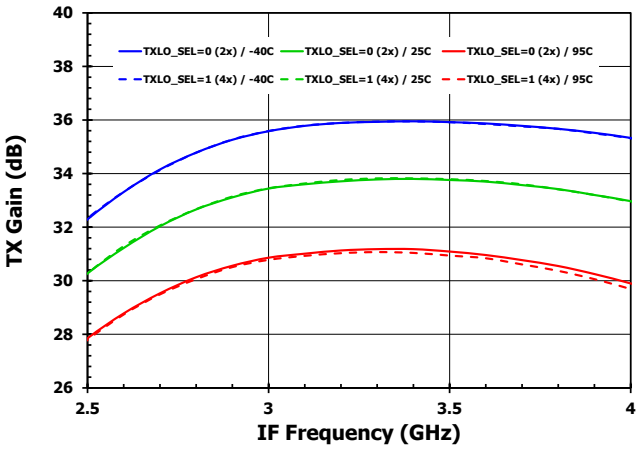

Figure 332. TX Gain vs IF

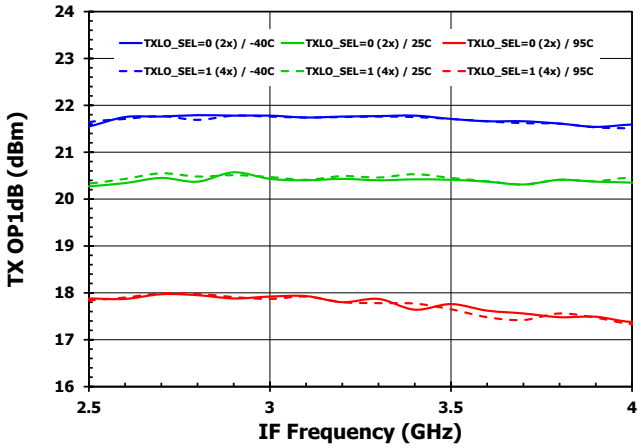

Figure 333. TX OP1dB vs IF

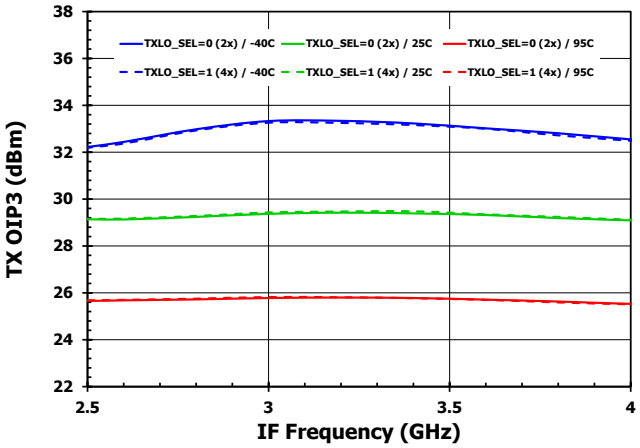

Figure 334. TX OIP3 vs IF

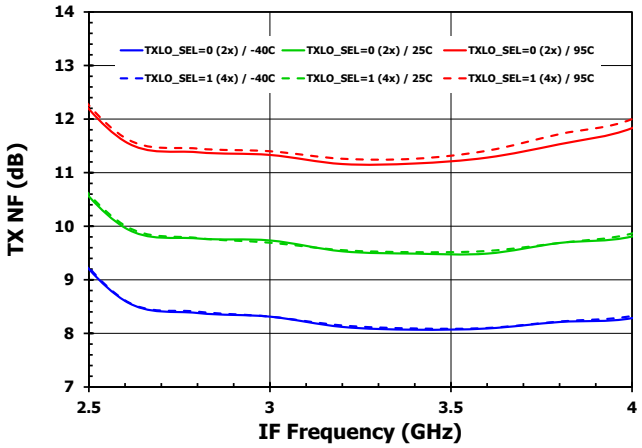

Figure 335. TX NF vs IF

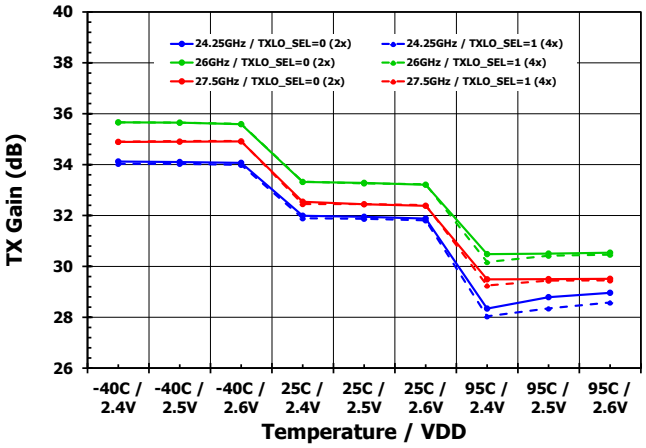

Figure 336. TX Gain over VT

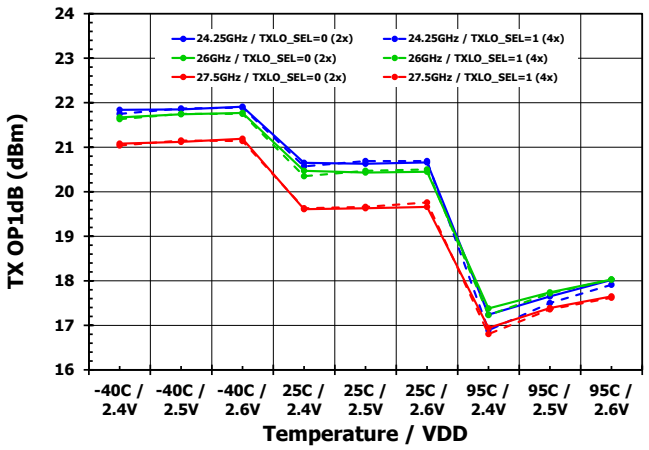

Figure 337. TX OP1dB over VT

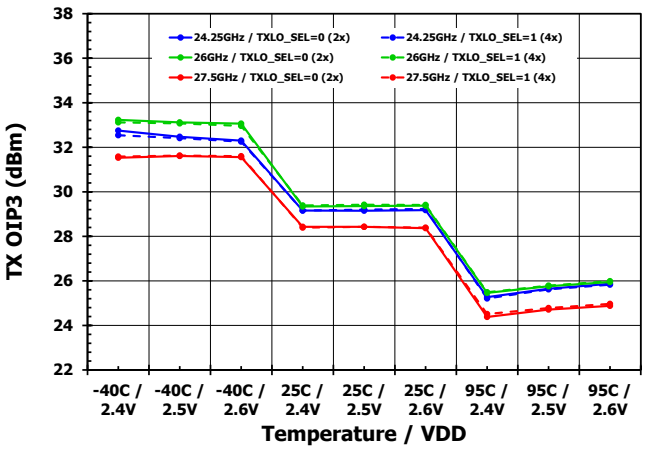

Figure 338. TX OIP3 over VT

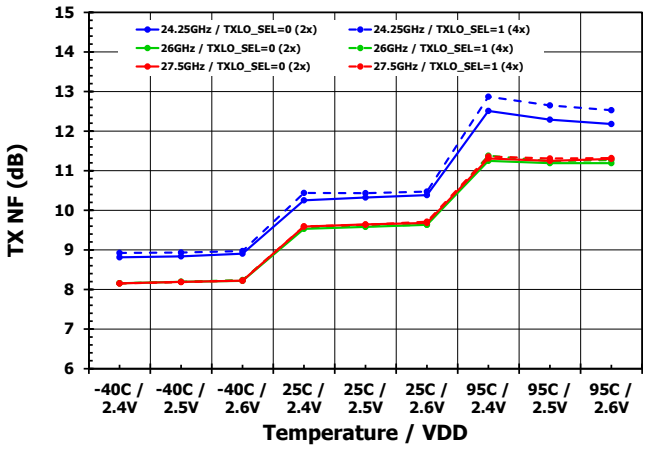

Figure 339. TX NF over VT

4.6.2 TX Performance – V_{DDPA} = 3.3V

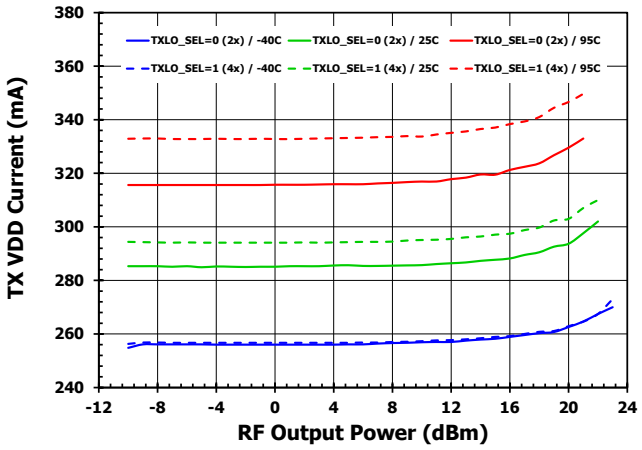

Figure 340. TX VDD Current

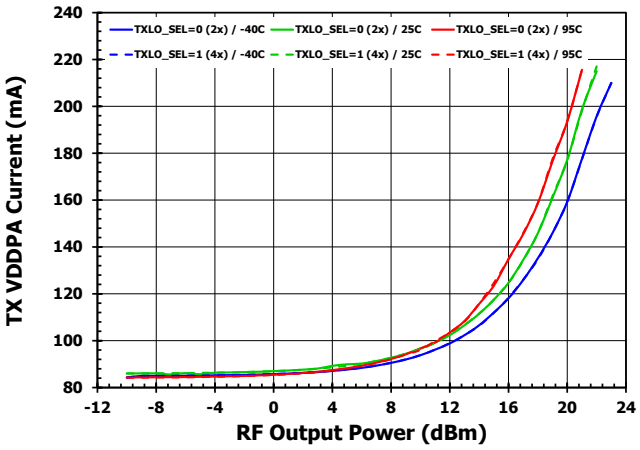

Figure 341. TX VDDPA Current

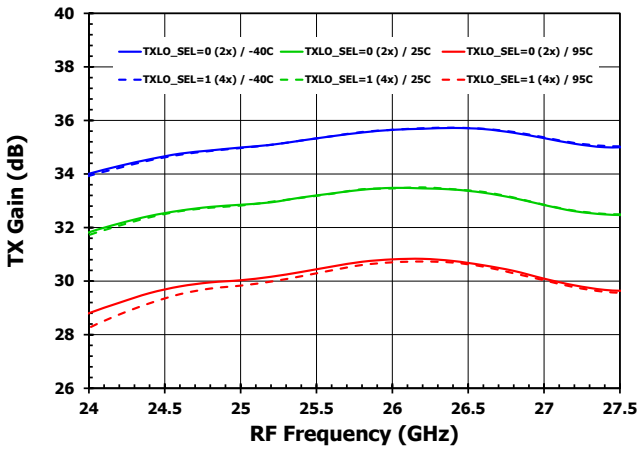

Figure 342. TX Gain

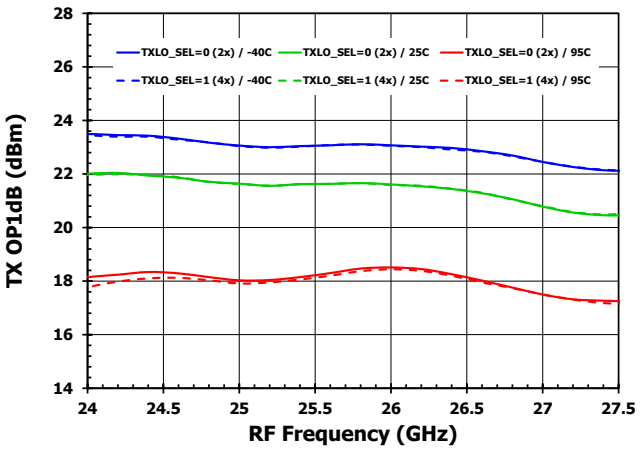

Figure 343. TX OP1dB

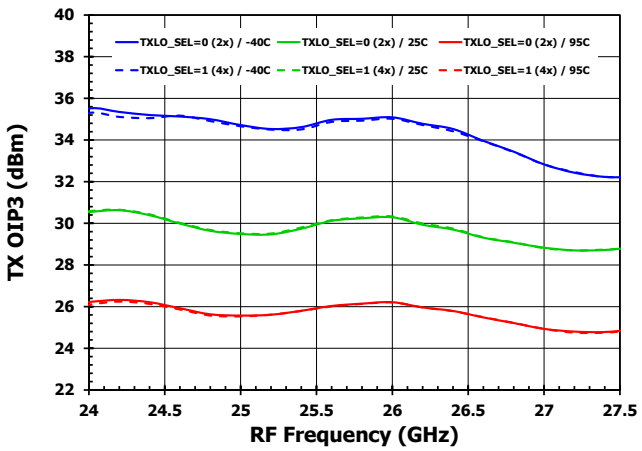

Figure 344. TX OIP3

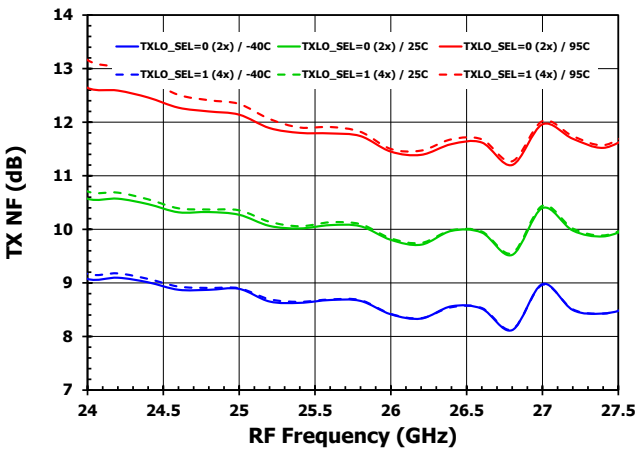

Figure 345. TX NF

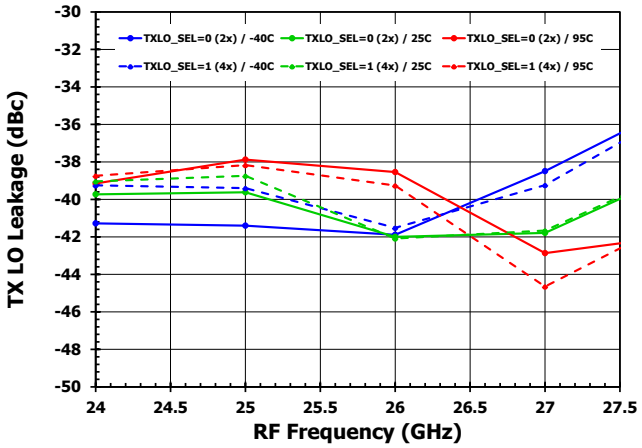

Figure 346. TX LO Leakage (uncalibrated)

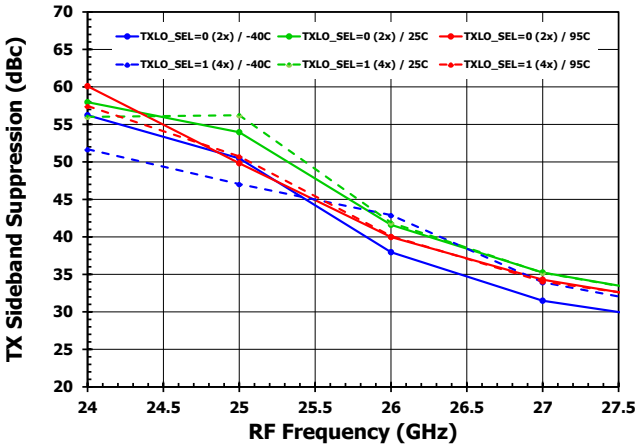

Figure 347. TX Sideband Suppression (uncalibrated)

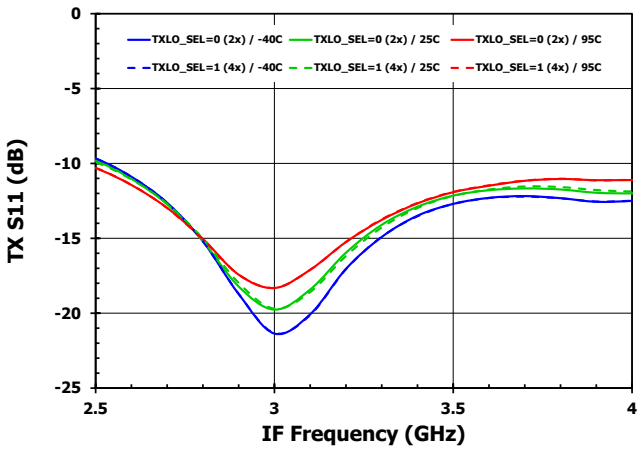

Figure 348. TX S11

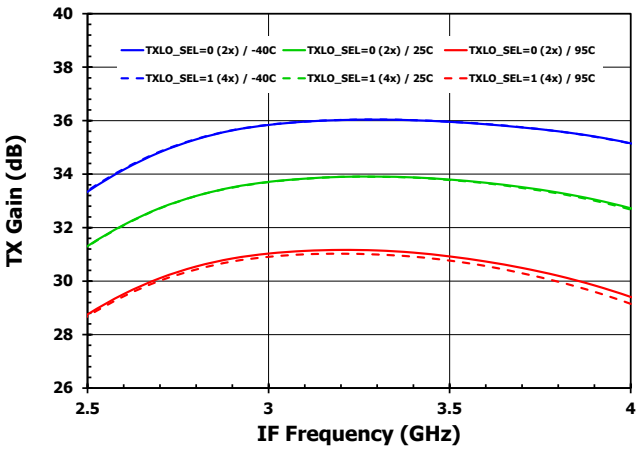

Figure 349. TX Gain vs IF

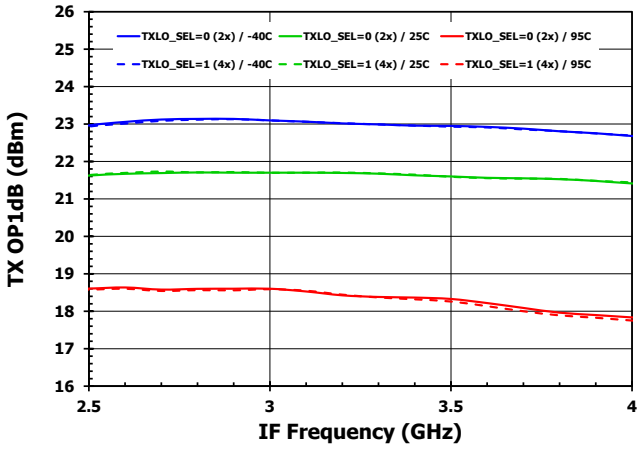

Figure 350. TX OP1dB vs IF

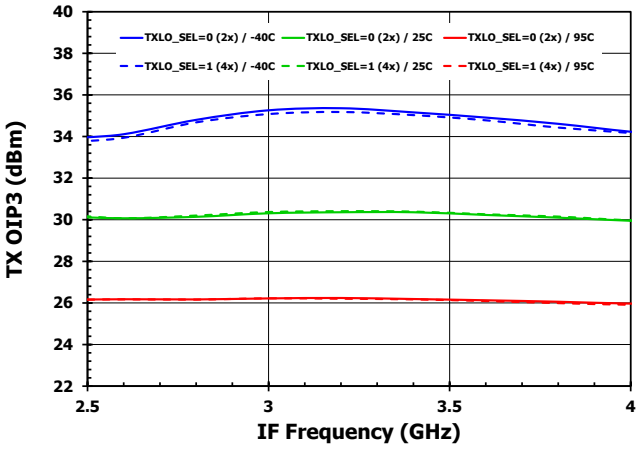

Figure 351. TX OIP3 vs IF

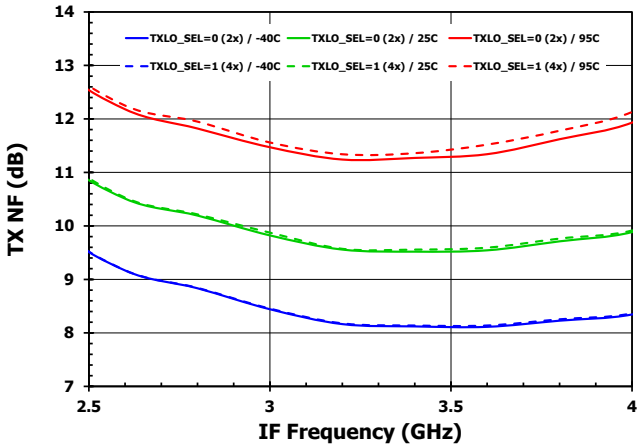

Figure 352. TX NF vs IF

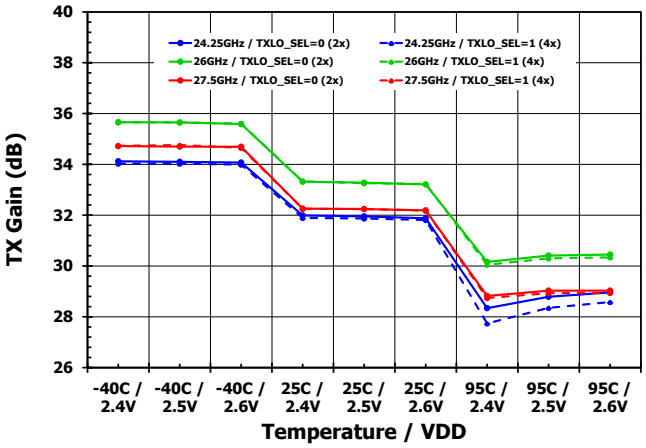

Figure 353. TX Gain over VT

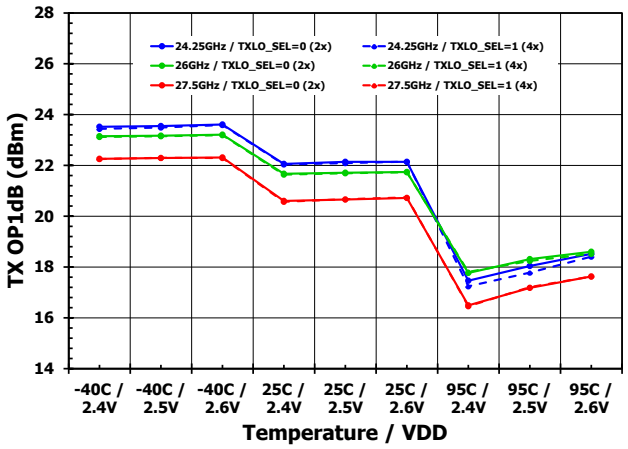

Figure 354. TX OP1dB over VT

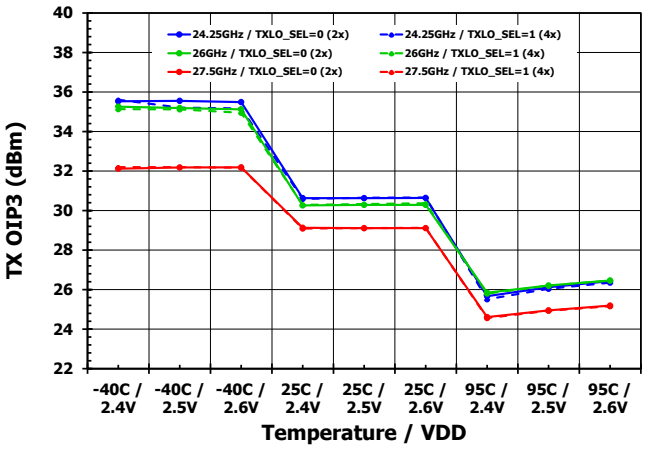

Figure 355. TX OIP3 over VT

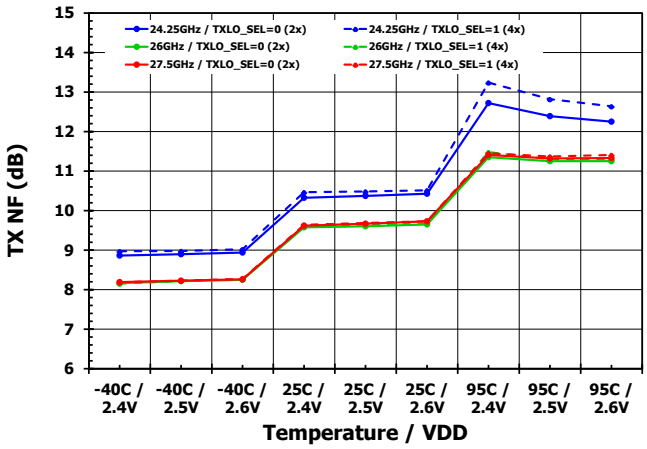

Figure 356. TX NF over VT

4.6.3 RX Performance

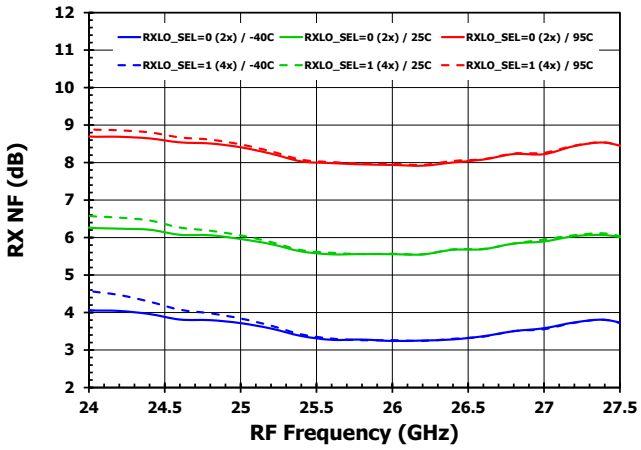

Figure 357. RX NF

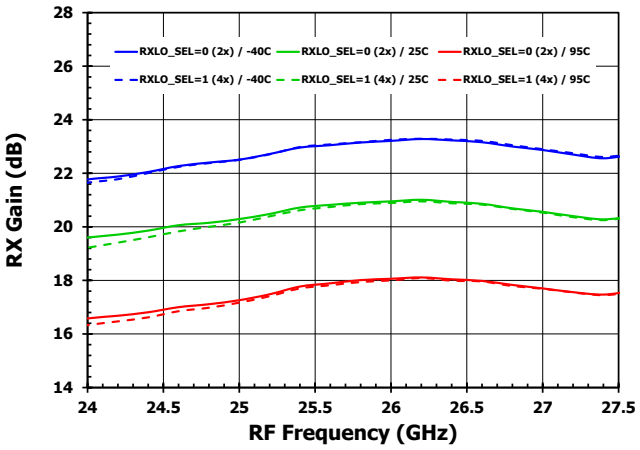

Figure 358. RX Gain

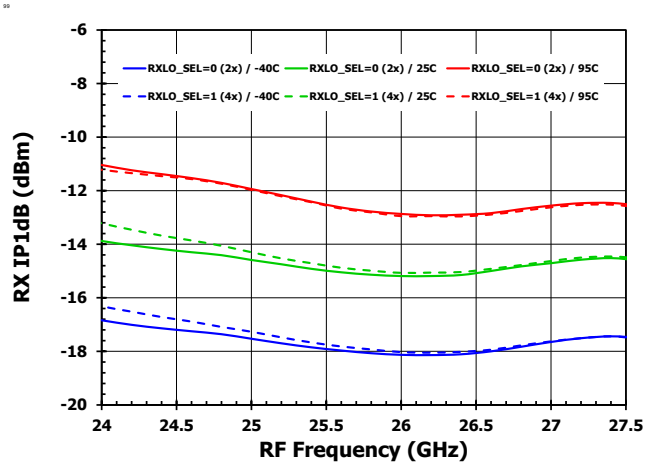

Figure 359. RX IP1dB

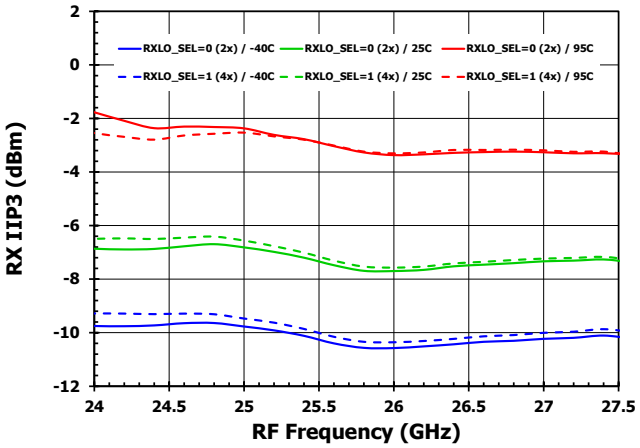

Figure 360. RX IIP3

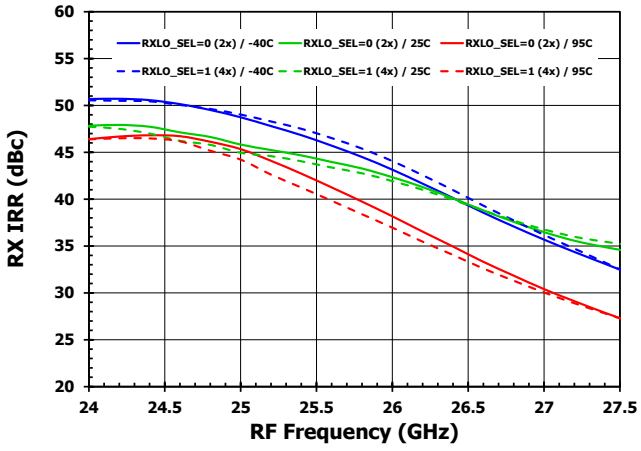

Figure 361. RX Image Rejection Ratio (uncalibrated)

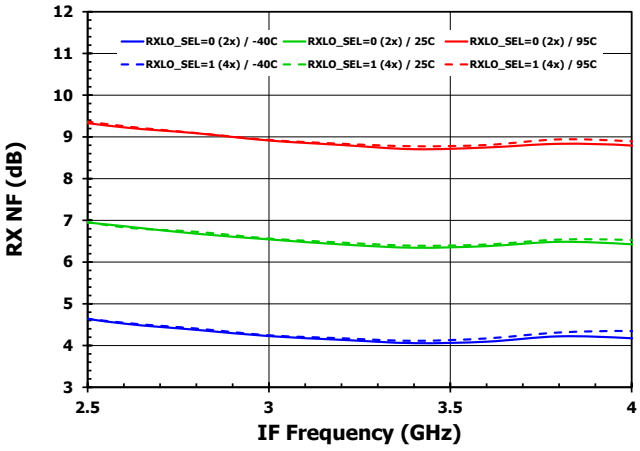

Figure 362. RX NF vs IF

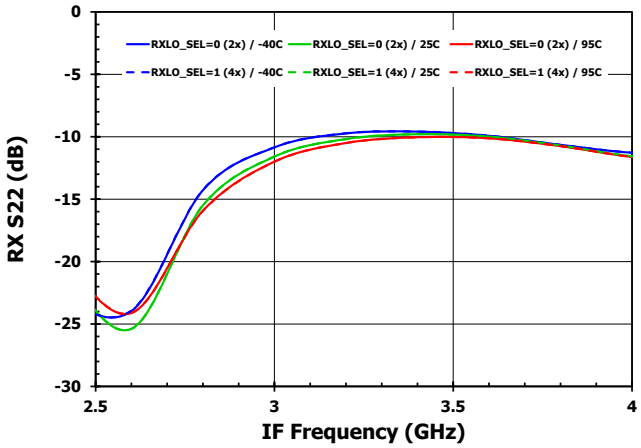

Figure 363. RX S22 vs IF

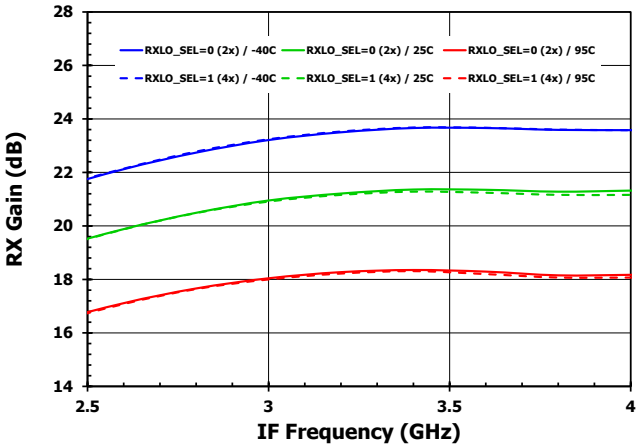

Figure 364. RX Gain vs IF

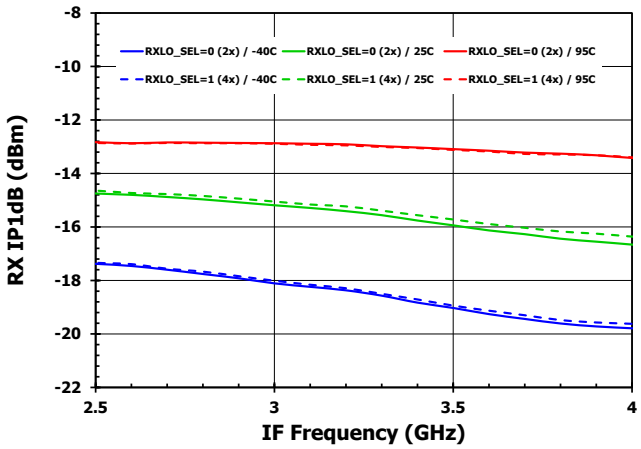

Figure 365. RX IP1dB vs IF

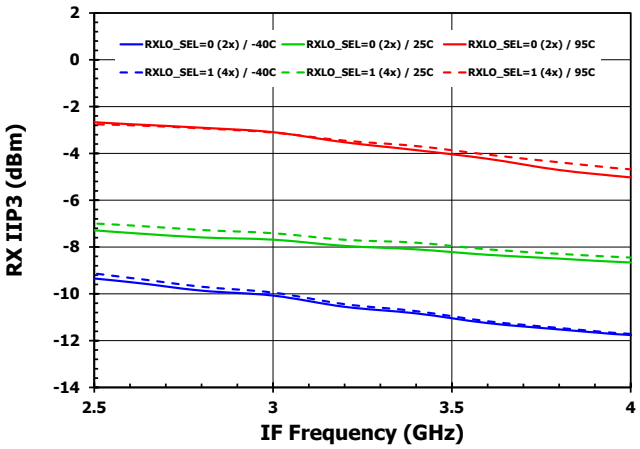

Figure 366. RX IIP3 vs IF

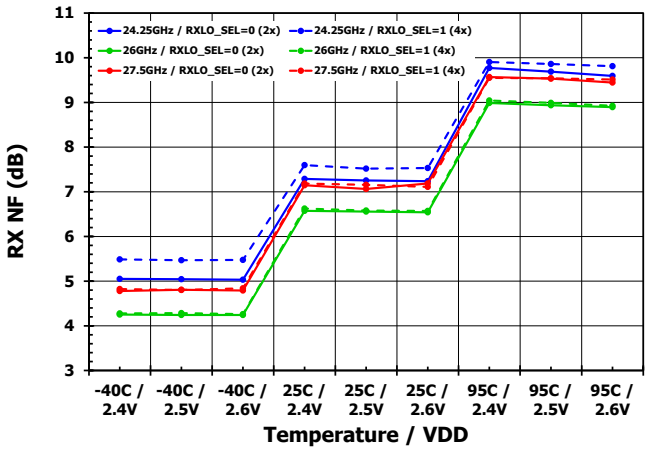

Figure 367. RX NF over VT

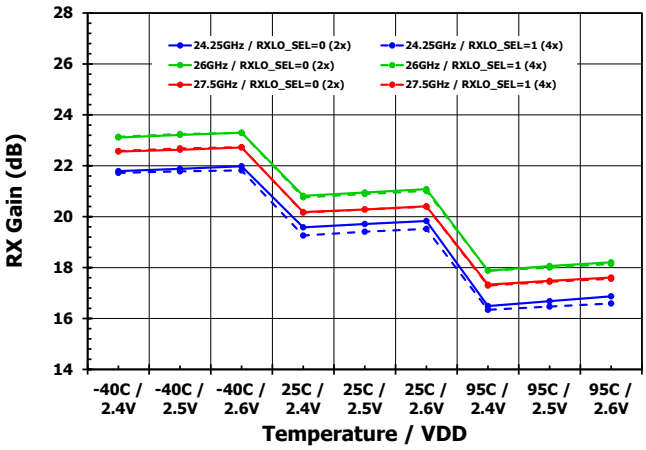

Figure 368. RX Gain over VT

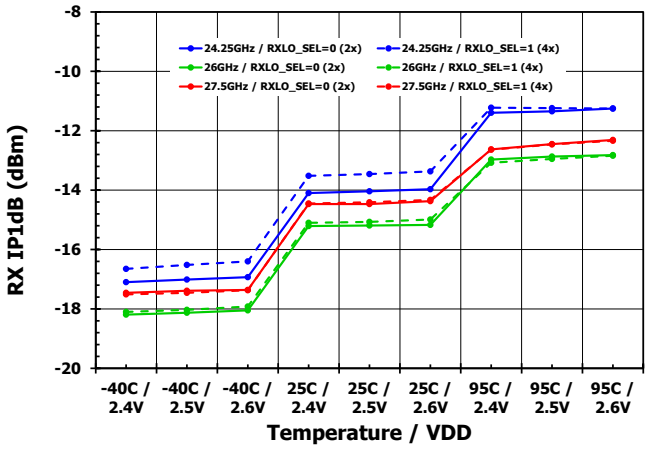

Figure 369. RX IP1dB over VT

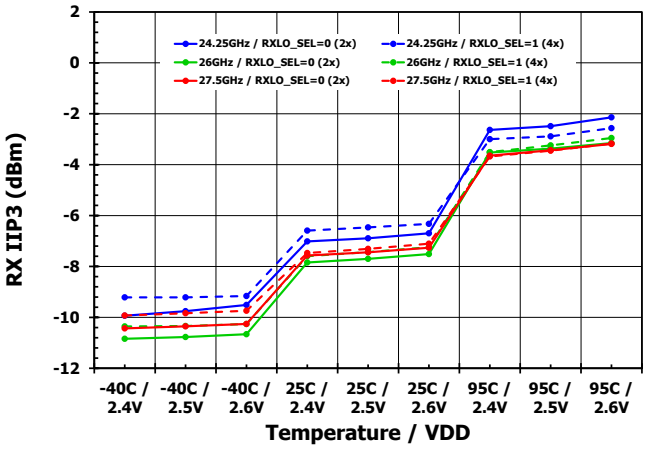

Figure 370. RX IIP3 over VT

4.6.4 RX Performance – RX2 Path

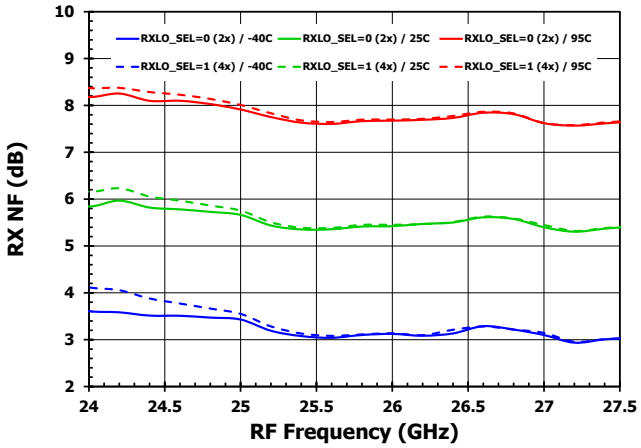

Figure 371. RX2 NF

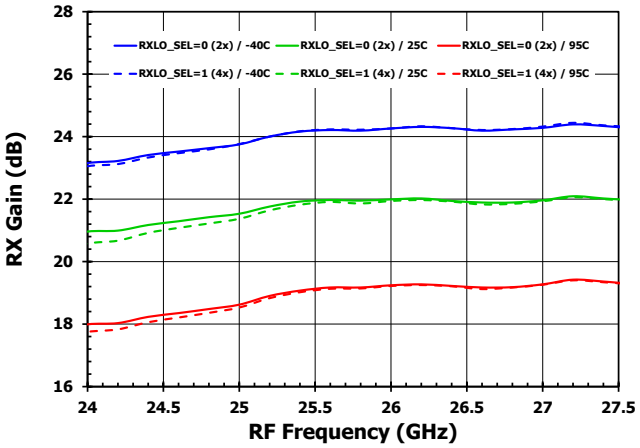

Figure 372. RX2 Gain

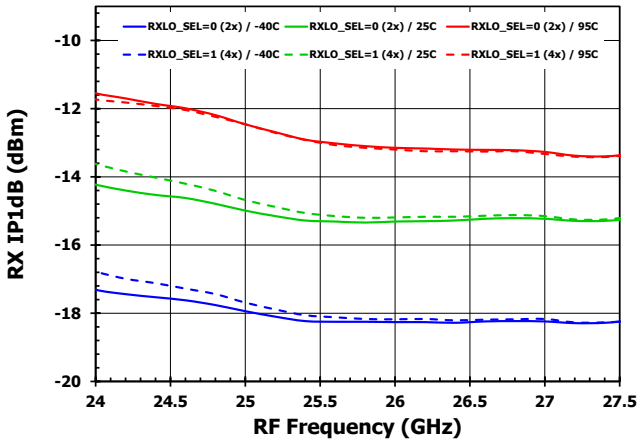

Figure 373. RX2 IP1dB

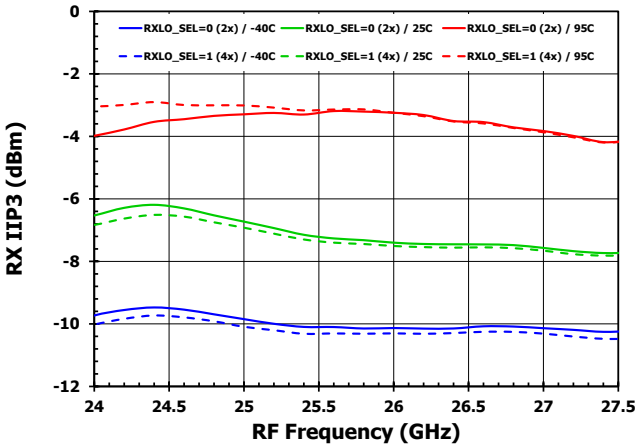

Figure 374. RX2 IIP3

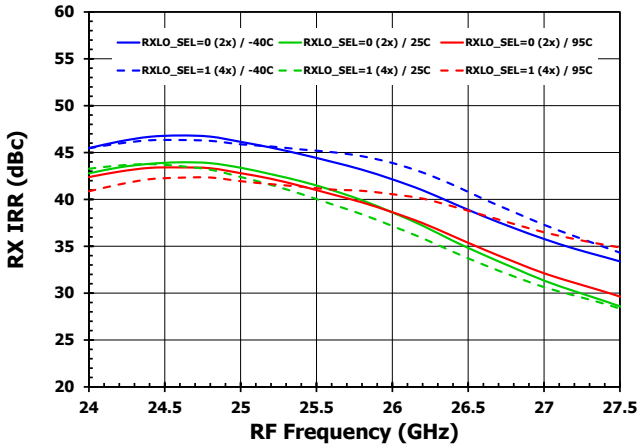

Figure 375. RX2 Image Rejection Ratio (uncalibrated)

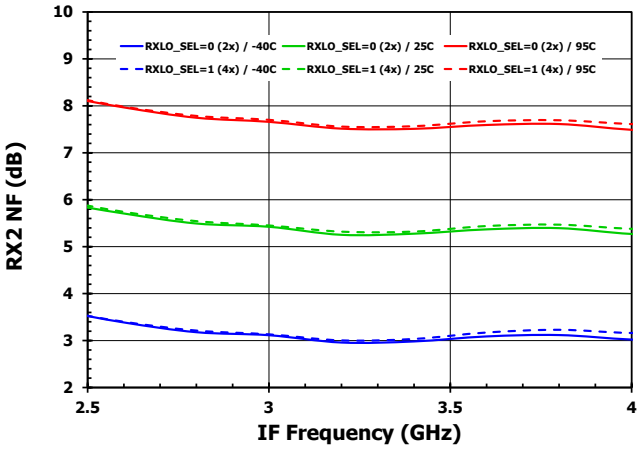

Figure 376. RX2 NF vs IF

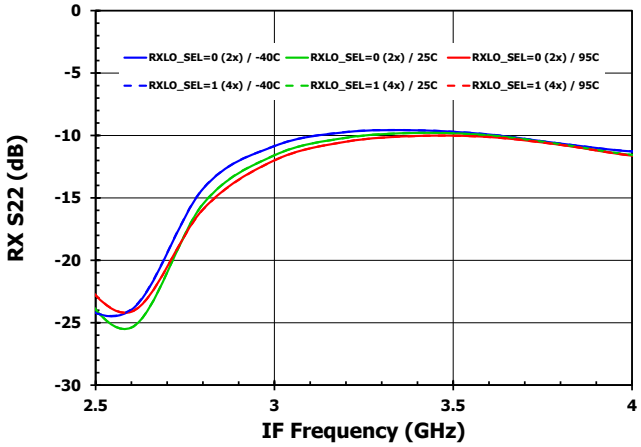

Figure 377. RX2 S22 vs IF

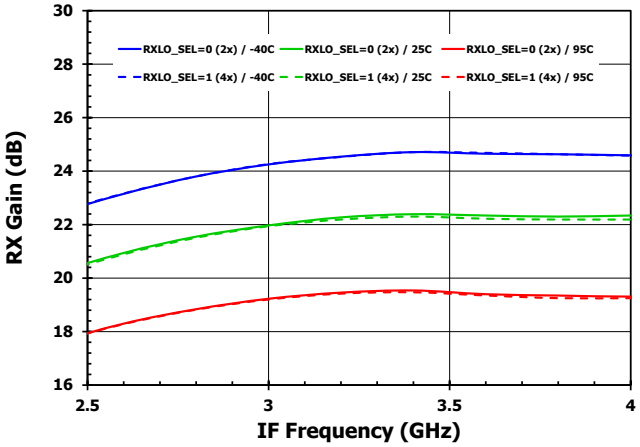

Figure 378. RX2 Gain vs IF

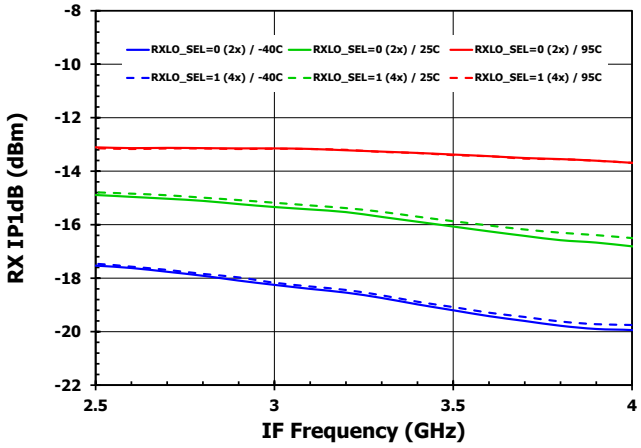

Figure 379. RX2 IP1dB vs IF

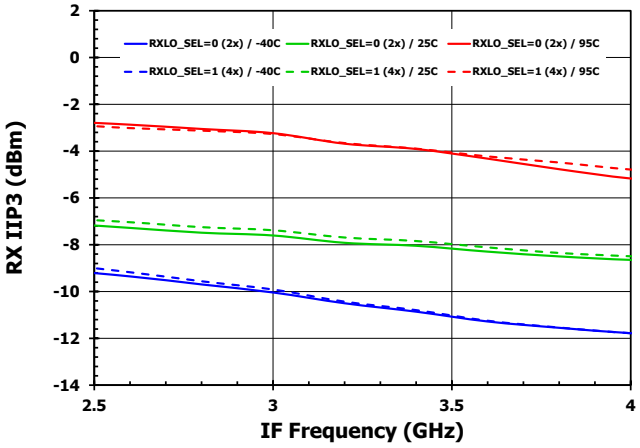

Figure 380. RX2 IIP3 vs IF

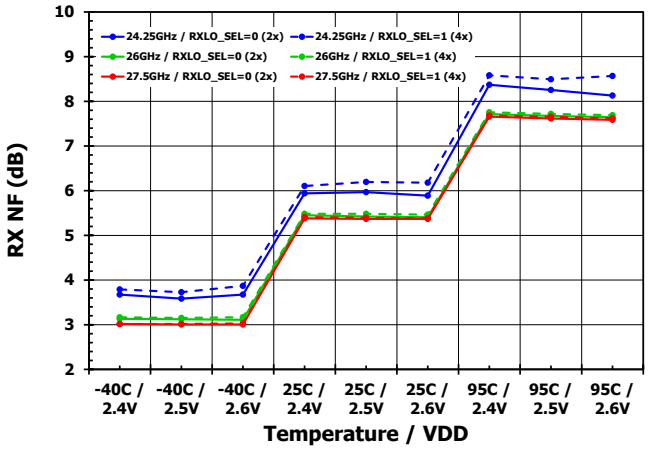

Figure 381. RX2 NF over VT

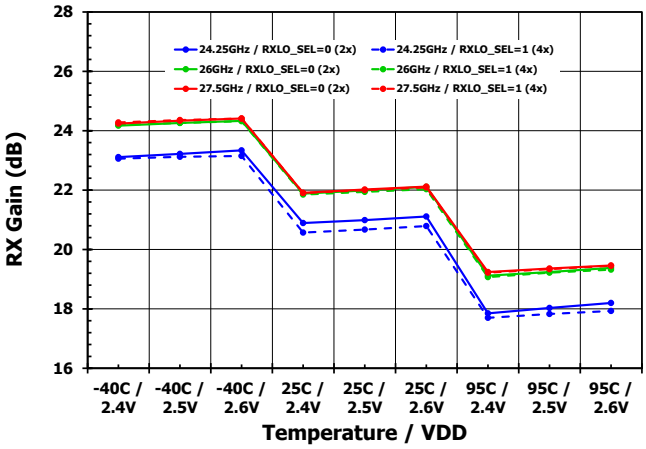

Figure 382. RX2 Gain over VT

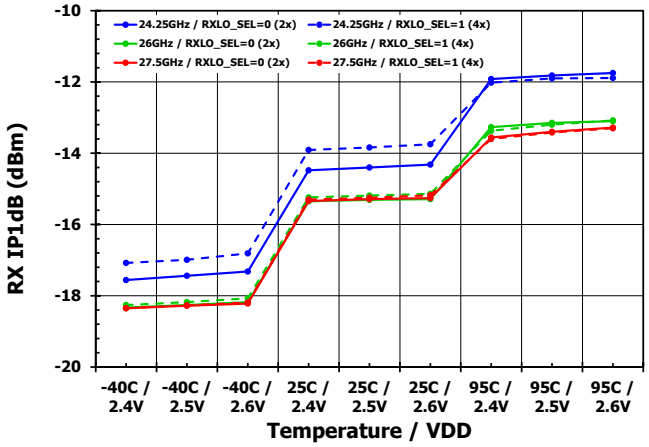

Figure 383. RX2 IP1dB over VT

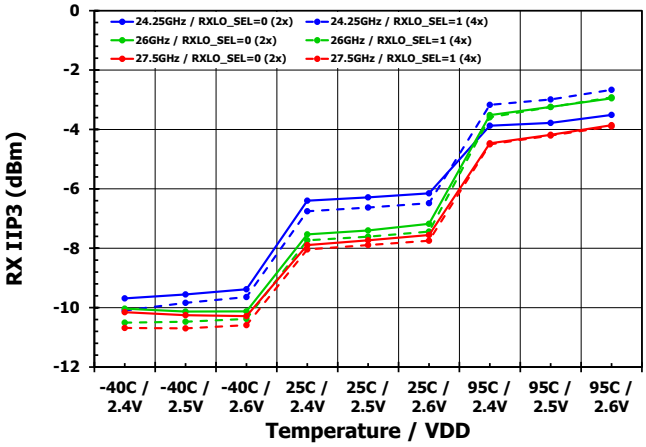

Figure 384. RX2 IIP3 over VT

5. Functional Description

The F5701 has an integrated temperature sensor and a TX power detector. These signals can be read through SPI interface using the on-chip ADC. The F5701 can also output an analog signal representation of the temperature sensor or power detector measurements through the AOUT pin. However, the use of the AOUT pin is not suggested for panel implementation or operation. The pin can be grounded or left floating when not used.

5.1 Temperature Sensor

Complete the procedure outlined in “Procedure to Read Temperature Sensor” to operate and access the measurement data through the SPI interface. For the full register information, see “Register Information”. The theoretical equation used to estimate the temperature from the digital readout is:

$$T[°C] = 0.78 \cdot D + T_0$$

The intercept, T_0, of this linear approximation function is sensitive to process variation, having a typical value of -290 and standard deviation of 20. Therefore, achieving accurate temperature readings requires a single point calibration to remove the error due to process induced intercept variation. To perform a single point calibration, measure the temperature while signal paths are disabled and at a known ambient temperature (ensuring no heat generating sources nearby that would cause a delta between ambient temperature and chip temperature). To disable signal paths, set register bits 0x00[0] and 0x00[3] to 0 (TRX_EN and LO_EN bits of the CTRL_CFG register). Calculate T_0 from the known temperature and the returned code value and store it in the scratch register or off-chip memory. For all future temperature readings, use this intercept value to calculate the temperature.

Note: The chip cannot be in the standby mode and the master bias must be enabled to operate the sensor.

5.1.1 Procedure to Read Temperature Sensor

The following example explains how to read values from the temperature sensor:

1. Enable the temperature sensor and select the core sensor: write 0x3630 to Register 0x05.
2. Run the ADC on Temperature Sensor: write 0x0100 to Register 0x0A and write 0x0285 to Register 0x0B.
3. Fetch the temperature sensor result: read bits [9:0] of Register 0x58.
4. Turn off the ADC and oscillator: write 0x0204 to Register 0x0B.
5. Disable the temperature sensor: write 0x0630 to Register 0x05.

5.2 Power Detector

The on-chip power detector measures the TX output power and operates over a broad power range from 0dBm to 19dBm. Complete the procedures outlined in “Procedure to Read TX Power Detector” to operate and access the measurement data through the SPI interface. For the full register information, see “Register Information.” The average RF output power level in dBm may be calculated from the digital readout, D, using the following equation.

$$P_{out}[dBm] = 10 \cdot log_{10}\left(\frac{D}{1024}\right) + 18$$

5.2.1 Procedure to Read TX Power Detector

The following example explains how to read values from the TX power detector:

1. Turn on the power detector bias: write 0x0632 to Register 0x05.
2. Enable the power detector: write 0x2021 to Register 0x06.
3. Run the ADC on Power Detector: write 0x0011 to Register 0x0A and write 0x0285 to Register 0x0B. Note that both ADC_TX_PD and ADC_TX_PDREF need to be selected (set to 1) in Register 0x0A.
4. Fetch the result: read bits [9:0] of Register 0x50.

5. Turn off the ADC and oscillator: write 0x0204 to Register 0x0B.
6. Turn off the power detector bias: write 0x0630 to Register 0x05.

5.3 Look-Up Table (LUT)

The F5701 has a dedicated LUT used for Fast Gain Switching Mode, which allows for fast programming to a specific gain setting. The LUT has 128 addresses and each address points to a 32-bit register that contains a single programmable gain setting (TX/RX FE_SET and VGA_SET register values). Each gain setting can be used for either TX or RX. Latch capability is also implemented in the protocol such that the LUT information can be buffered to be loaded later. For more information, see “LUT Read/Write” and “Fast Gain Switching.”

6. Control Mode

6.1 Strobe Pin Control

The external STRB pin (pin D7) acts as an asynchronous request, which can change configuration of all the chips in the panel with a single pulse. By setting the register bits CTRL_CFG.STROBE_PROG (or CTRL_CFG[7:5]), the STRB pin can be configured to function as a latch control pin, a TRX toggle pin, or a LUT increment pin for Fast Gain Switching control. Table 1 summarizes STRB pin function settings. Note that the CTRL_CFG.STROBE_PROG register bits can be set to either 001, 010, or 011 for the TRX toggle function, and either 100, 101, or 110 for the LUT increment function. To avoid interfering with regular SPI operation, this strobe function is executed only when the CSB signal is high.

Table 1. STRB Pin Function Settings

CTRL_CFG.STROBE_PROG Bits	Strobe Function
000	Latch mode
001	TRX toggle
010	TRX toggle
011	TRX toggle
100	LUT increment (enabled RX/TX)
101	LUT increment (enabled RX/TX)
110	LUT increment (enabled RX/TX)

6.1.1 Latch Mode

In this mode, when a strobe pulse is inserted, all the buffers are latched to their respective registers at the strobe pulse’s positive edge.

6.1.2 TRX Toggle

In TRX toggle mode, if any of the buffers for registers 0x0 and 0x1 differ from their registers, the strobe pulse will latch the buffers to their registers. Thus, the desired program mode, TRX mode, and the effective pointer registers become effective. The subsequent strobe pulse then toggles the TRX bit in CTRL_CFG and LUT registers and it becomes effective immediately. If the buffers are already the same as their respective registers, however, TRX toggle will happen in the first strobe pulse.

6.1.3 LUT Increment for Fast Gain Switching

Similar to the TRX toggle mode, if any of the buffers differ from their registers, the first strobe pulse will latch the buffers to their registers. In subsequent strobe pulses, the LUT address pointers are incremented and the data is fetched from the selected LUTs at the strobe pulse rising edge. At the strobe falling edge they are loaded to the SET registers.

6.2 Gain Control

TX gain is controlled by registers TX_VGA_SET (0x22) and TX_FE_SET (0x23). RX gain is controlled by registers RX_VGA_SET (0x20) and RX_FE_SET (0x21). The VGA_SET registers adjust VGA gain attenuation in the IF path to provide 20dB gain dynamic range, while the FE_SET registers adjust VGA gain attenuation in the RF path to provide 10dB gain dynamic range. For gain control mapping and typical performance at nominal settings for the 26GHz RF/ 5GHz IF frequency band, see the following tables. Note that optimal gain settings may need to be updated for the other RF/IF frequency bands.

Table 2. TX Gain Control Mapping and Typical Performance: 26GHz RF/5GHz IF

Gain Step	RF/ IF	TX_FE_SET [11:8] TX_RFVGA_GAIN	TX_VGA_SET [11:7] TXVGA2_CTRL	TX_VGA_SET [6:2] TXVGA1_CTRL	TX_VGA_SET [0] TXVGA_SW_0p25	Gain Attenuation (dB)	OP1dB (dBm)	OIP3 (dBm)	NF (dB)
0	RF	15	31	31	1	0.0	20.3	31.8	12.7
1		14	31	31	1	1.0	20.3	32.2	13.7
2		13	31	31	1	2.0	20.2	32.4	14.3
3		10	31	31	1	2.9	19.8	30.9	15
4		9	31	31	1	4.0	19.5	30.6	15.7
5		5	31	31	1	5.0	19.2	31.4	16.3
6		2	31	31	1	6.1	18.2	29.9	17.1
7		4	31	31	1	6.8	17.6	27.9	17.5
8		1	31	31	1	7.8	16.5	26.9	18.2
9		0	31	31	1	10.4	13.9	25.3	19.8
0	IF	15	31	31	1	0.0	20.3	31.2	13.1
1		15	31	28	1	0.7	20	31.3	13.9
2		15	31	26	1	1.1	20.2	30.9	14.5
3		15	31	24	1	1.5	20.1	32.3	15
4		15	24	31	0	1.9	20.2	31	14.7
5		15	23	31	1	2.5	19.9	33.3	15.2
6		15	31	21	1	3.0	20.3	32	16.6
7		15	31	19	1	3.6	20.1	30.9	17.3
8		15	30	18	1	4.1	20.3	30.8	17.7
9		15	30	15	0	4.5	20.1	30.1	18.2
10		15	30	13	1	4.9	20.3	32.3	18.6
11		15	30	12	0	5.4	20.2	32.4	19.1
12		15	31	10	0	6.0	20.3	28.6	19.7

Gain Step	RF/ IF	TX_FE_SET [11:8] TX_RFVGA_GAIN	TX_VGA_SET [11:7] TXVGA2_CTRL	TX_VGA_SET [6:2] TXVGA1_CTRL	TX_VGA_SET [0] TXVGA_SW_0p25	Gain Attenuation (dB)	OP1dB (dBm)	OIP3 (dBm)	NF (dB)
13		15	30	9	0	6.6	20.1	30.3	20.2
14		15	30	8	0	7.0	19.9	28.6	20.5
15		15	28	8	0	7.4	19.6	29.1	20.9
16		15	25	8	1	8.0	19.3	28.2	21.3
17		15	24	8	0	8.5	18.9	27.9	21.6
18		15	27	7	1	9.1	18.4	27.7	22.3
19		15	27	6	1	9.5	18	24.9	22.8
20		15	27	5	1	10.1	17.4	26.7	23.3
21		15	31	3	0	10.6	17	24.8	23.8
22		15	9	16	1	11.0	16.3	22.6	23.4
23		15	8	16	0	11.6	15.7	22.9	24.1
24		15	19	7	0	12.0	15.4	21.6	24.7
25		15	19	6	0	12.5	14.9	21	25.2
26		15	19	5	0	13.1	14.4	21.8	25.7
27		15	19	4	0	13.6	13.8	19.7	26.3
28		15	19	3	1	14.1	13.3	19.9	26.7
29		15	4	16	1	14.5	12.6	17.7	26.7
30		15	3	15	0	15.0	12.1	18.3	27.1
31		15	2	15	1	15.5	11.6	17.3	27.6
32		15	15	1	1	16.0	11.4	16.8	28.6
33		15	14	1	0	16.6	10.8	15.6	29
34		15	12	1	1	17.1	10.3	13.4	29.5
35		15	11	1	0	17.7	9.7	14.5	30.1
36		15	10	1	0	18.1	9.3	12.6	30.4
37		15	5	5	1	18.6	8.7	11.1	30.8
38		15	5	4	1	19.2	8.1	11.3	31.3
39		15	4	5	0	19.4	7.9	12.2	31.6
40		15	3	5	0	20.1	7.2	9	32.1

Table 3. RX Gain Control Mapping and Typical Performance: 26GHz RF/5GHz IF

Gain Step	RF/ IF	RX_FE_SET [13:10] RX_LNA2_GAIN	RX_FE_SET [9:8] RX_LNA1_GAIN	RX_VGA_SET [11:7] RXVGA2_CTRL	RX_VGA_SET [6:2] RXVGA1_CTRL	Gain Attenuation (dB)	IP1dB (dBm)	IIP3 (dBm)	NF (dB)
0	RF	15	3	31	31	0.0	-14.1	-7.1	6.4
1		13	3	31	31	1.1	-12.5	-4.8	6.8
2		12	3	31	31	2.1	-11.5	-3.6	7.2
3		3	3	31	31	2.9	-10.6	-2.8	7.7
4		8	3	31	31	3.9	-9.7	-2	8.2
5		6	1	31	31	4.9	-8.6	-1.2	9.6
6		5	1	31	31	5.7	-7.9	-0.4	10.2
7		2	1	31	31	6.9	-6.7	0.2	10.8
8		1	2	31	31	8.0	-5.9	1.9	11.5
9		3	0	31	31	8.8	-5	2.7	13
10		8	0	31	31	9.9	-4	3.6	13.7
0	IF	15	3	31	31	0.0	-14.1	-7.1	6.4
1		15	3	28	31	0.6	-14.2	-7.2	6.5
2		15	3	25	31	1.1	-14.3	-7.3	6.5
3		15	3	23	31	1.5	-14.5	-7.4	6.5
4		15	3	21	31	1.9	-14.5	-7.4	6.5
5		15	3	18	31	2.6	-14.6	-7.6	6.6
6		15	3	16	31	3.2	-14.7	-7.7	6.6
7		15	3	14	31	3.5	-14.8	-7.8	6.6
8		15	3	12	31	4.2	-14.9	-7.9	6.7
9		15	3	11	31	4.4	-15	-8	6.6
10		15	3	9	31	5.2	-15.2	-8.1	6.7
11		15	3	8	31	5.6	-15.1	-8.2	6.7
12		15	3	6	31	6.3	-15.2	-8.3	6.7
13		15	3	6	30	6.5	-15.1	-8.1	6.8
14		15	3	6	28	6.9	-14.8	-7.8	6.9
15		15	3	6	25	7.6	-14.5	-7.4	6.9
16		15	3	6	23	8.1	-14.3	-7.2	7.1
17		15	3	6	21	8.6	-14	-6.9	7
18		15	3	6	20	8.9	-13.9	-6.8	7.1
19		15	3	6	18	9.4	-13.8	-6.7	7.2
20		15	3	6	16	10.0	-13.6	-6.5	7.4
21		15	3	6	14	10.4	-13.5	-6.4	7.4

Gain Step	RF/ IF	RX_FE_SET [13:10] RX_LNA2_GAIN	RX_FE_SET [9:8] RX_LNA1_GAIN	RX_VGA_SET [11:7] RXVGA2_CTRL	RX_VGA_SET [6:2] RXVGA1_CTRL	Gain Attenuation (dB)	IP1dB (dBm)	IIP3 (dBm)	NF (dB)
22		15	3	6	13	10.8	-13.4	-6.3	7.5
23		15	3	6	11	11.4	-13.3	-6.2	7.8
24		15	3	6	10	11.8	-13.3	-6.1	7.8
25		15	3	6	9	12.3	-13.2	-6	8
26		15	3	6	7	13.1	-13.2	-5.9	8.2
27		15	3	6	6	13.6	-13	-5.9	8.4
28		15	3	6	5	14.1	-13	-5.8	8.5
29		15	3	5	5	14.6	-13.1	-5.8	8.7
30		15	3	6	3	15.0	-13.1	-5.7	8.9
31		15	3	3	5	15.4	-13.2	-5.9	8.8
32		15	3	4	3	16.0	-13.1	-5.7	9.2
33		15	3	3	3	16.3	-13.1	-5.8	9.1
34		15	3	3	2	17.0	-13.1	-5.7	9.5
35		15	3	5	0	17.5	-13	-5.6	10
36		15	3	4	0	18.0	-13	-5.6	10.2
37		15	3	3	0	18.4	-12.9	-5.6	10.2
38		15	3	2	0	18.9	-12.9	-5.6	10.5
39		15	3	0	1	19.5	-13.2	-5.8	10.4
40		15	3	0	0	20.2	-12.9	-5.6	10.9

6.3 RESETB Control

The device can be reset, without power supply cycling, by toggling the RESETB pin from logic high to low. The RESETB pin needs to be asserted back to logic high for normal device operation. During the chip reset, the register contents return to the factory default values.

Table 4. RESETB Control Truth Table

RESETB	State
0	Reset
1	Normal operation

7. Programming

The F5701 uses a standard Serial Peripheral Interface (SPI) protocol for synchronous serial communication. The SPI bus consists of four wire signals: Serial Clock (SCLK), Serial Data In (SDI), Serial Data Out (SDO), and Chip Select Bit (CSB). SPI clock operates up to 65MHz and SCLK pin is associated with the clock signal rising edge. For SPI write transactions, SPI clock can be operated up to 95MHz. The input data stream (addresses, commands, messages, and data) is received on the SDI pin, while the output data stream is transmitted from the SDO pin. The SDO pin shows a high-Z impedance level when the chip is in listen mode. The CSB pin acts as a chip-select pin. All SPI bus pins are synchronous and compatible with multi-chip connection.

There are eight general SPI modes defined by the three mode control bits of all SPI commands as summarized in Table 5. Data is loaded with the most-significant bit (MSB) first and transferred to the input register on the rising edges of SCLK.

Table 5. SPI Modes

Mode Control Bits	Mode of Operation	Description
000	LCL_REG_RD	Local Register Read.
001	LCL_REG_WR	Local Register Write.
010	GBL_LUT_WR	Global LUT Write.
011	GBL_REG_WR	Global Register Write.
100	GBL_FST_GA_SW	Global Fast Gain Switching.
101	LCL_FST_GA_SW	Local Fast Gain Switching.
110	LCL_LUT_WR	Local LUT Write.
111	LCL_LUT_RD	Local LUT Read.

All chips on the SPI bus will be accessed in global operation modes, while in local operation modes, the chip address specifies for which chip the SPI command is intended. The chip address can be either a 3-bit hardwired address (see Pin Information) or a programmable chip address. If a hardwired chip address is used, the 4 MSBs of the 7-bit chip address must be set to 0. To use the programmable chip address functionality (see Shift Register (SHIFTREG)), all chips on the panel need to be daisy-connected.

7.1 Register Read/Write

LCL_REG_RD, LCL_REG_WR, and GBL_REG_WR modes provide access to the available registers for configuring and controlling the chip, including temperature sensor reading. Continuous write is supported for both LCL_REG_WR and GBL_REG_WR modes by appending more 16-bit data sets at the end of the 16-bit data bits (D[15:0]). Any 16-bit data appended is stored in consecutive register addresses.

7.1.1 LCL_REG_RD

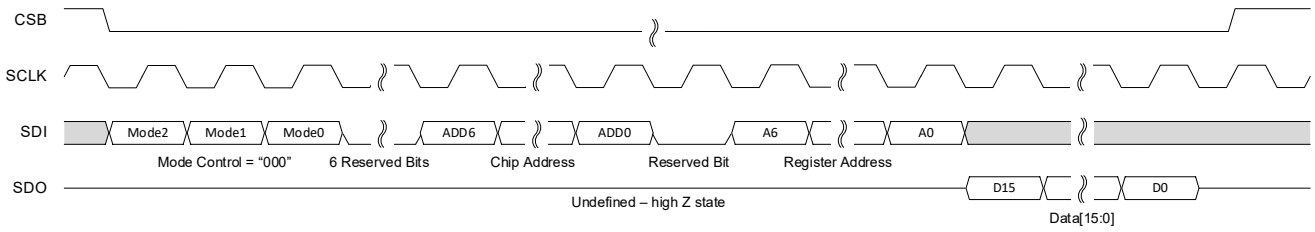

Figure 385. LCL_REG_RD Timing Sequence

Byte1								Byte2								Byte3								Byte4	Byte5
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7:0	7:0
MODE			RES					Chip Address								RES	Register Address							Data Read	
0	0	0	0	0	0	0	0	0	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	0	A6	A5	A4	A3	A2	A1	A0	D[15:8]	D[7:0]

Figure 386. LCL_REG_RD Command Bit Sequence

Table 6. LCL_REG_RD Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Register Read, mode = 000.
2	6:0	Chip Address	7-bit chip address.
3	6:0	Register Address	7-bit register address.
4	7:0	Data byte 1 – D[15:8]	Master sends out the SCLK pulses and data is received on the SDO line.
5	7:0	Data byte 2 – D[7:0]	

7.1.2 LCL_REG_WR

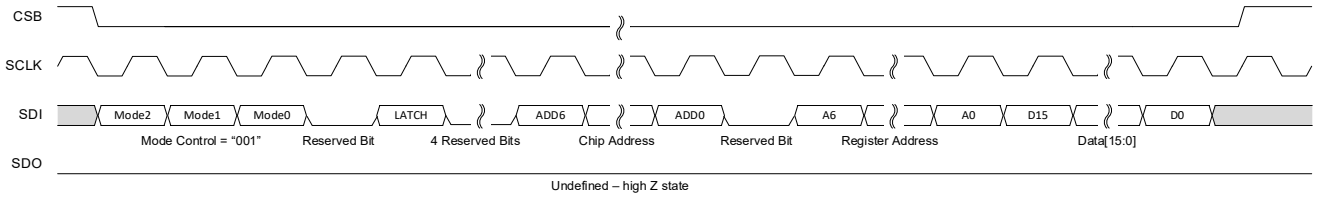

Figure 387. LCL_REG_WR Timing Sequence

Byte1								Byte2								Byte3								Byte4	Byte5
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7:0	7:0
MODE			RF Load		RES			Chip Address								RES	Register Address							Data	
0	0	1	0	LATCH	0	0	0	0	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	0	A6	A5	A4	A3	A2	A1	A0	D[15:8]	D[7:0]

Figure 388. LCL_REG_WR Command Bit Sequence

Table 7. LCL_REG_WR Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Register Write, mode = 001.
1	3	Data Latch	0 = Data is written to the buffer. 1 = Data is written to the buffer as well as the register. This also triggers the latch for all other buffered registers on the chip.
2	6:0	Chip Address	7-bit chip address.
3	6:0	Register Address	7-bit register address.
4	7:0	Data byte 1 – D[15:8]	Data sent on the SDI line will be saved to the buffer or register.
5	7:0	Data byte 2 – D[7:0]	

7.1.3 GBL_REG_WR

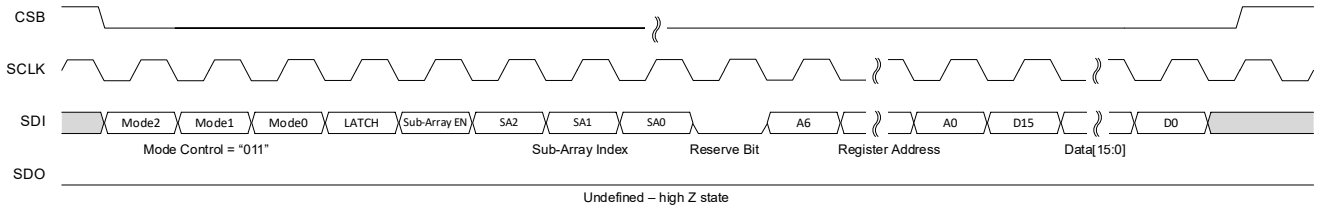

Figure 389. GBL_REG_WR Timing Sequence

Byte1								Byte2								Byte3	Byte4
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7:0	7:0
MODE			RF Load	Sub Array Enable	Sub-Array Idx			RES	Register Address							Data	
0	1	1	LATCH	SE	SA2	SA1	SA0	0	A6	A5	A4	A3	A2	A1	A0	D[15:8]	D[7:0]

Figure 390. GBL_REG_WR Command Bit Sequence

Table 8. GBL_REG_WR Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Register Write, mode = 011.
1	4	Data Latch	0 = Data is written to the buffer. 1 = Data is written to the buffer as well as the register. This also triggers the latch for all other buffered registers on the chip.
1	3	Sub-Array Enable (SE)	0 = Command executed on all chips. 1 = Command executed on chips with matching sub-array.
1	2:0	Sub-Array Index	If SE is set, data is written only when this index matches with the chip's sub-array index (stored in register 0x0).
2	6:0	Register Address	7-bit register address.
3	7:0	Data byte 1 – D[15:8]	Data sent on the SDI line will be saved to the buffer or register.
4	7:0	Data byte 2 – D[7:0]	

7.2 LUT Read/Write

LCL_LUT_RD, LCL_LUT_WR, and GBL_LUT_WR modes provide access to the available LUT for different gain settings. There are 128 total LUT addresses (7-bit) available with each address storing information for VGA and FE (2×16 bits) gain settings. Block selection (VGA/FE) is required for both Read and Write operations. Continuous write is supported by appending 16-bit data sets at the end of the 16-bit data bits (D[15:0]). Any 16-bit data appended are stored in consecutive LUT data blocks as shown by red arrows in Figure 391.

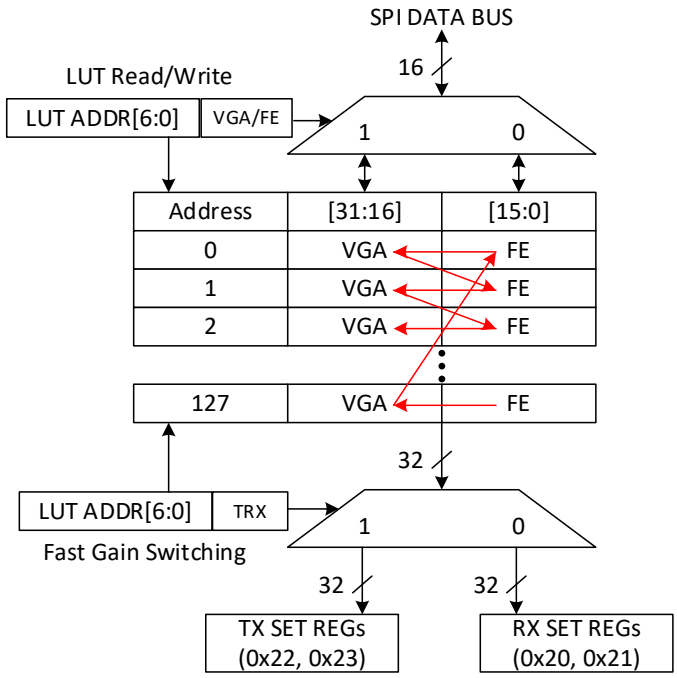

Figure 391. LUT Memory Structure and Control Diagram

7.2.1 LCL_LUT_RD

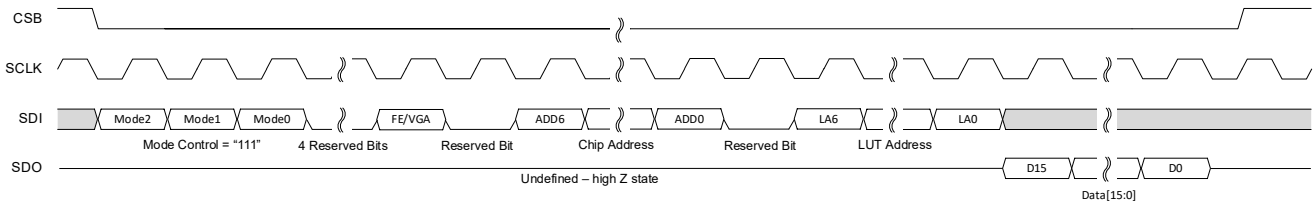

Figure 392. LCL_LUT_RD Timing Sequence

Byte1								Byte2								Byte3								Byte4	Byte5
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7:0	7:0
MODE			RES				FE/VGA	RES	Chip Address							RES	LUT Address							Data	
1	1	1	0	0	0	0	FE/VGA	0	ADD 6	ADD 5	ADD 4	ADD 3	ADD 2	ADD 1	ADD 0	0	LA 6	LA 5	LA 4	LA 3	LA 2	LA 1	LA 0	D[15:8]	D[7:0]

Figure 393. LCL_LUT_RD Command Bit Sequence

Table 9. LCL_LUT_RD Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local LUT Read, mode = 111.
1	0	FE/VGA	FE/VGA LUT block selection: 0 = FE block. 1 = VGA block.
2	6:0	Chip Address	7-bit chip address.
3	6:0	LUT Address	7-bit LUT address.

Byte	Bit	Description	Comment
4	7:0	Data byte 1 – D[15:8]	Master sends out the SCLK pulses and data is received on the SDO line.
5	7:0	Data byte 2 – D[7:0]	

7.2.2 LCL_LUT_WR

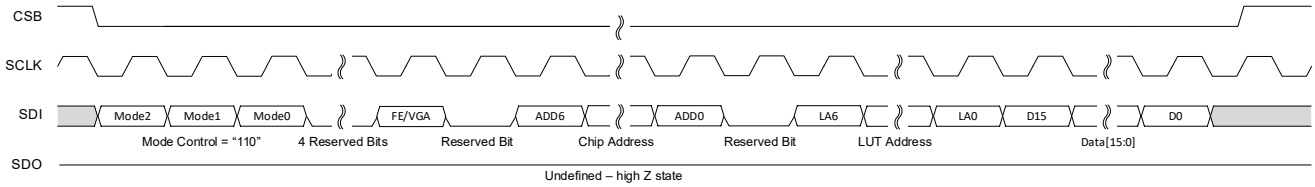

Figure 394. LCL_LUT_WR Timing Sequence

Byte1								Byte2								Byte3								Byte4	Byte5
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7:0	7:0
MODE			RES				FE/VGA	RES	Chip Address							RES	LUT Address							Data	
1	1	0	0	0	0	0	FE/VGA	0	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	0	LA6	LA5	LA4	LA3	LA2	LA1	LA0	D[15:8]	D[7:0]

Figure 395. LCL_LUT_WR Command Bit Sequence

Table 10. LCL_LUT_WR Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local LUT Write, mode = 110.
1	0	FE/VGA	FE/VGA LUT block selection: 0 = FE block. 1 = VGA block.
2	6:0	Chip Address	7-bit chip address.
3	6:0	LUT Address	7-bit LUT address.
4	7:0	Data byte 1 – D[15:8]	Data sent on the SDI is stored to the selected LUT.
5	7:0	Data byte 2 – D[7:0]	

7.2.3 GBL_LUT_WR

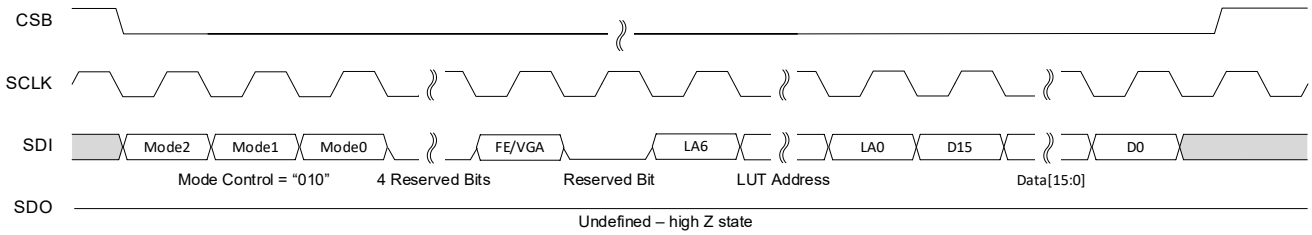

Figure 396. GBL_LUT_WR Timing Sequence

Byte1								Byte2								Byte3	Byte4
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7:0	7:0
MODE			RES				FE/VGA	RES	LUT Address							Data	
0	1	0	0	0	0	0	FE/VGA	0	LA6	LA5	LA4	LA3	LA2	LA1	LA0	D[15:8]	D[7:0]

Figure 397. GBL_LUT_WR Command Bit Sequence

Table 11. GBL_LUT_WR Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Global LUT Write, mode = 010.
1	0	FE/VGA	FE/VGA LUT block selection: 0 = FE block. 1 = VGA block.
2	6:0	LUT Address	7-bit LUT address.
3	7:0	Data byte 1 – D[15:8]	Data sent on the SDI is stored to the selected LUT.
4	7:0	Data byte 2 – D[7:0]	

7.3 Fast Gain Switching

Fast Gain Switching Mode allows for fast configuration of one gain setting in the chip through pre-loaded gain states in memory. The LCL_FST_GA_SW mode programs a single chip with the use of the device address. The GBL_FST_GA_SW mode programs all chips connected to the SPI master. The command includes a LUT address that points to pre-loaded gain settings for TX/RX VGA/FE paths. The Latch bit controls loading of the channel settings. A logic 1 indicates that the updated channel settings are loaded immediately. A logic 0 indicates that the updated settings are stored into a buffer until another Fast Gain Switching Mode command is received with the Latch bit equals 1. Use this feature when both RX and TX settings need to be loaded simultaneously for quick toggle using TRX pin.

7.3.1 LCL_FST_GA_SW

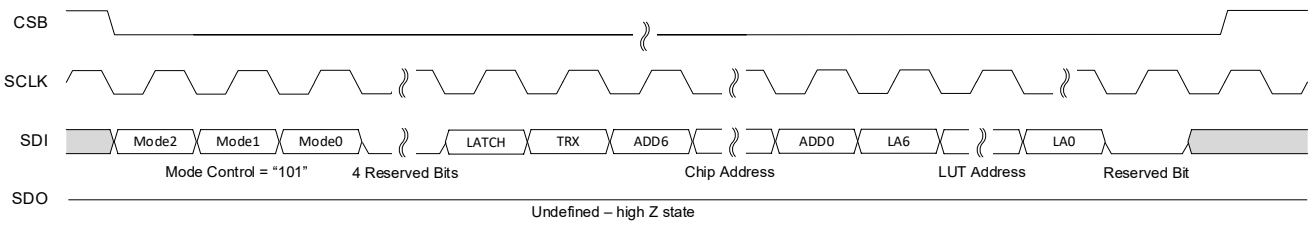

Figure 398. LCL_FST_GA_SW Timing Sequence

Byte1								Byte2								Byte3							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MODE			RES				RF Load	TRX	Chip Address							LUT Address							RES
1	0	1	0	0	0	0	LATCH	TRX	ADD 6	ADD 5	ADD 4	ADD 3	ADD 2	ADD 1	ADD 0	LA6	LA5	LA4	LA3	LA2	LA1	LA0	0

Figure 399. LCL_FST_GA_SW Command Bit Sequence

Table 12. LCL_FST_GA_SW Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Fast Gain Switching, mode = 101.
1	0	Latch	0 = Loads the LUT data only to the buffers. 1 = Loads the LUT data to both the buffers and the SET registers.
2	7	TRX	0 = Loads LUT data to RX channels. Also enables the RX channel. 1 = Loads LUT data to TX channels. Also enables the TX channel.
2	6:0	Chip Address	7-bit chip address.
3	7:1	LUT Address	7-bit LUT address.

7.3.2 GBL_FST_GA_SW

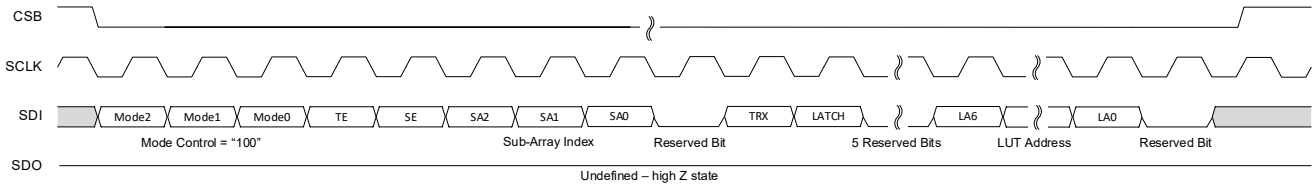

Figure 400. GBL_FST_GA_SW Timing Sequence

Byte1								Byte2								Byte3							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MODE			Toggle	SA Enable	Sub-Array Idx			RES	TRX	RF Load	RES					LUT Address							RES
1	0	0	TE	SE	SA2	SA1	SA0	0	TRX	LATCH	0	0	0	0	0	LA6	LA5	LA4	LA3	LA2	LA1	LA0	0

Figure 401. GBL_FST_GA_SW Command Bit Sequence

Table 13. GBL_FST_GA_SW Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Global Fast Gain Switching, mode = 100.
1	4	Toggle Enable (TE)	0 = No LUT increment. 1 = After byte 3, every SCLK pulse increments the LUT address and loads the contents to the registers.
1	3	Sub-Array Enable (SE)	0 = Command executed on all chips. 1 = Commands executed on chips with matching sub-array.
1	2:0	Sub-Array Index	If SE is set, data is written only when this index matches with the chip's sub-array index (stored in register 0x0).

Byte	Bit	Description	Comment
2	6	TRX	0 = Loads LUT data to RX channels. Also enables the RX channel. 1 = Loads LUT data to TX channels. Also enables the TX channel.
2	5	Latch	0 = Loads the LUT data only to the buffers. 1 = Loads the LUT data to both the buffers and the SET registers.
3	7:1	LUT Address	7-bit LUT address.

Timing requirements for general Read/Write SPI operations are shown and described for a V_{DD} of +2.5V and 50°C ambient temperature.

Table 14. SPI Timing Typical Specifications

Symbol	Test Condition	Minimum	Typical	Maximum	Unit
t_S	CSB to SCLK Setup Time	2	-	-	ns
t_{DS}	SDI Data Setup Time	2	-	-	ns
t_{DH}	SDI Data Hold Time	4.2	-	-	ns
t_{CLK}	SCLK Period	10.5	-	-	ns
t_{HI}	SCLK High Time	5.25	-	-	ns
t_{DO}	SCLK Falling Edge to Valid SDO (first valid output bit in a READ operation)	-	-	5.1	ns
t_H	SCLK to CSB Hold Time	7	-	-	ns
t_{CSB_HI}	CSB High Time	7	-	-	ns

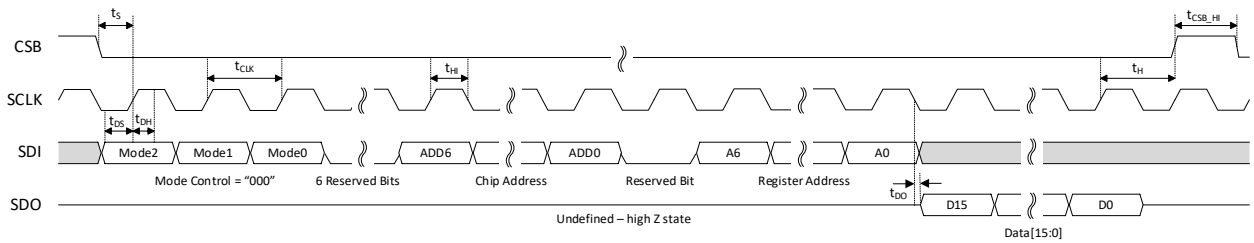

Figure 402. Timing Specification Diagram

8. Register Information

Reset register values stated below are default values after power-on-reset. Recommended register values, summarized in Table 15, need to be programmed by SPI register write for typical operation according to IF and RF frequency settings.

8.1 Control Configuration Register (CTRL_CFG)

Offset Address: 0x00 Reset Value: 0x001F

Bit	Field	Type	Description
15	IO_TEST	WO	IO test mode for IO's VIL/VIH and MISO's VOL/VOH tests, only reset by power-on reset. In IO test mode, MISO pin is the output pin and its logic is RESET OR SPI_CSB OR SPI_CLK OR SPI_MOSI OR ADD1_IN OR ADD2_IN OR ADD3_IN OR ADD4_IN OR STROBE_IN OR TRX_IN.
14	SCAN_MODE	WO	0 = Disable scan mode. 1 = Enable scan mode.
13	RESET	WO	1 = Reset the chip – auto self-reset to 0.
12	RSV	RW	Reserved.
11	STANDBY	RW	0 = Normal operation. 1 = Standby mode, irrespective of STANDBY_SEL. *Note*: the master bias is disabled (MBIAS_EN = 0) in the standby mode.
10:8	SA_IDX	RW	Sub-array index.
7:5	STROBE_PROG	RW	Program the strobe pin functionality. 000 = Latch buffers. 001 = TRX toggle. 010 = TRX toggle. 011 = TRX toggle. 100 = LUT increment (enabled RX/TX). 101 = LUT increment (enabled RX/TX). 110 = LUT increment (enabled RX/TX).
4	LO_SEL	RW	0 = 2x LO. 1 = 4x LO.
3	LO_EN	RW	0 = Disable LO path. 1 = Enable LO path.
2	TRX_SEL	RW	0 = Use an internal signal for TRX toggling. 1 = Use the external TRX pin for TRX toggling.
1	TRn	RW	This bit is identical to LUT[11]. Changing one will change the other. 0 = RX enabled. 1 = TX enabled.
0	TRX_EN	RW	0 = Disable signal paths. 1 = Enable signal paths.

8.2 LUT Address Pointer Register (LUT)

Offset Address: 0x01 Reset Value: 0x0000

Bit	Field	Type	Description
15:12	RSV	RO	Reserved.
11	TRn	RW	This bit is identical to CTRL_CFG[1]. Changing one will change the other. 0 = RX enabled. 1 = TX enabled.
10:4	LUT_PTR	RW	Updated when Global or Local Fast Gain Switching command is issued. When written to, channel SET register buffers are loaded with LUT data.
3:0	RSV	RO	Reserved.

8.3 Shift Register (SHIFTREG)

Offset Address: 0x02 Reset Value: 0x0000

Bit	Field	Type	Description
15:4	RSV	RO	Reserved.
3	OTP_UCOR	RO	Combined non-correctable ECC status: 0 = No uncorrected error detected during OTP read. 1 = More than one bit error was detected. Correction not possible.
2	OTP_COR	RO	Combined correctable ECC status: 0 = No error detected during the OTP read operation. 1 = A bit error was detected and corrected during OTP read operation.
1	SHIFTREG_ADDR_EN	RO	1 = Shift-register address is programmed and effective.
0	SHIFTREG_ADDR_PROG	WO	An 8-bit shift register (shift_reg) is placed between ADD0 pin (IN) and ADD1 pin (OUT). To program a new chip address, set this bit to 1, then without releasing CSB, send in 8-bit data to ADD0 pin, LSB first. Existing data is pushed out of ADD1 pin. New chip address = shift_reg[6:0].

8.4 Master Bias Control Register (MBIAS)

Offset Address: 0x04 Reset Value: 0x8090

Bit	Field	Type	Description
15:12	SCTAT_CTRL	RW	Super CTAT Bias control.
11:9	SCTAT_TRIM	RW	Super CTAT Bias trim.
8	SCTAT_EN	RW	Super CTAT Bias enable.
7:5	PTAT2_SLOPE	RW	$PTAT^2$ slope control.
4:2	PTADJ	RW	Internal reference current generator level control. ±30% reference current adjustment.
1	VBG_SEL	RW	Select band-gap generator. 0 = BG generated from PTAT source. 1 = Brokaw BG generator.
0	MBIAS_EN	RW	Master Bias enable.

8.5 Sensor Control Register (SENS_CTRL)

Offset Address: 0x05 Reset Value: 0x0630

Bit	Field	Type	Description
15:14	RSV	RW	Reserved.
13	TSCORE_SEL	RW	Temperature Sensor Core select.
12	TSENS_EN	RW	Temperature Sensor enable.
11:10	PD_BIAS_BUF_PROF	RW	PDET Buffer Bias profile.
9:7	PD_BIAS_BUF_CTRL	RW	PDET Buffer Bias control.
6:5	PD_BIAS_PROF	RW	PDET Bias profile.
4:2	PD_BIAS_CTRL	RW	PDET Bias control.
1	PD_BIAS_EN	RW	PDET Bias enable.
0	TSENS_CHOPPER_EN	RW	TSENS Chopper enable.

8.6 PDET Control Register (PDET_SW_CTRL)

Offset Address: 0x06 Reset Value: 0x2020

Bit	Field	Type	Description
15:14	RSV	RW	Reserved.
13:12	RXSW_BIAS	RW	RX Switch Bias.
11:7	RSV	RW	Reserved.
6:4	TX_PDET_ATEST	RW	PDET Atest control.
3:2	TX_PDET_RANGE	RW	PDET power range.
1	TX_PDET_AMPEN	RW	PDET differential amplifier enable.
0	TX_PDET_EN	RW	PDET enable.

8.7 Chip ID Register (CHIP_ID)

Offset Address: 0x07 Reset Value: 0x5111

Bit	Field	Type	Description
15:14	ID_CLASS	RO	0 = Beamformer. 1 = Up/Down Converter.
13:12	ID_FREQ	RO	1 = 26GHz/28GHz.
11:8	BASE_REV	RO	Base layer revision. 1 = V1XY. 2 = V2XY.
7:4	METAL_REV	RO	Metal layer revision. X in V1XY.
3:0	VARIANTS	RO	Variant number. Y in V1XY.

8.8 SRAM BIST Register (BIST)

Offset Address: 0x08 Reset Value: 0x0000

Bit	Field	Type	Description
15:8	RSV	RO	Reserved.
7	SRAM_DONE	RO	SRAM access (initialization, BIST, or CRC) status. 0 = SRAM access is requested. 1 = SRAM access is done.
6:4	SRAM_ERR	RO	Number of SRAM error times during SRAM BIST. When the number exceeds 7, it will be kept at 7.
3	RSV	RW	Reserved.
2	SRAM_CRC	RW	SRAM CRC check request. Request SRAM CRC by writing 1. The SRAM CRC algorithm is as follows: 1. Initial value is 0xFFFF. 2. CRC generator is $x^{16} + x^{12} + x^5 + 1$. 3. The sequence is: • N = 0 • Get data from LUT[N] • Do CRC on channel 1 data (bit11, bit 10, …, bit1, bit0) • Do CRC on channel 2, 3, and 4 • If N =1023, finish CRC check; else do N = N + 1 and go to step b.
1	SRAM_BIST	RW	SRAM BIST request. Request SRAM BIST by writing 1.
0	SRAM_INIT	RW	SRAM initialization request (initialize all SRAM data to 0). Request SRAM initialization by writing 1.

8.9 SRAM CRC Result Register (CRC_RESULT)

Offset Address: 0x09 Reset Value: 0xFFFF

Bit	Field	Type	Description
15:0	CRC_RESULT	RO	16-bit SRAM CRC result.

8.10 ADC Channel Select Register (ADC_SEL)

Offset Address: 0x0A Reset Value: 0x0000

Bit	Field	Type	Description
15	ADC_BG	RW	ADC channel 16: 50μA BG x 10kΩ R_{poly_lo}. Output data saved in register address 0x5F.
14	ADC_PT2	RW	ADC channel 15: 50μA PT2 x 10kΩ R_{poly_lo}. Output data saved in register address 0x5E.
13	ADC_PT	RW	ADC channel 14: 50μA PT x 10kΩ R_{poly_lo}. Output data saved in register address 0x5D.
12	ADC_RXDACM	RW	ADC channel 13: Vdacm/2. Output data saved in register address 0x5C.

Bit	Field	Type	Description
11	ADC_RXDACP	RW	ADC channel 12: Vdacp/2. Output data saved in register address 0x5B.
10	ADC_DVDD_BY_4	RW	ADC channel 11: DVDD/4. Output data saved in register address 0x5A.
9	ADC_VDD_BY_5	RW	ADC channel 10: VDD/5. Output data saved in register address 0x59.
8	ADC_TSENS	RW	ADC channel 9: Main temperature sensor. Output data saved in register address 0x58.
7	ADC_TX_PD_HWDIFF	RW	ADC channel 8: TX PDET HW Diff. Output data saved in register address 0x57.
6	ADC_RXLO_PDREF	RW	ADC channel 7: RXLO output PDET reference. Output data saved in register address 0x56.
5	ADC_TXLO_PDREF	RW	ADC channel 6: TXLO output PDET reference. Output data saved in register address 0x55.
4	ADC_TX_PDREF	RW	ADC channel 5: TX PDET reference. Output data saved in register address 0x54.
3	ADC_AOUT	RW	ADC channel 4: AOUT loop-back to ADC. Ensure AOUT_EN=0. Output data saved in register address 0x53.
2	ADC_RXLO_PD	RW	ADC channel 3. To run ADC on RXLO PDET, both ADC_RXLO_PD and ADC_RXLO_PDREF should be set to 1. Output data saved in register address 0x52. If PD_DIFF_MODE = 0: output = normalized RXLO PDET ADC readout (PD – PDREF). If PD_DIFF_MODE = 1: output = absolute RXLO PDET ADC readout.
1	ADC_TXLO_PD	RW	ADC channel 2. To run ADC on TXLO PDET, both ADC_TXLO_PD and ADC_TXLO_PDREF should be set to 1. Output data saved in register address 0x51. If PD_DIFF_MODE = 0: output = normalized TXLO PDET ADC readout (PD – PDREF). If PD_DIFF_MODE = 1: output = absolute TXLO PDET ADC readout.
0	ADC_TX_PD	RW	ADC channel 1. To run ADC on TX PDET, both ADC_TX_PD and ADC_TX_PDREF should be set to 1. Output data saved in register address 0x50. If PD_DIFF_MODE = 0: output = normalized TX PDET ADC readout (PD – PDREF). If PD_DIFF_MODE = 1: output = absolute TX PDET ADC readout.

8.11 ADC Control Register (ADC_CTRL)

Offset Address: 0x0B Reset Value: 0x0000

Bit	Field	Type	Description
15:12	RSV	RW	Reserved.
11	I_TEST_EXT	RW	Currents from ADC_EXT5-7 are sent to the AOUT port instead of the internal resistor.
10	PD_DIFF_MODE	RW	0 = Default setting. Normalized PDET ADC readout (PD - PDREF) calculated by the software and stored as the result for ADC_RXLO_PD, ADC_TXLO_PD, and ADC_TX_PD. 1 = No software difference calculation.
9:8	OSC_FREQ	RW	Oscillator frequency. 0 = 80MHz. 1 = 40MHz. 2 = 20MHz. 3 = OFF.
7	OSC_EN	RW	Oscillator enable.
6:5	AOUT_SEL	RW	AOUT mux selection. 0 = ADC input specified by registers ADC_SEL1 and ADC_SEL2. 1 = cbn1_test. 2 = vref(v1p5). 3 = vcm(v0p9).
4	AOUT_EN	RW	AOUT mux enable.
3	LSB_SEL	RW	Turn down LSB. 0 = LSB is Vref/1023. 1 = LSB is Vref/1055.
2	CHOPPER_EN	RW	Chopper enable.
1	ADC_I_2X	RW	Double ADC bias current.
0	ADC_START	RW	Start ADC operation.

8.12 ADC Clock Control Register (ADC_CLK)

Offset Address: 0x0C Reset Value: 0x0B30

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14:12	ADC_AVG	RW	0 = No averaging. 1–6 = Averaging count = 2^{ADC_AVG}. 7 = Averaging count = 2^6.
11:8	BASE_CLK_CTRL	RW	Select base clock (BASE_CLK) as OSC_60MHz/(N+1).
7:4	ADC_CLK_HIGH	RW	Select ADC clock’s high width as BASE_CLK*(N+1).
3:0	ADC_CLK_LOW	RW	Select ADC clock’s low width as BASE_CLK*(N+1).

8.13 OTP Control Register (OTP_CTRL)

Offset Address: 0x0D Reset Value: 0x4014

Bit	Field	Type	Description
15	OTP_FSM_START	WO	Start FSM for OTP read operation.
14	OTP_ECC_DIS	RW	0 = OTP Error Correction enabled. 1 = OTP Error Correction Coding disabled.
13	OTP_DIN_LATCH	WO	Latch data from otp_din[7:0] to OTP_DATAn (n = 1 to 7).
12:10	OTP_WR_BIT	RW	Bit number to burn during program mode.
9:6	OTP_RW_ADDRESS	RW	OTP Read/Write address back selection.
5	OTP_PROG	RW	OTP program mode.
4	OTP_POR	RW	OTP POR.
3:2	OTP_CUR	RW	OTP current control.
1	OTP_READ	RW	OTP Read enable.
0	OTP_EN	RW	OTP enable.

8.14 OTP ECC Status Register (OTP_ECC_STATUS)

Offset Address: 0x0E Reset Value: 0x0000

Bit	Field	Type	Description
15:8	OTP_ECC_UCOR	RO	Per DATA_OTPn non-correctable ECC status: 0 = No uncorrected error detected during OTP read. 1 = More than one bit error was detected. Correction not possible.
7:0	OTP_ECC_COR	RO	Per DATA_OTPn correctable ECC status: 0 = No error detected during OTP read operation. 1 = A bit error was detected and corrected during OTP read operation.

8.15 PCM Control Register (PCM_CTRL)

Offset Address: 0x0F Reset Value: 0x0038

Bit	Field	Type	Description
15:7	RSV	RO	Reserved.
6:3	PCM_CLK_DIV	RW	Counter duration = Tspi_clk/(PCM_CLK_DIV+1).
2:1	PCM_CH_SEL	RW	PCM channel selection. 0 = BJT ring oscillator. 1 = R ring oscillator. 2 = RC ring oscillator.
0	PCM_START	RW	PCM start (auto-reset).

8.16 TRX Enable Register (TRX_ENABLE)

Offset Address: 0x10 Reset Value: 0xFFFF

Bit	Field	Type	Description
15	TX_BIAS_EN	RW	TX bias enable.
14	TX_PA_EN	RW	TX PA enable.
13	TX_DRV_EN	RW	TX DRV enable.
12	TX_MXR_EN	RW	TX mixer enable.
11	TX_LO_DRV_EN	RW	TX LO DRV enable.
10	TXVGA_BIAS_EN	RW	TX VGA bias enable.
9	TXVGA2_EN	RW	TX VGA2 enable.
8	TXVGA1_EN	RW	TX VGA1 enable.
7	RX_BIAS_EN	RW	RX bias enable.
6	RX_LNA1_EN	RW	RX LNA1 enable.
5	RX_LNA2_EN	RW	RX LNA2 enable.
4	RX_MXR_EN	RW	RX mixer enable.
3	RX_LO_DRV_EN	RW	RX LO DRV enable.
2	RXVGA_BIAS_EN	RW	RX VGA bias enable.
1	RXVGA2_EN	RW	RX VGA2 enable.
0	RXVGA1_EN	RW	RX VGA1 enable.

8.17 TRX Warm-up Register (TRX_WARMUP)

Offset Address: 0x11 Reset Value: 0x0000

Bit	Field	Type	Description
15	TX_BIAS_WU	RW	TX bias warm-up.
14	TX_PA_WU	RW	TX PA warm-up.
13	TX_DRV_WU	RW	TX DRV warm-up.
12	TX_MXR_WU	RW	TX mixer warm-up.
11	TX_LO_DRV_WU	RW	TX LO DRV warm-up.
10	TXVGA_BIAS_WU	RW	TX VGA bias warm-up.
9	TXVGA2_WU	RW	TX VGA2 warm-up.
8	TXVGA1_WU	RW	TX VGA1 warm-up.
7	RX_BIAS_WU	RW	RX bias warm-up.
6	RX_LNA1_WU	RW	RX LNA1 warm-up.
5	RX_LNA2_WU	RW	RX LNA2 warm-up.
4	RX_MXR_WU	RW	RX mixer warm-up.
3	RX_LO_DRV_WU	RW	RX LO DRV warm-up.
2	RXVGA_BIAS_WU	RW	RX VGA bias warm-up.

Bit	Field	Type	Description
1	RXVGA2_WU	RW	RX VGA2 warm-up.
0	RXVGA1_WU	RW	RX VGA1 warm-up.

8.18 Envelope Detector Register (ENV_DET)

Offset Address: 0x12 Reset Value: 0x7292

Bit	Field	Type	Description
15	ENV_EN	RW	Envelope detector enable.
14:13	ENV_GAIN	RW	Second-stage amplifier gain control.
12:10	ENV_DET_CTRL	RW	Detector core bias control.
9:8	ENV_CH_CTRL	RW	Detector channel bias control.
7:5	ENV_BUFF_CTRL	RW	First-stage buffer bias control.
4:2	ENV_AMP_CTRL	RW	Amplifier bias control.
1:0	ENV_BUFF2_CTRL	RW	Second-stage buffer bias control.

8.19 TOP Spare Register (SPARE)

Offset Address: 0x13 Reset Value: 0x0000

Bit	Field	Type	Description
15:0	RSV	RW	Reserved.

8.20 PCM Data Register 1 (DATA_PCM1)

Offset Address: 0x15 Reset Value: 0x0000

Bit	Field	Type	Description
15:12	RSV	RO	Reserved.
11:0	DATA_CH1	RO	CH1: BJT.

8.21 PCM Data Register 2 (DATA_PCM2)

Offset Address: 0x16 Reset Value: 0x0000

Bit	Field	Type	Description
15:12	RSV	RO	Reserved.
11:0	DATA_CH2	RO	CH2: R.

8.22 PCM Data Register 3 (DATA_PCM3)

Offset Address: 0x17 Reset Value: 0x0000

Bit	Field	Type	Description
15:12	RSV	RO	Reserved.
11:0	DATA_CH3	RO	CH3: RC.

8.23 OTP Data Register 1 (DATA_OTP1)

Offset Address: 0x18 Reset Value: 0x0000

Bit	Field	Type	Description
15:8	DATA_OTP_REG1	RW	OTP address = 4'd1.
7:0	DATA_OTP_REG0	RW	OTP address = 4'd0.

8.24 OTP Data Register 2 (DATA_OTP2)

Offset Address: 0x19 Reset Value: 0x0000

Bit	Field	Type	Description
15:8	DATA_OTP_REG3	RW	OTP address = 4'd3.
7:0	DATA_OTP_REG2	RW	OTP address = 4'd2.

8.25 OTP Data Register 3 (DATA_OTP3)

Offset Address: 0x1A Reset Value: 0x0000

Bit	Field	Type	Description
15:8	DATA_OTP_REG5	RW	OTP address = 4'd5.
7:0	DATA_OTP_REG4	RW	OTP address = 4'd4.

8.26 OTP Data Register 4 (DATA_OTP4)

Offset Address: 0x1B Reset Value: 0x0000

Bit	Field	Type	Description
15:8	DATA_OTP_REG7	RW	OTP address = 4'd7.
7:0	DATA_OTP_REG6	RW	OTP address = 4'd6.

8.27 OTP Data Register 5 (DATA_OTP5)

Offset Address: 0x1C Reset Value: 0x0000

Bit	Field	Type	Description
15:8	DATA_OTP_REG9	RW	OTP address = 4'd9.
7:0	DATA_OTP_REG8	RW	OTP address = 4'd8.

8.28 OTP Data Register 6 (DATA_OTP6)

Offset Address: 0x1D Reset Value: 0x0000

Bit	Field	Type	Description
15:8	DATA_OTP_REG11	RW	OTP address = 4'd11.
7:0	DATA_OTP_REG10	RW	OTP address = 4'd10.

8.29 OTP Data Register 7 (DATA_OTP7)

Offset Address: 0x1E Reset Value: 0x0000

Bit	Field	Type	Description
15:8	DATA_OTP_REG13	RW	OTP address = 4'd13.
7:0	DATA_OTP_REG12	RW	OTP address = 4'd12.

8.30 OTP Data Register 8 (DATA_OTP8)

Offset Address: 0x1F Reset Value: 0x0000

Bit	Field	Type	Description
15:8	DATA_OTP_REG15	RW	OTP address = 4'd15.
7:0	DATA_OTP_REG14	RW	OTP address = 4'd14.

8.31 RX VGA SET Register (RX_VGA_SET)

Offset Address: 0x20 Reset Value: 0x07BF

Bit	Field	Type	Description
15:12	RSV	RW	Reserved.
11:7	RXVGA2_CTRL	RW	RX VGA2 gain control.
6:2	RXVGA1_CTRL	RW	RX VGA1 gain control.
1	RSV	RW	Reserved.
0	RXVGA_SW_0p25	RW	Provide 0.25dB step.

8.32 RX FE SET Register (RX_FE_SET)

Offset Address: 0x21 Reset Value: 0xFF44

Bit	Field	Type	Description
15:14	RX_LNA2_FB	RW	RX LNA2 feedback control.
13:10	RX_LNA2_GAIN	RW	RX LNA2 gain control.
9:8	RX_LNA1_GAIN	RW	RX LNA1 gain control. 0 = -6dB. 1 = -3dB. 2 = -3dB. 3 = 0dB.
7	RSV	RW	Reserved.
6:4	RXVGA2_BIAS	RW	RX VGA2 bias.
3:0	RXVGA1_BIAS	RW	RX VGA1 bias.

8.33 TX VGA SET Register (TX_VGA_SET)

Offset Address: 0x22 Reset Value: 0x3087

Bit	Field	Type	Description
15:13	TXVGA1_RTUNE	RW	TX VGA1 output resistance tuning.
12	TXVGA1_PT_PT2	RW	TX VGA1 bias selection: 0 = PTAT. 1 = BG.
11:7	TXVGA2_CTRL	RW	TX VGA2 gain control.
6:2	TXVGA1_CTRL	RW	TX VGA1 gain control.
1	RSV	RW	Reserved.
0	TXVGA_SW_0p25	RW	Provide 0.25dB step.

8.34 TX FE SET Register (TX_FE_SET)

Offset Address: 0x23 Reset Value: 0x0F44

Bit	Field	Type	Description
15:12	RSV	RW	Reserved.
11:8	TX_RFVGA_GAIN	RW	TX RFVGA gain control.
7	TXVGA2_PT_PT2	RW	0 = PTAT. 1 = $PTAT^2$.
6:4	TXVGA2_BIAS	RW	TX VGA2 bias.
3:0	TXVGA1_BIAS	RW	TX VGA1 bias.

8.35 RX LNA1 Bias Register (RX_LNA1_BIAS)

Offset Address: 0x24 Reset Value: 0x1684

Bit	Field	Type	Description
15:14	RX_BALUN_CTUNE	RW	RX LNA1 balun tuning.
13:12	RX_LNA1_CTUNE	RW	RX LNA1 frequency tuning.
11:10	RX_LNA1_RTUNE	RW	RX LNA1 output resistor control.
9:8	RX_LNA1_CASC_BIAS	RW	RX LNA1 cascode bias.
7:5	RX_LNA1_BIAS	RW	RX LNA1 bias.
4:3	RX_LNA_PT_PT2_BG	RW	RX LNA bias selection: 0 = PTAT. 1 = $PTAT^2$. 2 = BG.
2:0	RX_BIAS	-	RX bias.

8.36 RX LNA2 Bias Register (RX_LNA2_BIAS)

Offset Address: 0x25 Reset Value: 0x0034

Bit	Field	Type	Description
15:10	RSV	RW	Reserved.
9	RX_SEL	RW	RX path selection. 0 = TRX path enabled. 1 = RX2 path enabled.
8:7	RX_LNA2_CTUNE	RW	RX LNA2 frequency tuning.
6:5	RX_LNA2_RTUNE	RW	RX LNA2 output resistor tuning.
4:3	RX_LNA2_CASC_BIAS	RW	RX LNA2 cascode bias.
2:0	RX_LNA2 _BIAS	RW	RX LNA2 bias.

8.37 RX Mixer Bias Register (RX_MIX_BIAS)

Offset Address: 0x26 Reset Value: 0x0184

Bit	Field	Type	Description
15:10	RSV	RW	Reserved.
9:8	RX_MIX_LOBIAS	RW	RX mixer switch base voltage selection.
7:5	RX_MIX_FEED	RW	RX mixer Gm-feed bias.
4:3	RX_MIX_PT_PT2_BG	RW	RX mixer bias selection: 0 = PTAT. 1 = $PTAT^2$. 2 = BG.
2:0	RX_MIX_BIAS	-	RX mixer bias.

8.38 RX Mixer DAC Register (RX_MIX_DAC)

Offset Address: 0x27 Reset Value: 0x1100

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14	RX_ DAC_VCM_RANGE	RW	0 = Default VCM range of both DACs (1.3V–1.9V). 1 = VCM range shifted to higher voltage (1.5V–2.1V).
13	RX_DAC_VCM_CMN	RW	0 = Separate VCM control for mixer DAC and LODRV DAC. 1 = Same VCM for mixer DAC and LODRV DAC.
12:9	RX_MIX_DAC_VCM	RW	RX mixer DAC common mode voltage control.
8:0	RX_MIX_DAC	-	RX mixer DAC fine tuning.

8.39 RX LO Driver Bias Register (RX_LODRV_BIAS)

Offset Address: 0x28 Reset Value: 0x2A24

Bit	Field	Type	Description
15:14	RSV	RW	Reserved.
13:12	RX_LODRV_VCASC	RW	RX LO driver cascode voltage control.
11:10	RX_LODRV_QCTUNE	RW	RX LO driver Q-channel frequency tuning.
9:8	RX_LODRV_ICTUNE	RW	RX LO driver I-channel frequency tuning.
7:6	RX_LODRV_PT_PT2_BG	RW	RX LO driver bias selection: 0 = PTAT. 1 = $PTAT^2$. 2 = BG.
5:3	RX_LODRV_QBIAS	RW	RX LO driver Q-channel bias.
2:0	RX_LODRV_IBIAS	RW	RX LO driver Q-channel bias.

8.40 RX LO Polyphase Filter DAC Register (RX_LOPPF_DAC)

Offset Address: 0x29 Reset Value: 0x1100

Bit	Field	Type	Description
15:13	RSV	RW	Reserved.
12:9	RX_LOPPF_DAC_VCM	RW	RX LO PPF DAC common mode voltage.
8:0	RX_LOPPF_DAC	RW	RX LO PPF DAC fine tuning (LO phase tuning).

8.41 RX IF Polyphase Filter Register (RX_PPF)

Offset Address: 0x2A Reset Value: 0x0036

Bit	Field	Type	Description
15:6	RSV	RW	Reserved.
5:3	RX_IFPPF_CTUNE2	RW	RX IF PPF 2^{nd}-stage frequency tuning.
2:0	RX_IFPPF_CTUNE1	RW	RX IF PPF 1^{st}-stage frequency tuning.

8.42 RX Spare Register (RX_SPARE)

Offset Address: 0x2B Reset Value: 0x0000

Bit	Field	Type	Description
15:0	RSV	RW	Reserved.

8.43 RX VGA Register (RX_VGA)

Offset Address: 0x2C Reset Value: 0x03F4

Bit	Field	Type	Description
15:11	RSV	RW	Reserved.
10:9	RXVGA2_CTUNE_SEC	RW	RX VGA2 transformer output tuning.
8:7	RXVGA2_CTUNE_PRI	RW	RX VGA2 transformer input tuning.
6:5	RXVGA1_CTUNE	RW	RX VGA1 transformer output tuning.
4	RXVGA2_PT_PT2	RW	RX VGA2 bias selection: 0 = PTAT. 1 = $PTAT^2$.
3	RXVGA1_PT_PT2	RW	RX VGA1 bias selection: 0 = PTAT. 1 = $PTAT^2$.
2:0	RXVGA_BIAS	RW	RX VGA bias.

8.44 TX PA Bias Register (TX_PA_BIAS)

Offset Address: 0x30 Reset Value: 0x6B3C

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14	TX_PA_RFFB_CTRL	RW	TX PA feedback control.
13	TX_PA_BG_PT	RW	TX PA bias selection: 0 = PTAT, 1 = BG.
12:11	TX_PA_OUT_MATCH	RW	TX PA output frequency match.
10:9	TX_PA_CASC_CAP	RW	TX PA cascode capacitance control.
8:6	TX_PA_CASC_BIAS	RW	TX PA cascode bias control.
5:4	TX_PA_BIAS_R	RW	TX PA bias resistance control.
3:0	TX_PA_BIAS	RW	TX PA bias.

8.45 TX Driver Bias Register (TX_DRV_BIAS)

Offset Address: 0x31 Reset Value: 0x3FCC

Bit	Field	Type	Description
15:14	TX_DRV_PT_PT2_BG	RW	TX driver bias selection: 0 = PTAT. 1 = $PTAT^2$. 2 = BG.
13:12	TX_DRV_INTER_MATCH	RW	TX driver-PA interstage match.
11:10	TX_DRV_IN_MATCH	RW	TX driver input match.
9:7	TX_DRV_CASC_BIAS	RW	TX driver cascode bias.
6:3	TX_DRV_BIAS	RW	TX driver bias.
2:0	TX_BIAS	RW	TX channel bias.

8.46 TX RF VGA Register (TX_RFVGA)

Offset Address: 0x32 Reset Value: 0x0192

Bit	Field	Type	Description
15:9	RSV	RW	Reserved.
8	TX_RFVGA_EN	RW	TX RF VGA enable.
7	TX_RFVGA_RDAMP	RW	TX RF VGA output resistance control.
6:5	TX_RFVGA_PT_PT2_BG	RW	TX RF VGA bias selection: 0 = PTAT. 1 = $PTAT^2$. 2 = BG.
4:3	TX_RFVGA_VCASC	RW	TX RF VGA cascode control.
2:0	TX_RFVGA_BIAS	RW	TX RF VGA bias.

8.47 TX Mixer Bias Register (TX_MIX_BIAS)

Offset Address: 0x33 Reset Value: 0x1824

Bit	Field	Type	Description
15:14	TX_PA_OUT_match2	RW	TX PA output match.
13	TX_IFPPF_CTUNE	RW	TX IF PPF frequency tuning.
12:11	TX_MXR_VCASC	RW	TX mixer cascode voltage.
10:9	TX_MXR_PT_PT2_BG	RW	TX mixer bias selection: 0 = PTAT. 1 = $PTAT^2$. 2 = BG.
8:7	TX_MXR_CTUNE	RW	TX mixer frequency tuning.
6	TX_MXR_RTUNE	RW	TX mixer output resistance control.
5:3	TX_MXRI_BIAS	RW	TX mixer I-channel bias.
2:0	TX_MXRQ_BIAS	RW	TX mixer Q-channel bias.

8.48 TX LO Driver Bias Register (TX_LODRV_BIAS)

Offset Address: 0x34 Reset Value: 0x0224

Bit	Field	Type	Description
15:14	RSV	RW	Reserved.
13:12	TX_LO_PT_PT2_BG	RW	TX LO driver bias selection: 0 = PTAT. 1 = $PTAT^2$. 2 = BG.
11:10	TX_LODRV_CTUNEQ	RW	TX LO driver Q-channel frequency tuning.
9:8	TX_LODRV_VCASC	RW	TX LO driver cascode voltage.
7:6	TX_LODRV_CTUNEI	RW	TX LO driver I-channel frequency tuning.
5:3	TX_LODRV_QBIAS	RW	TX LO driver Q-channel bias.
2:0	TX_LODRV_IBIAS	RW	TX LO driver I-channel bias.

8.49 TX Q-Channel DAC Register (TX_QDAC)

Offset Address: 0x35 Reset Value: 0x0100

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14	TX_LO_VCM_RANGE	RW	0 = Default VCM range (1.3V–1.9V). 1 = Increased VCM range (1.5V–2.1V).
13	TX_DAC_VCM_CMN	RW	0 = Use separate VCM for TX DACI and TX DACQ. 1 = Use TX_DACI_VCM to control both VCMs.
12:9	TX_DACQ_VCM	RW	TX Q-channel mixer bias DAC common mode control.
8:0	TX_DACQ	RW	TX Q-channel mixer bias DAC fine control.

8.50 TX I-Channel DAC Register (TX_IDAC)

Offset Address: 0x36 Reset Value: 0x0100

Bit	Field	Type	Description
15:13	RSV	RW	Reserved.
12:9	TX_DACI_VCM	RW	TX Q-channel mixer bias DAC common mode control.
8:0	TX_DACI	RW	TX Q-channel mixer bias DAC fine control.

8.51 TX Spare Register (TX_SPARE)

Offset Address: 0x37 Reset Value: 0x0000

Bit	Field	Type	Description
15:0	RSV	RW	Reserved.

8.52 TX VGA Register (TX_VGA)

Offset Address: 0x38 Reset Value: 0x81FC

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14:12	TXVGA2_SEC_CTUNE	RW	TX VGA2 secondary capacitance tuning.
11:9	TXVGA2_PRI_CTUNE	RW	TX VGA2 primary capacitance tuning.
8:7	TXVGA1_SEC_CTUNE	RW	TX VGA1 secondary capacitance tuning.
6:3	TXVGA1_PRI_CTUNE	RW	TX VGA1 primary capacitance tuning.
2:0	TXVGA_BIAS	RW	TX VGA bias capacitance tuning.

8.53 RX LO CT Register (RXLO_CT)

Offset Address: 0x40 Reset Value: 0x2134

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14:13	RXLO_BUF_CASC	RW	RX LO input buffer cascode tuning.
12:11	RXLO_BUF_PT_PT2_BG	RW	RX LO input buffer bias selection: 0 = PTAT. 1 = $PTAT^2$. 2 = BG.
10:9	RXLO_MULT_PT_PT2_BG	RW	RX LO multiplier bias selection: 0 = PTAT. 1 = $PTAT^2$. 2 = BG.
8:6	RXLO_CH_BIAS	RW	RX LO bias.
5:3	RXLO_VGA_CTRL	RW	RX LO VGA control.
2:0	RXLO_CT_4X	RW	RX LO 4x frequency tuning.

8.54 RX LO Bias Register (RXLO_BIAS)

Offset Address: 0x41 Reset Value: 0x4924

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14:12	RXLO_VGA_BIAS	RW	RX LO NFET bias control for both multiplier and buffers.
11:9	RXLO_BIAS_BUF	RW	RX LO output buffer bias.
8:6	RXLO_BIAS_BUF_10G	RW	RX LO 4x buffer bias.
5:3	RXLO_BIAS_2X	RW	RX LO 2x doubler bias.
2:0	RXLO_BIAS_4X	RW	RX LO 4x doubler bias.

8.55 RXLO Spare Register (RXLO_SPARE)

Offset Address: 0x42 Reset Value: 0x000C

Bit	Field	Type	Description
15:5	RSV	RW	Reserved.
4	RXLO_MULT_CTUNE	RW	1-bit capacitance switch at the collector side of the doubler output transformer.
3	RXLO_VGA_CTUNE	RW	1-bit capacitance switch at the collector side of the VGA output transformer.
2:0	RXLO_BIAS_INBUFF	RW	Bias control for the limiter/buffer.

8.56 TX LO CT Register (TXLO_CT)

Offset Address: 0x43 Reset Value: 0x2134

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14:13	TXLO_BUF_CASC	RW	TX LO input buffer cascode tuning.
12:11	TXLO_BUF_PT_PT2_BG	RW	TX LO input buffer bias selection: 0 = PTAT. 1 = $PTAT^2$. 2 = BG.
10:9	TXLO_MULT_PT_PT2_BG	RW	TX LO multiplier bias selection: 0 = PTAT. 1 = $PTAT^2$. 2 = BG.
8:6	TXLO_CH_BIAS	RW	TX LO bias.
5:3	TXLO_VGA_CTRL	RW	TX LO VGA control.
2:0	TXLO_CT_4X	RW	TX LO 4x frequency tuning.

8.57 TX LO Bias Register (TXLO_BIAS)

Offset Address: 0x44 Reset Value: 0x4924

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14:12	TXLO_VGA_BIAS	RW	TX LO NFET bias control for both multiplier and buffers.
11:9	TXLO_BIAS_BUF	RW	TX LO output buffer bias.
8:6	TXLO_BIAS_BUF_10G	RW	TX LO 4x buffer bias.
5:3	TXLO_BIAS_2X	RW	TX LO 2x doubler bias.
2:0	TXLO_BIAS_4X	RW	TX LO 4x doubler bias.

8.58 TXLO Spare Register (TXLO_SPARE)

Offset Address: 0x45 Reset Value: 0x000C

Bit	Field	Type	Description
15:5	RSV	RW	Reserved.
4	TXLO_MULT_CTUNE	RW	1-bit capacitance switch at the collector side of the doubler output transformer.
3	TXLO_VGA_CTUNE	RW	1-bit capacitance switch at the collector side of the VGA output transformer.
2:0	TXLO_BIAS_INBUFF	RW	Bias control for the limiter/buffer.

8.59 ADC DATA Register (DATA_ADC_CHn) (n = 0 to 15)

Offset Address: 0x50 + Reset Value: 0x0000

Bit	Field	Type	Description
15:11	RSV	RO	Reserved.
10	DONE	RO	ADC status.
9:0	VALUE	RO	ADC data.

Table 15. Recommended Register Settings

Address	Register	Recommended Value				
		Band H8 26.5–29.5 GHz RF/ 3.5-7GHz IF	**Band H6 24.25–27.5 GHz RF/ 3.5-7GHz IF**	**Band L8 26.5–29.5 GHz RF/ 2.5-4GHz IF**	**Band L6 24.25–27.5 GHz RF/ 2.5-4GHz IF**	**Band H6h 24.25-27.5 GHz RF/ 3.5-7 GHz IF (High Linearity Mode)**
0x4	MBIAS	0x8991	0x8991	0x8991	0x8991	0x8991
0x5	SENS_CTRL	0x0630	0x0630	0x0630	0x0630	0x0630
0x6	PDET_SW_CTRL	0x2020	0x2020	0x2020	0x2020	0x2020
0xB	ADC_CTRL	0x0000	0x0000	0x0000	0x0000	0x0000
0xC	ADC_CLK	0x0B30	0x0B30	0x0B30	0x0B30	0x0B30
0x10	TRX_ENABLE	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x11	TRX_WARMUP	0x0000	0x0000	0x0000	0x0000	0x0000
0x12	ENV_DET	0x7292	0x7292	0x7292	0x7292	0x7292
0x13	SPARE	0x0000	0x0000	0x0000	0x0000	0x0000
0x20	RX_VGA_SET	0x0FFF	0x0FFF	0x0FFF	0x0FFF	0x0FFF
0x21	RX_FE_SET	0xFB44	0xFB44	0xFB44	0xFB44	0x7F44
0x22	TX_VGA_SET	0x3FFF	0x3FFF	0x1FFF	0x1FFF	0x3FFF
0x23	TX_FE_SET	0x0FC4	0x0FC4	0x0FC4	0x0FC4	0x0FC4
0x24	RX_LNA1_BIAS	0xA684	0x1684	0xA684	0x1684	0x0F84
0x25	RX_LNA2_BIAS	0x0134	0x0034	0x0334	0x0234	0x0074
0x26	RX_MIX_BIAS	0x0190	0x0190	0x0190	0x0190	0x0091

Address	Register	Recommended Value				
		Band H8 26.5–29.5 GHz RF/ 3.5-7GHz IF	Band H6 24.25–27.5 GHz RF/ 3.5-7GHz IF	Band L8 26.5–29.5 GHz RF/ 2.5-4GHz IF	Band L6 24.25–27.5 GHz RF/ 2.5-4GHz IF	Band H6h 24.25-27.5 GHz RF/ 3.5-7 GHz IF (High Linearity Mode)
0x27	RX_MIX_DAC	0x0100	0x0100	0x0100	0x0100	0x0100
0x28	RX_LODRV_BIAS	0x2A24	0x2A24	0x2A24	0x2A24	0x2A24
0x29	RX_LOPPF_DAC	0x1100	0x1100	0x1100	0x1100	0x1100
0x2A	RX_PPF	0x0036	0x0036	0x0034	0x0034	0x0036
0x2B	RX_SPARE	0x0000	0x0000	0x0000	0x0000	0x0000
0x2C	RX_VGA	0x03E4	0x03E4	0x04C4	0x04C4	0x03E4
0x30	TX_PA_BIAS	0x61FE	0x6B3C	0x61FE	0x6B3C	0x6B3C
0x31	TX_DRV_BIAS	0x1BB4	0x3FCC	0x1BB4	0x3FCC	0x3FCC
0x32	TX_RFVGA	0x01B2	0x01B2	0x01B2	0x01B2	0x0192
0x33	TX_MIX_BIAS	0x1824	0x9824	0x1824	0x9824	0x9824
0x34	TX_LODRV_BIAS	0x1224	0x1224	0x1224	0x1224	0x0224
0x35	TX_QDAC	0x0130	0x0128	0x0134	0x0130	0x0100
0x36	TX_IDAC	0x006C	0x009C	0x0064	0x0064	0x0100
0x37	TX_SPARE	0x0000	0x0000	0x0000	0x0000	0x0000
0x38	TX_VGA	0xFFFC	0xFFFC	0x8004	0x8004	0xFFFC
0x40	RXLO_CT	0x2136	0x2136	0x2137	0x2137	0x2136
0x41	RXLO_BIAS	0x4924	0x4924	0x4924	0x4924	0x4924
0x42	RXLO_SPARE	0x000C	0x000C	0x001C	0x001C	0x0004
0x43	TXLO_CT	0x213E	0x213D	0x213F	0x213E	0x2134
0x44	TXLO_BIAS	0x4924	0x4924	0x4924	0x4924	0x4924
0x45	TXLO_SPARE	0x001C	0x000C	0x001C	0x001C	0x000C

9. Evaluation Board

9.1 Evaluation Board Image

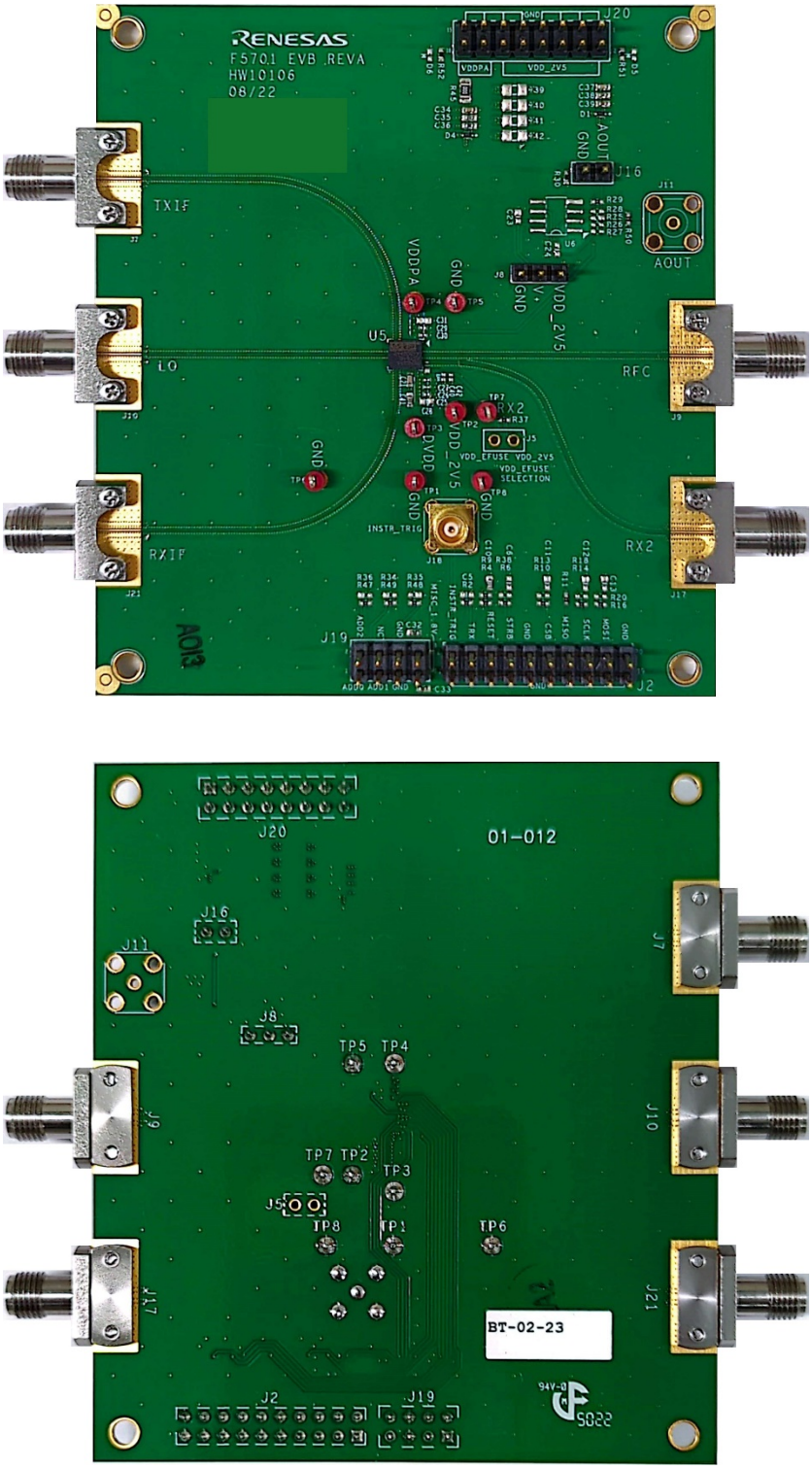

Figure 403. Evaluation Board – Top and Bottom View

9.2 Evaluation Board Applications Circuits

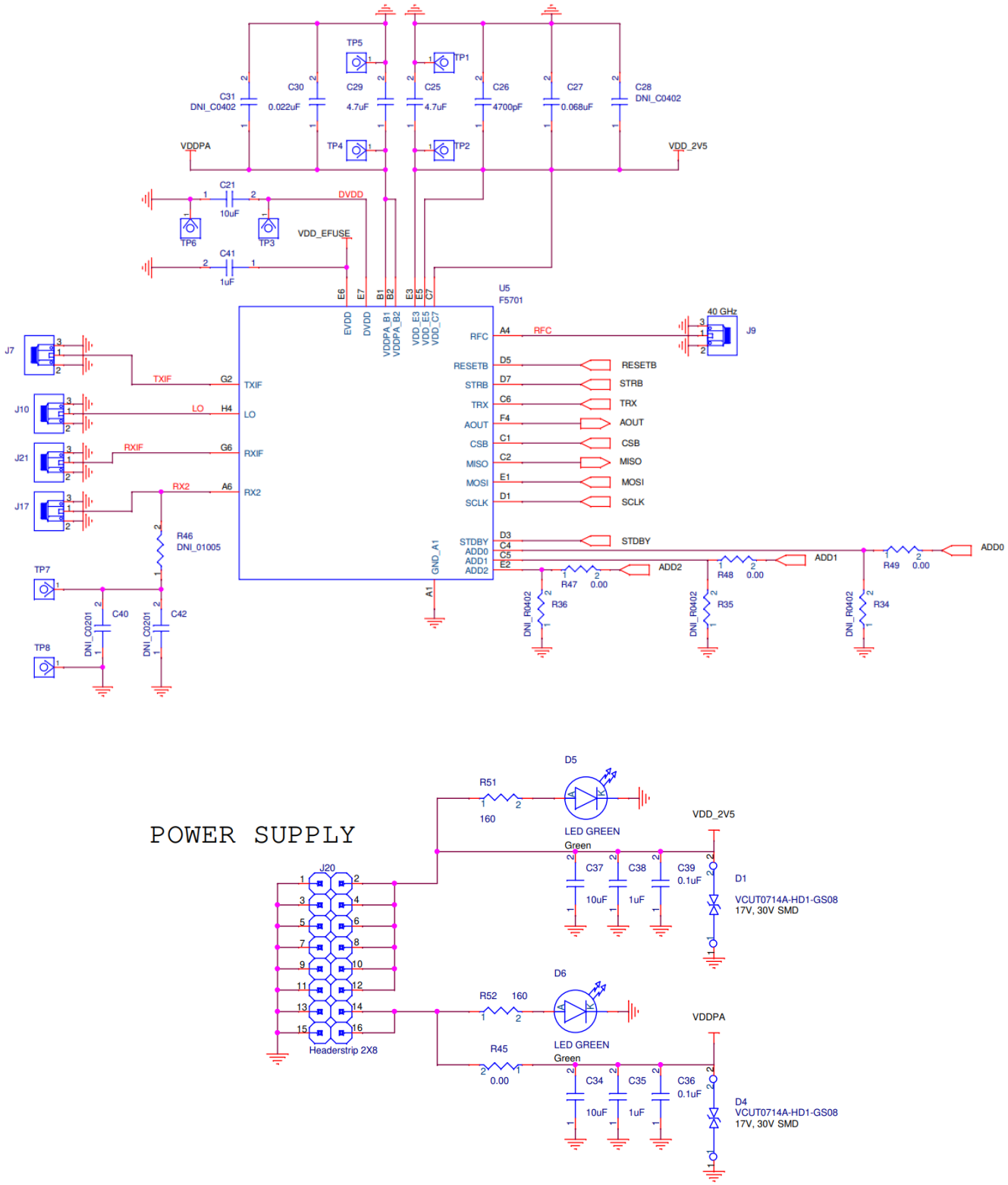

Figure 404. Evaluation Board Schematic (Part 1)

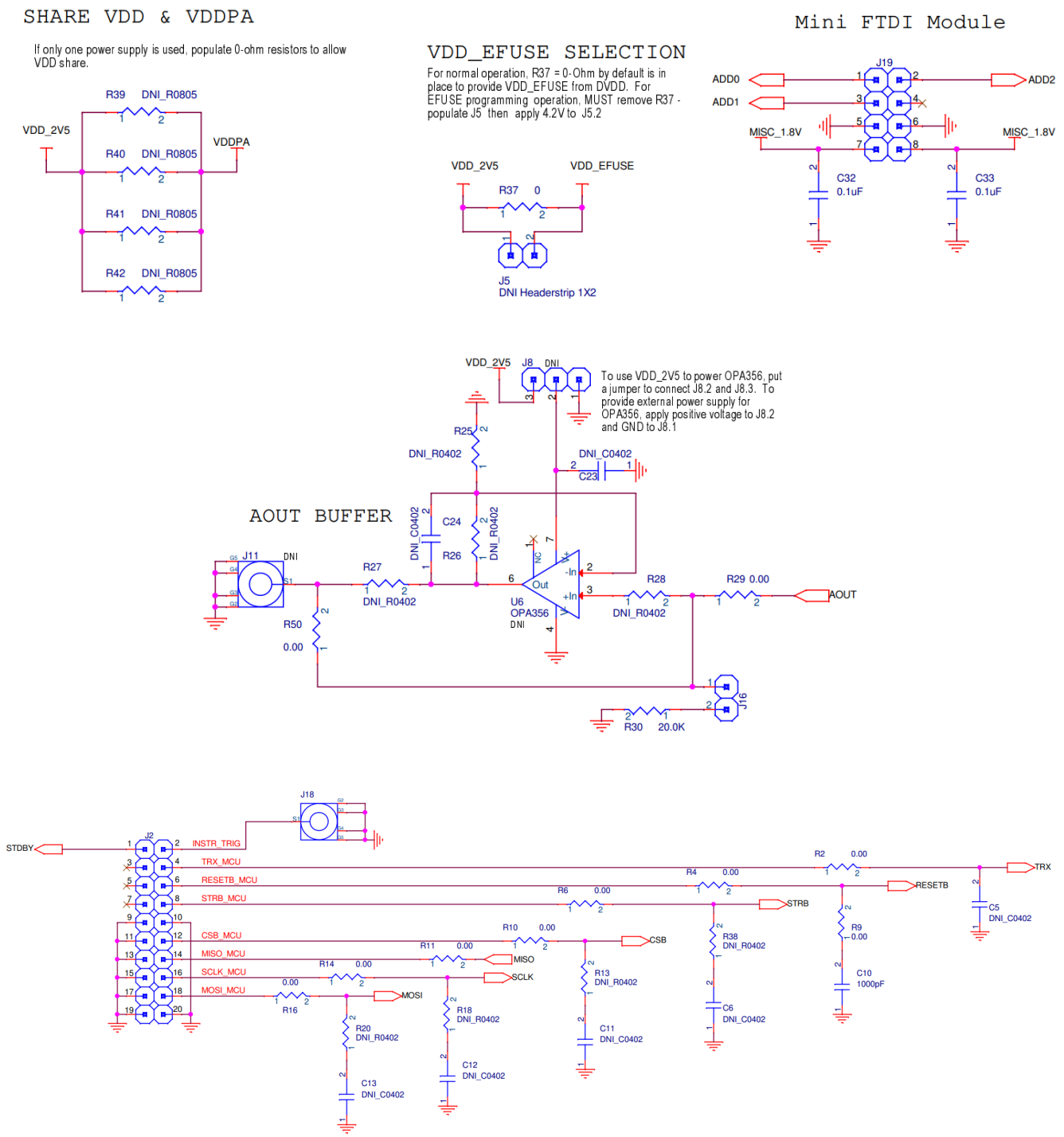

Figure 405. Evaluation Board Schematic (Part 2)

9.3 Bill-of-Materials (BOM)

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C5, C6, C11, C12, C13, C23, C24, C28, C31	9	TBD Surface Mount Capacitor	DNI	-
C10	1	COG Surface Mount Capacitor, 1000pF	GRM1555C1E102J	Murata
C21, C34, C37	3	X5R Surface Mount Capacitor, 10uF	GRM155R60J106M	Murata
C25, C29	2	X5R Surface Mount Capacitor, 4.7uF	GRM035R60J475ME15D	Murata
C26	1	X7R Surface Mount Capacitor, 4700pF	GRM033R71E472K	Murata
C27	1	X5R Surface Mount Capacitor, 0.068uF	GRM033R61C683K	Murata
C30	1	X5R Surface Mount Capacitor, 0.022uF	GRM033R61C223K	Murata
C32, C33, C36, C39	4	X7R Surface Mount Capacitor, 0.1uF	GRM155R71C104KA88D	Murata
C35, C38, C41	3	X5R Surface Mount Capacitor, 1uF	CL05A105KA5NQNC	Samsung
C40, C42	2	TBD Surface Mount Capacitor	DNI	-
D1, D4	2	Surface Mount Diode	VCUT0714A-HD1-GS08	Vishay
D5, D6	2	Green LED, SMD	APHHS1005CGCK	Kingbright
J2	1	Header Dual, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240-inch contact mating length	10-89-7200	Molex
J5	1	Header, 2x10 Vertical	DNI	-
J7, J9, J10, J17, J21	5	2.92mm edge launch, Female Standard Profile	ELF40-002	Signal Microwave
J8	1	Header, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240-inch contact mating length	22-28-4033	Molex
J11	1	SMB Connector Jack, Male Pin 50-Ohm Through Snap Connect	1-1337482-0	TE Connectivity
J16	5	Header, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240-inch contact mating length	22-28-4023	Molex
J18	1	MCX Connector Jack, Female Socket 50-Ohm Through Hole Solder	0733660061	Molex
J19	1	C-Grid Header Dual, Gold, Unshrouded, Breakaway, 100mil pitch	10-89-7080	Molex
J20	1	Header Dual, Gold, Unshrouded, 100mil pitch, 0.062-inch contact mating length	68602-116HLF	Amphenol FCI
R2, R4, R6, R9, R10, R11, R14, R16, R29, R47, R48, R49, R50	13	Surface Mount Resistor	ERJ-2GE0R00	Panasonic
R13, R18, R20, R25, R26, R27, R28, R34, R35, R36, R38	11	Surface Mount Resistor	DNI	-
R30	1	Surface Mount Resistor	RCG040220K0FK	Vishay
R37	1	Surface Mount Resistor	ERJ-2GE0R00	Panasonic

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
R39, R40, R41, R42	4	Surface Mount Resistor	DNI	-
R45	1	Surface Mount Resistor	CRCW08050000Z0EA	Vishay
R46	1	Surface Mount Resistor	DNI	-
R51, R52	2	Surface Mount Resistor	CRCW0402160RFK	Vishay
SO1, SO2, SO3, SO4	4	Hex Standoff Threaded M3 Nylon 0.984" (25.00mm) Natural	25506	Keystone Electronics
TP1, TP2, TP3, TP4, TP5, TP6	4	Phosphor Bronze Wire Loop	5000	Keystone Electronics
U5	1	mmWave Upconverter/Downconverter 24.25GHz – 29.5GHz RF, 2.5GHz – 7GHz IF	F5701	Renesas
U6	1	Voltage Feedback Amplifier 1 Circuit Rail-to-Rail SOIC8	OPA356AID	TI

9.4 Evaluation System Information

For information on how to use the evaluation board and graphical user interface software, see the F5701 Evaluation Kit Manual.

10. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

11. Marking Diagram

- Line 1: indicates the manufacturer
- Line 2: indicates the part number
- Line 3: denotes the following:
  - $ is stepping.
  - Y and WW indicate year and week of manufacture.
  - *** denotes lot seq.
- Line 4: [2D ID] denotes the barcode containing wafer and substrate information.

12. Ordering Information

Part Number	Package Description	MSL Rating	Carrier Type	Temperature Range
RA81F5701GAVG#BC0	4.0 × 4.5 × 0.9 mm, 49-BGA	3	Tray	-40°C to +95°C
RA81F5701GAVG#HC0	4.0 × 4.5 × 0.9 mm, 49-BGA	3	Reel	-40°C to +95°C
RTKA81F5701	F5701 Evaluation Board			

13. Revision History

Revision	Date	Description
1.00	Mar 4, 2025	Initial release.