F6413

8-Channel Dual-Polarized TRx Active Beamforming IC, 12GHz–18GHz

Description

The F6413 is an 8-channel, dual-polarized, transmit/receive active beamforming IC (TRx BFIC) designed for use in X/Ku-band planar phased array antennas. The BFIC has eight antenna ports with independent phase/amplitude control channels and two common ports, allowing for independent combining and distribution of vertical and horizontal signal paths. All inputs and outputs are single-ended and 50Ω matched for ease of integration on to phased array antenna panels.

The F6413 has integrated high resolution voltage DACs designed to provide T/R-synchronized gate bias control signals to external GaAs/GaN front-end modules (FEMs). It also contains an ADC and dedicated voltage sensing pins for voltage sensing from off-chip power detectors.

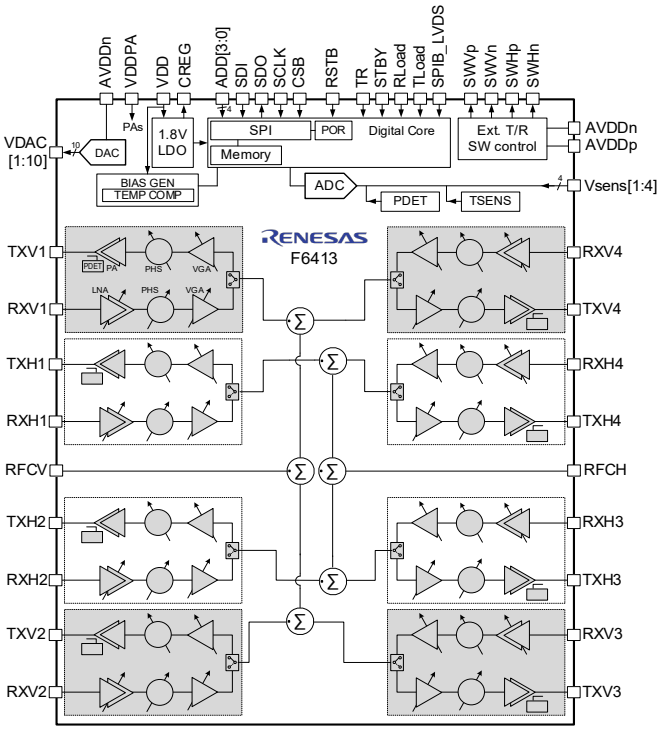


Figure 1. Block Diagram

Features

- Frequency: 12GHz to 18GHz
- Rx reference state, High gain / linearity mode:
  - Single-path gain: 24dB / 5dB
  - NF: 2.3dB / 10.5dB
  - IP1dB: -23dBm / -7dBm
  - Pdc: 125mW/ch / 125mW/ch
- Tx reference state, Nominal / High power mode:
  - Gain: 25dB / 25dB
  - Output P1dB: 15dBm / 20.5dBm
  - Pdc: 250mW/ch / 470mW/ch at P1dB
- Gain and phase control:
  - 360° phase control with 5.6° step
  - 28dB gain control with 0.45dB step
- Supply Voltages:
  - Core (V_{DD}): 2.4V–2.6V
  - PA (V_{DDPA}):
    - 1.1V–1.3V (Nominal)
    - 2.15V–2.35V (High power)
  - Analog (V_{AVDDp} / V_{AVDDn}): 0V–3.6V / -3.6V–0V
  - Internal LDO: 1.8V for digital
- Fast and flexible digital interface:
  - 4-wire SPI up to 50MHz or LVDS up to 100MHz
  - 4-bit address for 16 devices per SPI bus
  - 128 beam-state memory per channel
  - Dedicated pins for T/R and Load control
  - In-pulse beam steering
  - 50ns phase and gain settling time
- Integrated DACs for external FEM gate bias
- On-chip ADC for internal/external voltage sensing
- Compact size for planar integration on λ/2 grid:
  - 8.00 × 8.00 × 0.88 mm, 180-FCCSP (FCBGA)
- Ambient operating temperature: -40°C to +95°C

Applications

- Electronically Steered Phased Array Antennas (ESAs)
- X/Ku-band SATCOM and Point-to-Point terminals
- FMCW and pulse-doppler radar

Contents

Figures

1. Overview

1.1 Functional Block Diagram

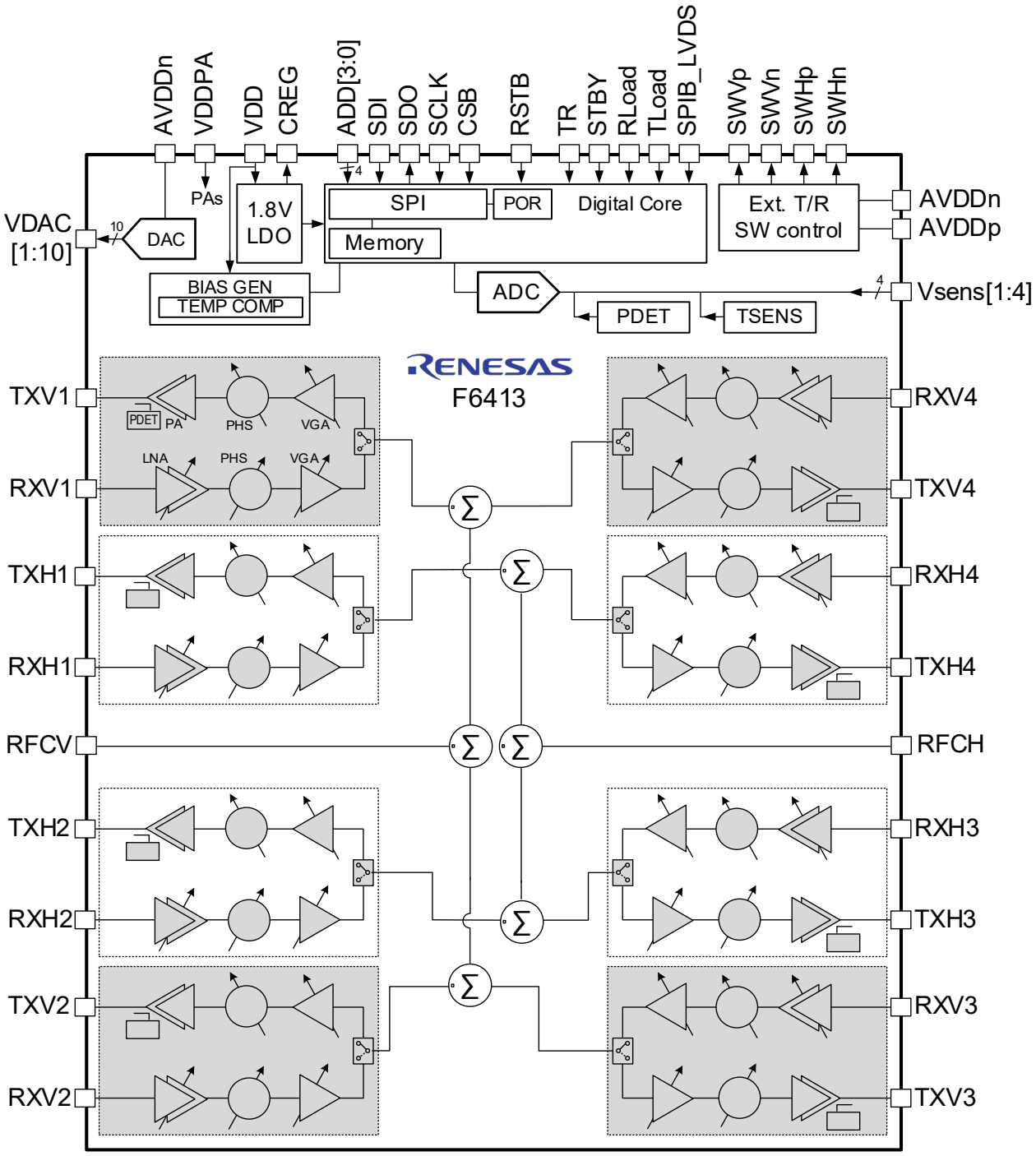


Figure 2. Functional Block Diagram

2. Pin Information

2.1 Pin Assignments

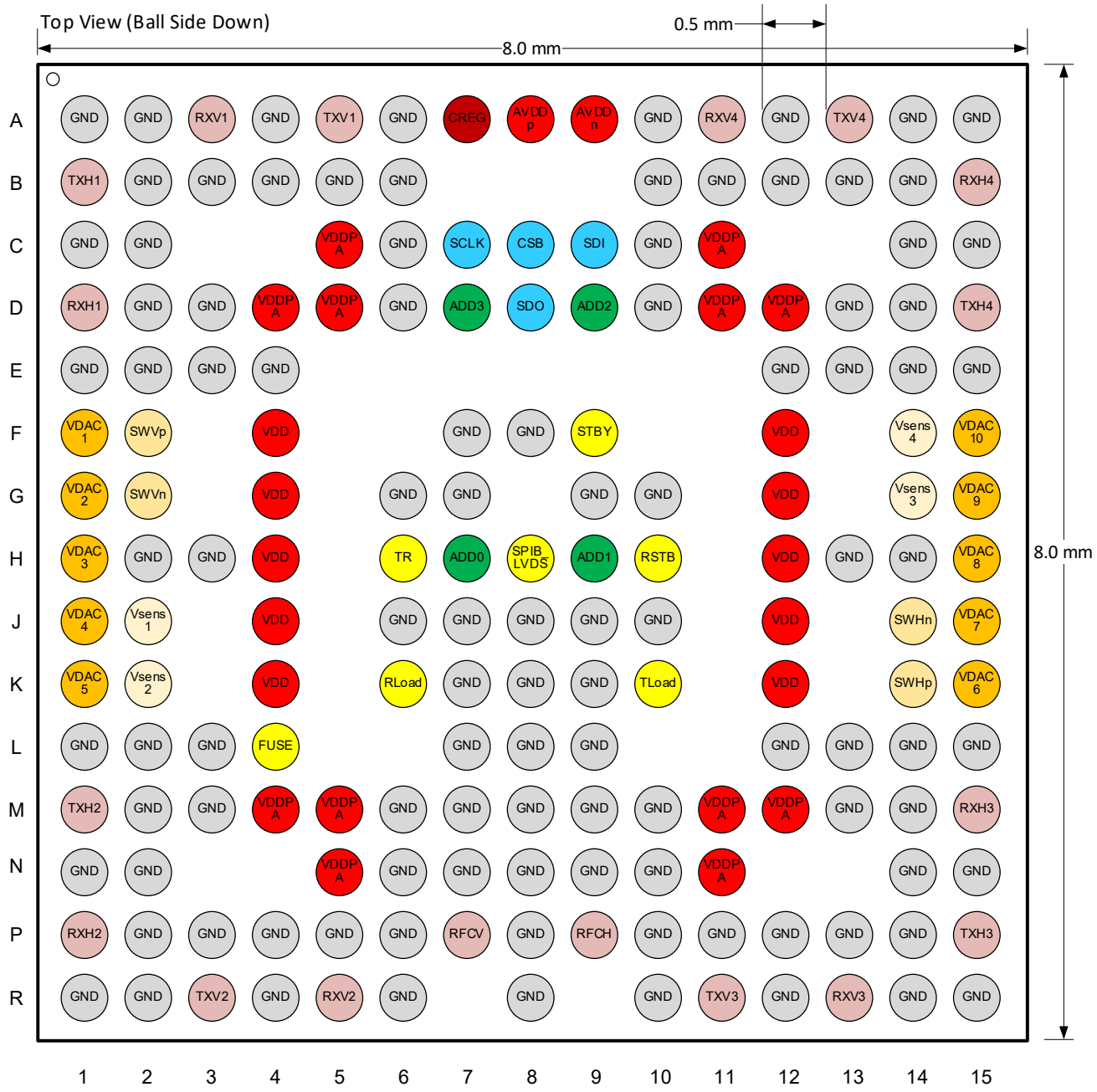


Figure 3. Pin Assignments – Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Type	I/O [1]	Description
A1, A2, A4, A6, A10, A12, A14, A15, B2, B3, B4, B5, B6, B10, B11, B12, B13, B14, C1, C2, C6, C10, C14, C15, D2, D3, D6, D10, D13, D14, E1, E2, E3, E4, E12, E13, E14, E15, F7, F8, G6, G7, G9, G10, H2, H3, H13, H14, J6, J7, J8, J9, J10, K7, K8, K9, L1, L2, L3, L7, L8, L9, L12, L13, L14, L15, M2, M3, M6, M7, M8, M9, M10, M13, M14, N1, N2, N6, N7, N8, N9, N10, N14, N15, P2, P3, P4, P5, P6, P8, P10, P11, P12, P13, P14, R1, R2, R4, R6, R8, R10, R12, R14, R15	GND	Ground	-	Power supply ground, common for RF, DC, and Digital.
F4, G4, H4, J4, K4, F12, G12, H12, J12, K12	VDD	Power	Input	Positive supply voltage for the core and small signal blocks.
C5, C11, D4, D5, D11, D12, M4, M5, M11, M12, N5, N11	VDDPA	Power	Input	Dedicated supply voltage input for the PAs.
A8	AVDDp	Power	Input	Positive analog voltage supply for external switch controls.
A9	AVDDn	Power	Input	Negative analog voltage supply for DACs and external switch controls.
A7	CREG	Power	Output	LDO-regulated digital supply voltage node.[2]
H6	TR	Digital	Input (PD)	Tx/Rx pin. Logic LOW (ground or floating) = Rx. Logic HIGH (1.8V) = Tx.
H10	RSTB	Digital	Input (PU)	All memory registers are reset to factory default. Active LOW.
K6	RLoad	Digital	Input (PD)	Rx toggle pin.
K10	TLoad	Digital	Input (PD)	Tx toggle pin.
F9	STBY	Digital	Input (PD)	Standby pin. Logic LOW (ground or floating) = full operation. Logic HIGH (1.8V) = standby mode.
H8	SPIB_LVDS	Digital	Input (PD)	SPI/LVDS mode select. Logic LOW (ground or floating) = SPI. Logic HIGH (1.8V) = LVDS.
C7	SCLK	Digital	Input (PD)	SPI clock input.
C8	CSB	Digital	Input (PU)	SPI chip-select bar pin. Active LOW.
D8	SDO	Digital	Output	SPI data output pin.
C9	SDI	Digital	Input (PD)	SPI data input pin.
H7	ADD0	Digital	Input (PU)*	Chip address bit 0. ADD0 is the LSB in ADD[3:0] of the SPI command word. Connect to GND for logic 0. Connect to 1.8V or leave floating for logic 1.
H9	ADD1	Digital	Input (PU)	
D9	ADD2	Digital	Input (PU)	

Pin Number	Pin Name	Type	I/O [1]	Description
D7	ADD3	Digital	Input (PU)	Chip address bits. ADD3 is the MSB in ADD[3:0] of the SPI command word. Connect to GND for logic 0. Connect to 1.8V or leave floating for logic 1. In LVDS mode (SPIB_LVDS = 1), ADD3 and ADD2 are the negative differential pair pin for SCLK and SDI, respectively.
L4	FUSE	Analog	Input	Programming pin for OTP memory.
P7	RFCV	Analog	Output	RF common port for vertical polarization channels RXV[1:4] and TXV[1:4].
P9	RFCH	Analog	Output	RF common port for horizontal polarization channels RXH[1:4] and TXH[1:4].
A5	TXV1	Analog	Input	RF antenna port for Tx channel V1.
A3	RXV1	Analog	Input	RF antenna port for Rx channel V1.
B1	TXH1	Analog	Input	RF antenna port for Tx channel H1.
D1	RXH1	Analog	Input	RF antenna port for Rx channel H1.
M1	TXH2	Analog	Input	RF antenna port for Tx channel H2.
P1	RXH2	Analog	Input	RF antenna port for Rx channel H2.
R3	TXV2	Analog	Input	RF antenna port for Tx channel V2.
R5	RXV2	Analog	Input	RF antenna port for Rx channel V2.
R11	TXV3	Analog	Input	RF antenna port for Tx channel V3.
R13	RXV3	Analog	Input	RF antenna port for Rx channel V3.
P15	TXH3	Analog	Input	RF antenna port for Tx channel H3.
M15	RXH3	Analog	Input	RF antenna port for Rx channel H3.
D15	TXH4	Analog	Input	RF antenna port for Tx channel H4.
B15	RXH4	Analog	Input	RF antenna port for Rx channel H4.
A13	TXV4	Analog	Input	RF antenna port for Tx channel V4.
A11	RXV4	Analog	Input	RF antenna port for Rx channel V4.
F1, G1, H1, J1, K1, K15, J15, H15, G15, F15	VDAC[1:10]	Analog	Output	Programmable voltage DAC output pins for gate bias control of external LNAs and PAs.
J2, K2, G14, F14	Vsens[1:4]	Analog	Input	Analog voltage sense pins for external voltage sensing by internal ADC.
F2	SWVp	Digital	Output	Positive and negative voltage control signal pair for external T/R switch for the vertical polarization channels.
G2	SWVn	Digital	Output	
J14	SWHn	Digital	Output	Positive and negative voltage control signal pair for external T/R switch for the horizontal polarization channels.
K14	SWHp	Digital	Output	

1. Internal Pull-up (PU) or pull-down (PD) resistors, when present, are indicated in parentheses. Resistor value is 100kΩ.
2. Requires a low impedance (< 0.1Ω) connection to GND through a 10µF external capacitor.
3. In v100 only, the resistor is PD. Connect to GND or leave floating for logic 0. Connect to 1.8V for logic 1.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Exposure of the device to parameter values outside of the range listed below may reduce the operating lifetime and adversely and permanently alter the device characteristics. Furthermore, functional operation at or near absolute maximum ratings is not implied.

Parameter	Symbol	Conditions	Minimum	Maximum	Unit
Core Supply Voltage	V_{DD}	-	-0.3	3.0	V
PA Supply Voltage	V_{DDPA}	-	-0.3	2.5	V
Positive Supply for Ext Switch Ctrl	V_{AVDDp}	-	0	3.6	V
Negative Supply for VDAC and Ext Switch Ctrl	V_{AVDDn}	-	-3.6	0	V
Digital Pin Voltage	V_{CTL}	-	-0.3	2.1	V
TX Mode RF Common Port Input Power	P_{ABS_TX}	-	-	15	dBm
RX Mode RF Antenna Port Input Power	P_{ABS_RX}	-	-	23	dBm
Junction Temperature	T_J	-	-	150	°C
Lead Temperature (soldering)	T_{LEAD}	Not to exceed 30s at Max temperature per J-STD-020E	-	260	°C
Human Body Model (Tested per JS-001-2012)	V_{HBM}	-	-	2000	V
Charged Device Model (Tested per JESD22-C101)	V_{CDM}	-	-	250	V

3.2 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
RF Frequency Range	f_{RF}	12	-	18	GHz
Core Supply Voltage	V_{DD}	2.4	2.5	2.6	V
PA Supply Voltage, Nominal Bias Mode	V_{DDPA}	1.1	1.2	1.3	V
PA Supply Voltage, High Power Bias Mode [1]	V_{DDPA}	2.15	2.25	2.35	V
Ambient Temperature	T_A	-40	-	95	°C
RF Pin Load Impedance	Z_{RF}	-	50	-	Ω
VDAC Load Resistance	$R_{L\text{-}VDAC}$	350	-	-	Ω
VDAC Load Capacitance	$C_{L\text{-}VDAC}$	-	-	100	pF

1. With additional register programming.

3.3 Thermal Specifications

Parameter	Symbol	Value	Unit
Theta JA, Junction to ambient	θ_{JA}	29	°C/W
Theta JB, Junction to board	θ_{JB}	4	°C/W
Theta JC, Junction to case (exposed silicon backside)	θ_{JC}	2.5	°C/W
Storage Temperature	T_{STOR}	-40 to +150	°C

3.4 Electrical Specifications

3.4.1 Digital Electrical Specifications

Applies to all digital pins in SPI Mode.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Logic Input High Voltage	V_{IH}	-	1.1	-	1.8	V
Logic Input Low Voltage	V_{IL}	-	0	-	0.6	V
Logic Input Current	I_{IH}, I_{IL}	For each input control pin	-50	-	50	µA
Logic Output High Voltage [2]	V_{OH}	I_{OH} = -2mA	1.4	-	-	V
Logic Output Low Voltage [2]	V_{OL}	I_{OL} = 2mA	-	-	0.4	V
SPI Clock Frequency	F_{CLK}	-	-	-	50	MHz

Applies to all digital pins in LVDS Mode.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
LVDS Clock Frequency	F_{CLK}	-	-	-	100	MHz

3.4.2 DC Electrical Specifications

V_{DD} = 2.5V, V_{DDPA} = 1.2V, T_A = 25°C, Z_S = Z_L = 50Ω on all channels. Nominal or high power bias mode register settings applied with channels set to reference state and all channels enabled.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Tx Mode						
Tx V_{DD} and V_{DDPA} Supply Currents at P1dB	$I_{DD\_Tx\_P1dB}$	Nominal Bias Mode V_{DDPA} = 1.2V	-	360	-	mA
	$I_{DDPA\_Tx\_P1dB}$		-	704	-	mA
	$I_{DD\_Tx\_P1dB}$	High Power Bias Mode V_{DDPA} = 2.25V	-	410	-	mA
	$I_{DDPA\_Tx\_P1dB}$		-	1337	-	mA
Tx V_{DD} and V_{DDPA} Supply Currents, Quiescent	$I_{DD\_Tx\_Q}$	Nominal Bias Mode V_{DDPA} = 1.2V	-	345	-	mA
	$I_{DDPA\_Tx\_Q}$		-	376	-	mA
	$I_{DD\_Tx\_Q}$	High Power Bias Mode V_{DDPA} = 2.25V	-	347	-	mA
	$I_{DDPA\_Tx\_Q}$		-	379	-	mA
Rx Mode						
Rx V_{DD} Supply Current	I_{DD_Rx}	High Gain Mode	-	480	-	mA
		High Linearity Mode	-	480	-	mA
Standby Mode						
Standby V_{DD} and V_{DDPA} Supply Currents	I_{DD_Stby}	All channels disabled	-	16	-	mA
	I_{DDPA_Stby}	All channels disabled or Tx channels disabled	-	0.1	-	mA

3.4.3 RF Electrical Specifications – Rx Mode

V_{DD} = 2.5V, T_A = 25°C, f_{RF} = 12GHz–18GHz, Z_S = Z_L = 50Ω on all RF ports and register settings applied identically to all Rx channels.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Reference State, High Gain Mode						
Gain [1]	G_{REF}	-	-	24	-	dB
Noise Figure	NF	-	-	2.3	-	dB
Input 1dB Compression Point	IP1dB	-	-	-23	-	dBm
Input Third Order Intercept Point	IIP3	1MHz Tone Separation	-	-18	-	dBm
Input Return Loss	IRL	-	-	12	-	dB
Output Return Loss	ORL	-	-	12	-	dB
Reference State, High Linearity Mode						
Gain [1]	G_{REF}	-	-	5	-	dB

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Noise Figure	NF	-	-	10.5	-	dB
Input 1dB Compression Point	IP1dB	-	-	-7	-	dBm
Input Third Order Intercept Point	IIP3	1MHz Tone Separation	-	0	-	dBm
Input Return Loss	IRL	-	-	12	-	dB
Output Return Loss	ORL	-	-	12	-	dB
Phase Control						
Phase Adjustment Range	Φ_{RANGE_PS}	-	-	360	-	deg
Phase Adjustment Step	Φ_{STEP_PS}	-	-	5.6	-	deg
RMS Phase Error	$\Phi_{ERR\_RMS\_PS}$	-	-	3	-	deg
RMS Gain Error over Phase Settings	$G_{ERR\_RMS\_PH\_PS}$	-	-	0.5	-	dB
Gain Control, Aligner						
Gain Adjustment Range	G_{RANGE_GA}	-	-	5	-	dB
Gain Adjustment Step	G_{STEP_GA}	-	-	0.7	-	dB
RMS Phase Error over Gain Settings	$\Phi_{ERR\_RMS\_G\_GA}$	-	-	3	-	deg
Gain Control, VGA						
Gain Adjustment Range	G_{RANGE_VGA}	-	-	28.4	-	dB
Gain Adjustment Step	G_{STEP_VGA}	-	-	0.45	-	dB
RMS Gain Error	$G_{ERR\_RMS\_VGA}$	-	-	0.5	-	dB
RMS Phase Error over Gain Settings	$\Phi_{ERR\_RMS\_G\_VGA}$	-	-	5	-	deg
Isolation						
Reverse Isolation	ISO_{OUT_IN}	Any Rx port to common port	-	45	-	dB

1. Gain, in this instance, refers to the Single Path Gain (SPG). Electronic gain will be SPG+ 6dB (4:1 combine). SPG is the measured gain between one of the four input ports and the common port, with the other three Rx ports match terminated. Electronic Gain is the active channel gain inclusive of the 4:1 combiner ohmic loss and is the value typically used in cascaded NF analysis of coherent beam phased array antennas. Reference State gain setting is 2.5dB backed-off from maximum gain on the aligner gain control and at maximum gain setting on the VGA gain control.

3.4.4 RF Electrical Specifications – Tx Mode

V_{DD} = 2.5V, V_{DDPA} = 1.2V, T_A = 25°C, f_{RF} = 12GHz–18GHz, Z_S = Z_L = 50Ω on all RF ports and register settings applied identically to all Tx channels.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Reference State, Nominal Bias Mode						
Gain	G_{REF}	-	-	25	-	dB
Output 1dB Compression Point	OP1dB	-	-	15	-	dBm
Input Return Loss	IRL	-	-	12	-	dB
Output Return Loss	ORL	-	-	12	-	dB
Reference State, High Power Mode (V_{DDPA} = 2.25V with additional bias programming)						
Gain	G_{REF}	-	-	25	-	dB
Output 1dB Compression Point	OP1dB	-	-	20.5	-	dBm
Input Return Loss	IRL	-	-	12	-	dB
Output Return Loss	ORL	-	-	12	-	dB
Phase Control						
Phase Adjustment Range	Φ_{RANGE_PS}	-	-	360	-	deg
Phase Adjustment Step	Φ_{STEP_PS}	-	-	5.6	-	deg
RMS Phase Error	$\Phi_{ERR\_RMS\_PS}$	-	-	3	-	deg
RMS Gain Error Over Phase Settings	$G_{ERR\_RMS\_PH\_PS}$	-	-	0.5	-	dB
Gain Control, Aligner						
Gain Adjustment Range	G_{RANGE_GA}	-	-	5	-	dB
Gain Adjustment Step	G_{STEP_GA}	-	-	0.7	-	dB
RMS Phase Error over Gain Settings	$\Phi_{ERR\_RMS\_G\_GA}$	-	-	3	-	deg
Gain Control, VGA						
Gain Adjustment Range	G_{RANGE_VGA}	-	-	28.4	-	dB
Gain Adjustment Step	G_{STEP_VGA}	-	-	0.45	-	dB
RMS Gain Error	$G_{ERR\_RMS\_VGA}$	-	-	0.5	-	dB
RMS Phase Error over Gain Settings	$\Phi_{ERR\_RMS\_G\_VGA}$	-	-	5	-	deg
Isolation						
Reverse Isolation	ISO_{IN_OUT}	Any Tx port to common port	-	45	-	dB

1. Reference State gain setting is 2.5dB backed-off from maximum gain on the aligner gain control and at maximum gain setting on the VGA gain control.

4. Feature Description

4.1 Power-on Reset (POR)

The POR ensures that all chip registers come up in the default state when power is first applied to the VDD pin. In the default state the chip is in Standby with T/R switch connected to Rx. When power cycling the chip, the POR will trigger when VDD falls below a certain threshold for a minimum amount of time. It is recommended that VDD fall below 1V for at least several milli-seconds before coming back to 2.5V to ensure that the POR is triggered.

4.2 Power Sequence

Figure 4 shows the recommended power sequence for F6413 devices. The AVDDn should be powered up first, followed by VDD. AVDDp and VDDPA can be powered up at any time during this sequence.

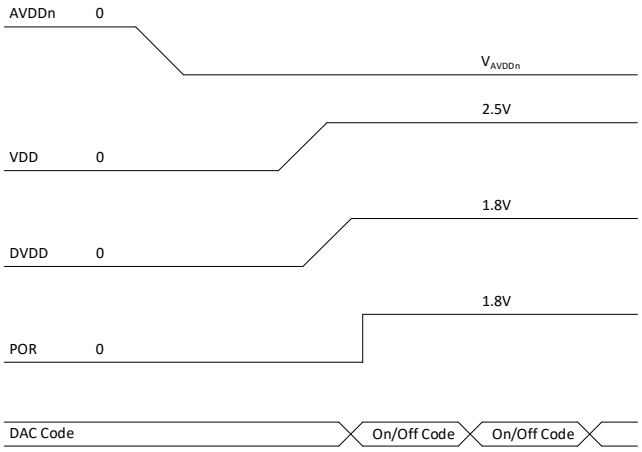


Figure 4. Recommended Power Sequence

4.3 ADC Operation and Sensor Data Access

Operation of voltage sensors and power detectors is done using Service Request Routines (SRQ). The ADC_CFG.ADC_SEL_SOURCE bit (Register 0x10[10]) should be set to 0 for the SRQ mode (default value with the recommended settings). Users can then trigger one or multiple measurements by setting corresponding trigger bits in ADC_SRQ1 register (Register 0x11) to 1 (see Table 1). After triggering, the on-chip ADC will start, and the data will be available in ADC_DATA_CHn registers (Registers 0x3F – 0x5E corresponding to n = 1–32) after the acquisition is completed. Access to the ADC_SRQ1 register is write-only. Data acquisition is completed when the corresponding ADC_DATA_CHn[10] bit (DONE bit) is equal to 1.

Table 1. Trigger Bits and Digital Readout Registers of Sensor Data

Sensor	Trigger Bit	Digital Readout, D
TX1_V Power Detector	ADC_SRQ1[0]=1	ADC_DATA_CH1[9:0]
TX2_V Power Detector	ADC_SRQ1[1]=1	ADC_DATA_CH3[9:0]
TX3_V Power Detector	ADC_SRQ1[2]=1	ADC_DATA_CH5[9:0]
TX4_V Power Detector	ADC_SRQ1[3]=1	ADC_DATA_CH7[9:0]
RFC_V Power Detector	ADC_SRQ1[4]=1	ADC_DATA_CH9[9:0]
TX1_H Power Detector	ADC_SRQ1[5]=1	ADC_DATA_CH11[9:0]
TX2_H Power Detector	ADC_SRQ1[6]=1	ADC_DATA_CH13[9:0]
TX3_H Power Detector	ADC_SRQ1[7]=1	ADC_DATA_CH15[9:0]

Sensor	Trigger Bit	Digital Readout, D
TX4_H Power Detector	ADC_SRQ1[8]=1	ADC_DATA_CH17[9:0]
RFC_H Power Detector	ADC_SRQ1[9]=1	ADC_DATA_CH19[9:0]
Temperature Sensor 1	ADC_SRQ1[10]=1	ADC_DATA_CH21[9:0]
Temperature Sensor 2	ADC_SRQ1[11]=1	ADC_DATA_CH22[9:0]
Internal Reference Current	ADC_SRQ1[12]=1	ADC_DATA_CH23[9:0]
VDD	ADC_SRQ1[12]=1	ADC_DATA_CH24[9:0]
DVDD	ADC_SRQ1[12]=1	ADC_DATA_CH25[9:0]
VDDPA [1]	ADC_SRQ1[12]=1	ADC_DATA_CH26[9:0]
AVDDn	ADC_SRQ1[13]=1	ADC_DATA_CH27[9:0]
Vsens1	ADC_SRQ1[14]=1	ADC_DATA_CH29[9:0]
Vsens2	ADC_SRQ1[14]=1	ADC_DATA_CH30[9:0]
Vsens3	ADC_SRQ1[15]=1	ADC_DATA_CH31[9:0]
Vsens4	ADC_SRQ1[15]=1	ADC_DATA_CH32[9:0]

1. V200 release.

4.3.1 Procedure to Read Voltage Sensors

The following example explains how to read ADC values from voltage sensors:

1. Activate voltage/current sensors to be read by writing 1 to the corresponding bits of Register 0x11. For example, to read ADC values for all four analog voltage sense pins (Vsens[1:4]), write 0xC000 to Register 0x11.
2. Read bits [9:0] of Registers 0x5B (ADC channel 29) for VSENS1, 0x5C (ADC channel 30) for VSENS2, 0x5D (ADC channel 31) for VSENS3, and 0x5E (ADC channel 32) for VSENS4.

4.3.2 Procedure to Read the Temperature Sensor

The following example explains how to read ADC values from the temperature sensor (TSENS1):

1. The master bias needs to be enabled (Register 0x0B[11] = 1).
2. Activate the TSENS1 ADC operation by writing 0x0400 to Register 0x11.
3. Fetch the TSENS1 result (ADC channel 21) by reading bits [9:0] of Register 0x53.

4.3.3 Procedure to Read Tx Power Detectors

The following example explains how to read ADC values from Tx power detectors:

1. Enable Tx common PDET coupler (Register 0x3E[6] = 1) and set PDET power range to high-power mode (Register 0x3E[1:0] = 0) by writing 0x0040 to Register 0x3E.
2. Activate Tx power detectors to be read by writing 1 to the corresponding PDET bits of Register 0x11. For example, to read PDET_TX1_V and PDET_TX2_V (PDET1 and PDET2, respectively), write 0x0003 to Register 0x11.
3. Read bits [9:0] of Registers 0x3F (ADC channel 1) and 0x41 (ADC channel 3) for PDET1 and PDET2 results, respectively.

4.4 Voltage Sensors

Voltage sensors are available for V_{DD}, V_{DDPA}[1] and D_{VDD}. D_{VDD} is the 1.8V digital core voltage that is generated and regulated by the on-chip LDO. The voltage is sensed over a 1:4 divider and is calculated as:

$$V[V] = 4 \cdot \frac{1.38}{2^{10}} \cdot D$$

The estimation formula for V_{AVDDn} is:

$$V[V] = 4 \cdot \frac{1.38}{2^{10}} \cdot D - 3 \cdot V_{DD}$$

In addition, there are four analog voltage sense pins, Vsens[1:4], for sensing of external voltages by the internal ADC. The formula for these is given by:

$$V[V] = \frac{1.38}{2^{10}} \cdot D$$

1. V200 release.

4.5 Current Sensors

Current sensors are available for the three types of reference currents generated inside the chip: PTAT (PT) (IREF_SEL = 01), PTAT2 (PT2) (IREF_SEL = 10) and bandgap (BG) (IREF_SEL = 00). The currents are measured across a 10kΩ resistor and calculated as:

$$I[\mu A] = 100 \cdot \frac{1.38}{2^{10}} \cdot D$$

4.6 Temperature Sensor

There are two temperature sensors on the chip. The theoretical equation used to estimate the temperature from the digital readout is:

$$T[°C] = 0.78 \cdot D + T_0$$

The intercept, T_0, of this linear approximation function is sensitive to process variation, having a typical value of -290 and standard deviation of 20. Therefore, achieving accurate temperature readings requires a single point calibration to remove the error due to process induced intercept variation. To perform a single point calibration, measure the temperature while the chip is in standby mode and at a known ambient temperature (ensuring no heat generating sources nearby that would cause a delta between ambient temperature and chip temperature). Calculate T_0 from the known temperature and the returned code value and store it in the scratch register or off-chip memory. For all future temperature readings, use this intercept value to calculate the temperature.

4.7 Power Detectors

Each transmit channel has a dedicated RF power detector that measures power at the output port and operates over a broad power range. The average RF output power level in dBm may be calculated from the digital readout, D, using the following equation.

$$P_{out}[dBm] = 10 \cdot log_{10}\left(\frac{D}{1024}\right) + 21$$

4.8 Channel Bias Control

Each channel bias control is a value between 0 and 7 (in decimal) set by bits [10:8] of respective OFFSET registers, as summarized in Table 2. Note that the channel bias setting value is an unsigned absolute value and not an offset value as the register name may suggest.

Table 2. Registers for Channel Bias Control

Control	Register	Bits
TxV Channel Bias	0x26 – 0x29 TXVn_OFFSET	10:8 unsigned
TxH Channel Bias	0x2A – 0x2D TXHn_OFFSET	10:8 unsigned
RxV Channel Bias	0x2E – 0x31 RXVn_OFFSET	10:8 unsigned
RxH Channel Bias	0x32 – 0x35 RXHn_OFFSET	10:8 unsigned

4.9 SET and OFFSET Registers

As summarized in Table 3, phase and gain for each channel are controlled by SET and OFFSET registers. The unsigned SET registers are used to perform gain and phase control required for beam steering and shaping. The OFFSET registers may be used to hold the correction factor obtained from calibration, allowing gain and phase alignment across channels.

Table 3. SET and OFFSET Registers for Phase and Gain Aligner

Control	SET Register	SET Bits	OFFSET Register	OFFSET Bits
TxV Phase	0x16 – 0x19 TXVn_SET	15:8 unsigned	0x26 – 0x29 TXVn_OFFSET	7:4 signed
TxH Phase	0x1A – 0x1D TXHn_SET	15:8 unsigned	0x2A – 0x2D TXHn_OFFSET	7:4 signed
RxV Phase	0x1E – 0x21 RXVn_SET	15:8 unsigned	0x2E – 0x31 RXVn_OFFSET	7:4 signed
RxH Phase	0x22 – 0x25 RXHn_SET	15:8 unsigned	0x32 – 0x35 RXHn_OFFSET	7:4 signed
TxV Gain	0x16 – 0x19 TXVn_SET	7:0 unsigned	0x26 – 0x29 TXVn_OFFSET	3:1 unsigned
TxH Gain	0x1A – 0x1D TXHn_SET	7:0 unsigned	0x2A – 0x2D TXHn_OFFSET	3:1 unsigned
RxV Gain	0x1E – 0x21 RXVn_SET	7:0 unsigned	0x2E – 0x31 RXVn_OFFSET	3:1 unsigned
RxH Gain	0x22 – 0x25 RXHn_SET	7:0 unsigned	0x32 – 0x35 RXHn_OFFSET	3:1 unsigned

4.9.1 Phase Control

Tx phase is controlled by TXVn_SET[15:8] and TXHn_SET[15:8] registers for vertical and horizontal channels, respectively. Similarly, Rx phase is controlled by RXVn_SET[15:8] and RXHn_SET[15:8] registers for vertical and horizontal channels, respectively. The phase SET code is a value between 0 and 255 in decimal. The corresponding phase OFFSET registers hold 4-bit signed OFFSET codes (-7 to 7 in decimal) for phase alignment across channels. The combined phase control code is calculated using the following equation.

$$Phase\ Control\ Code = SET + (OFFSET \cdot 4)$$

When the final phase control code falls outside of the range 0 – 255, the value rolls over in a cyclical fashion.

Table 4. Phase Control Operation Example

Phase SET Value	Phase OFFSET Value	Phase Control Code
0 – 255 (dec)	0	0 – 255 (dec)
0 – 255 (dec)	-7	-28 – 227 = [228, …, 255, 0, …, 227] (dec)
0 – 255 (dec)	7	28 – 283 = [28, …, 255, 0, …, 27] (dec)

4.9.2 Gain Control

Tx gain is controlled by TXVn_SET[7:0] and TXHn_SET[7:0] registers for vertical and horizontal channels, respectively. Similarly, Rx gain is controlled by RXVn_SET[7:0] and RXHn_SET[7:0] registers for vertical and horizontal channels, respectively. The gain SET code is a value between 0 and 255 in decimal. The corresponding gain OFFSET registers hold 3-bit unsigned OFFSET codes (0 – 7 in decimal) for gain alignment across channels.

4.10 Programmable Voltage DACs for External Gate Bias Control

The VDAC[1:10] pins provide ten programmable analog voltage outputs for external gate-bias control. Each pin can be individually enabled/disabled and configured to control either LNA or PA and either vertical or horizontal polarization by setting Registers 0x5F (PA_LNA_DAC_CFG1), 0x60 (PA_LNA_DAC_CFG2), and 0x61 (PA_LNA_DAC_CFG3) as summarized in Table 5.

Table 5. Configuration Registers for Programmable Voltage DACs

VDAC Pin	PA/LNA Selection Bit (0 = LNA, 1 = PA)	Polarization Selection Bit (0 = V, 1 = H)	DAC Channel Enable Bit (0 = Disable, 1 = Enable)
VDAC10	PA_LNA_DAC_CFG1[9]	PA_LNA_DAC_CFG2[9]	PA_LNA_DAC_CFG3[9]
VDAC9	PA_LNA_DAC_CFG1[8]	PA_LNA_DAC_CFG2[8]	PA_LNA_DAC_CFG3[8]
VDAC8	PA_LNA_DAC_CFG1[7]	PA_LNA_DAC_CFG2[7]	PA_LNA_DAC_CFG3[7]
VDAC7	PA_LNA_DAC_CFG1[6]	PA_LNA_DAC_CFG2[6]	PA_LNA_DAC_CFG3[6]
VDAC6	PA_LNA_DAC_CFG1[5]	PA_LNA_DAC_CFG2[5]	PA_LNA_DAC_CFG3[5]
VDAC5	PA_LNA_DAC_CFG1[4]	PA_LNA_DAC_CFG2[4]	PA_LNA_DAC_CFG3[4]
VDAC4	PA_LNA_DAC_CFG1[3]	PA_LNA_DAC_CFG2[3]	PA_LNA_DAC_CFG3[3]
VDAC3	PA_LNA_DAC_CFG1[2]	PA_LNA_DAC_CFG2[2]	PA_LNA_DAC_CFG3[2]
VDAC2	PA_LNA_DAC_CFG1[1]	PA_LNA_DAC_CFG2[1]	PA_LNA_DAC_CFG3[1]
VDAC1	PA_LNA_DAC_CFG1[0]	PA_LNA_DAC_CFG2[0]	PA_LNA_DAC_CFG3[0]

The output voltage for each channel can be set by 9-bit DAC data registers based on which PA/LNA mode and ON/OFF state they are in as summarized in Table 6. The output voltage can be calculated from the 9-bit DAC data, *D* (in decimal), using the following equation.

$$V_{DAC}[V] = max\left\{-|AVDDn|, \left(\frac{4.25}{512}\right) \cdot D - 4.25\right\}$$

As illustrated in Figure 5, the relationship between DAC output voltage and DAC data has a fixed slope and the operating range is limited by the negative analog voltage, AVDDn. The output voltage is constant at AVDDn if the DAC data code is lower than D_{min}, which can be approximated from the following equation.

$$D_{min} \approx 512 \left(1 - \frac{|AVDDn|}{4.25}\right)$$

Table 6. Registers for DAC Output Voltage Settings

VDAC Pin	PA/LNA DAC Channel ON	PA DAC Channel OFF or Disabled	LNA DAC Channel OFF or Disabled
VDAC10	DAC_ON10 (0x6C)	DAC_PA_OFF (0x6D)	DAC_LNA_OFF (0x6E)
VDAC9	DAC_ON9 (0x6B)	DAC_PA_OFF (0x6D)	DAC_LNA_OFF (0x6E)
VDAC8	DAC_ON8 (0x6A)	DAC_PA_OFF (0x6D)	DAC_LNA_OFF (0x6E)
VDAC7	DAC_ON7 (0x69)	DAC_PA_OFF (0x6D)	DAC_LNA_OFF (0x6E)
VDAC6	DAC_ON6 (0x68)	DAC_PA_OFF (0x6D)	DAC_LNA_OFF (0x6E)
VDAC5	DAC_ON5 (0x67)	DAC_PA_OFF (0x6D)	DAC_LNA_OFF (0x6E)
VDAC4	DAC_ON4 (0x66)	DAC_PA_OFF (0x6D)	DAC_LNA_OFF (0x6E)
VDAC3	DAC_ON3 (0x65)	DAC_PA_OFF (0x6D)	DAC_LNA_OFF (0x6E)
VDAC2	DAC_ON2 (0x64)	DAC_PA_OFF (0x6D)	DAC_LNA_OFF (0x6E)
VDAC1	DAC_ON1 (0x63)	DAC_PA_OFF (0x6D)	DAC_LNA_OFF (0x6E)

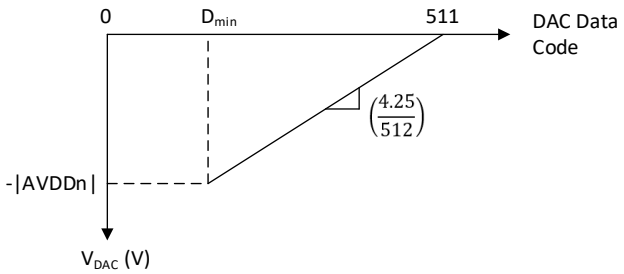


Figure 5. DAC Output Voltage vs 9-bit DAC Data

4.11 Tx/Rx Operation and Manual Channel Control

The main Tx/Rx switching operation can be controlled either by the SPI (SW_TRX.TRX register bit) or the external TR pin. The TRX control mode setting (CTRL_CFG.TRX_CONT_MODE: 0 = SPI and 1 = TR pin) selects which mode to operate in. All internal Tx/Rx beamformer switches will be synchronized to the main Tx/Rx operation if the CTRL_CFG.SYNC_TRX register bit is set to 1. If the CTRL_CFG.SYNC_TRX register bit is set to 0, the internal Tx/Rx beamformer switches for each polarization can be separately set to Tx or Rx by setting SW_TRX.TRX_BFV and SW_TRX.TRX_BFH register bits, regardless of the main Tx/Rx operation, as summarized in Figure 6.

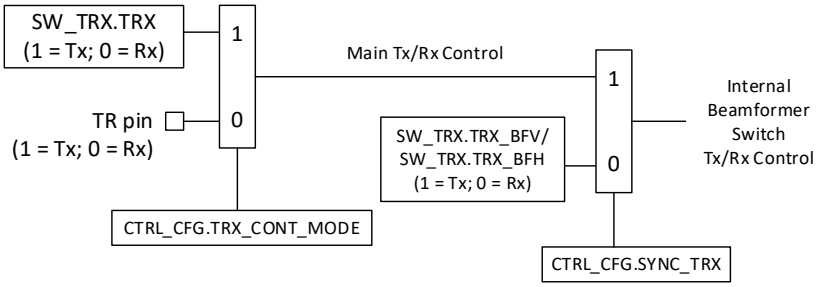


Figure 6. Internal Beamformer Switch Tx/Rx Control Diagram

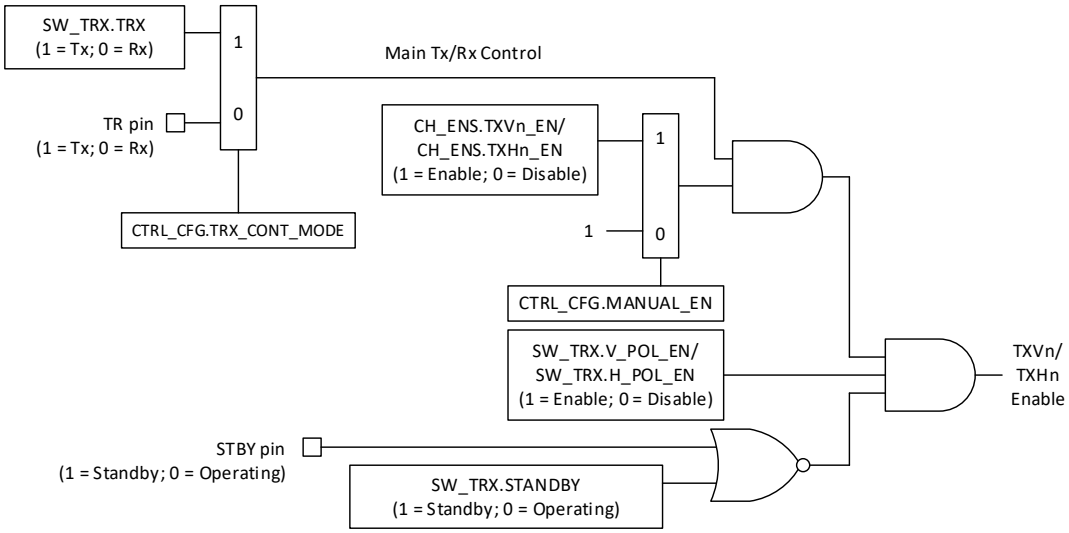


Figure 7. Tx Channel Control Diagram

Tx/Rx beamformer channels are also enabled and disabled by the main Tx/Rx control. All Rx channels will be disabled in Tx mode, and vice versa for Tx channels in Rx mode. The corresponding CH_ENS register bits further control the individual channels that can be enabled (Tx channels in Tx mode and Rx channels in Rx mode) if the CTRL_CFG.MANUAL_EN register is set to 1. Figure 7 and Figure 8 respectively show simplified control diagrams for TX and RX channels.

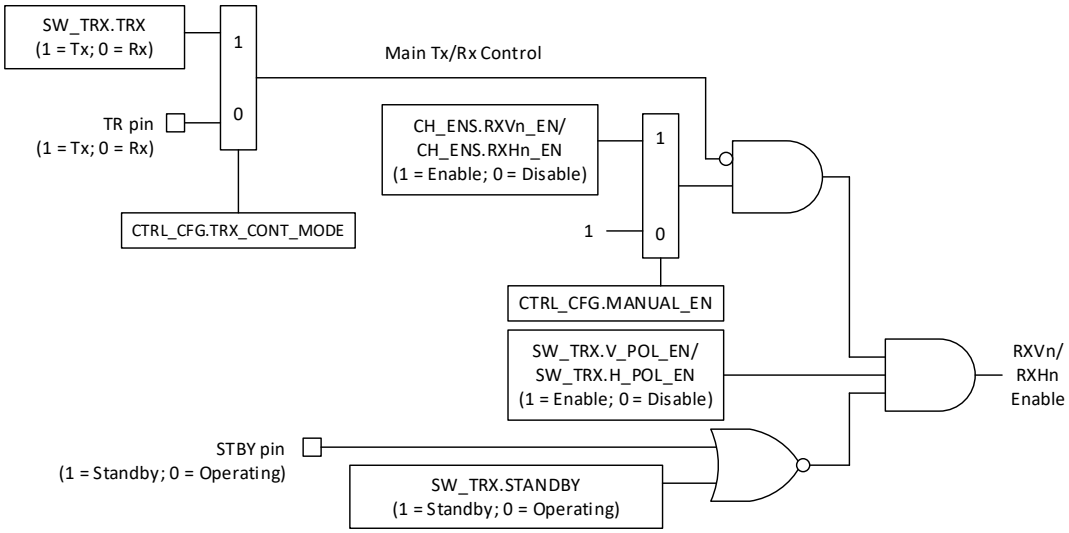


Figure 8. Rx Channel Control Diagram

4.12 External Switch Control

The SWVp/SWVn and SWHp/SWHn pins provide voltage signals to control external Tx/Rx switches for vertical polarization and horizontal polarization, respectively. The operation will be synchronized to the main Tx/Rx operation if the CTRL_CFG.SYNC_TRX register bit is set to 1. If the CTRL_CFG.SYNC_TRX register bit is 0, the Tx/Rx control for each polarization will be separately set through SW_TRX.TRX_EXTV and SW_TRX.TRX_EXTH register bits, regardless of the mail Tx/Rx operation, as shown Figure 9. The pins can be configured to provide AVDDp, AVDDn, ground, or floating (high impedance) as summarized in Table 7.

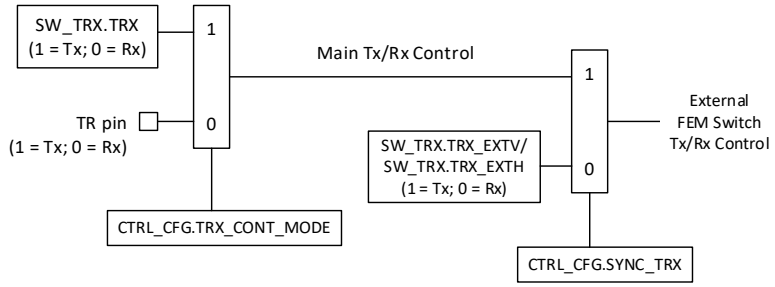


Figure 9. External Switch Tx/Rx Control Diagram

Table 7. External Switch Control Settings

Tx/Rx Control	SW_DRV_EN_TR	SW_DRV_TR_STATE	SW_FEM_TR_MODE	SWVp/SWHp	SWVn/SWHn
X	0	X	X	Floating	Floating
0	1	0	0	AVDDp	Floating
0	1	0	1	Floating	AVDDn
0	1	1	0	0	Floating
0	1	1	1	Floating	0
1	1	0	0	0	Floating
1	1	0	1	Floating	0
1	1	1	0	AVDDp	Floating
1	1	1	1	Floating	AVDDn

4.13 External Pin Configuration and Operation

By setting the TRX control mode register bit (CTRL_CFG.TRX_CONT_MODE) to 0, the external TR pin will be used for Tx/Rx operation. In addition, the PIN_CFG register will become active, enabling the use of TR, TLoad, and RLoad pins for updating Tx/Rx set registers and PA/LNA DAC states. Either rising edges or logical changes of these three external pins will trigger changes according to the external pin configuration set by the PIN_CFG. EXT_PIN_MODE register bits. Note that only configurations 1–12 are valid for operation.

Table 8. PA/LNA DAC States Based on External Pin Mode and Pin Logical Values

PIN_CFG.EXT_PIN_MODE	(TR, TLoad, RLoad) Logical Values							
	000	001	010	011	100	101	110	111
1–3	PA = OFF LNA = OFF	PA = OFF **LNA = ON**	PA = OFF LNA = OFF	PA = OFF **LNA = ON**	PA = OFF LNA = OFF	PA = OFF LNA = OFF	**PA = ON** LNA = OFF	**PA = ON** LNA = OFF
4–6	PA = OFF; LNA = OFF			N/A	PA = OFF; LNA = OFF			N/A
7–9	PA = OFF; **LNA = ON**			N/A	**PA = ON**; LNA = OFF			N/A
10–12	PA = OFF **LNA = ON**	PA = OFF **LNA = ON**	PA = OFF **LNA = ON**	PA = OFF **LNA = ON**	**PA = ON** LNA = OFF	**PA = ON** LNA = OFF	**PA = ON** LNA = OFF	**PA = ON** LNA = OFF

4.13.1 PA/LNA DAC State Control

Table 8 summarizes PA/LNA DAC states for different logical values of the three external pins. PA DACs can only be ON in the Tx mode (TR = 1) and LNA DACs can only be ON in the Rx mode (TR = 0). When changing the TR pin's logical value to switch between Tx and Rx modes, both TLoad and RLoad pins need to be 0 by design to avoid triggering any unintended action.

4.13.2 Edge-Triggered Operation

While the device is in either Tx or Rx mode, rising edges of the TLoad and RLoad pins can also result in modifications of active Tx/Rx set registers (for phase/gain control) and respective buffers by triggering three types of LUT-based actions: Latch TX/RX+1, TX/RX+1, and Latch TX/RX Buffer. The operation flowcharts for external pin configurations 1–3 and 10–12, and configurations 4–9 are illustrated in Figure 10 and Figure 11, respectively.

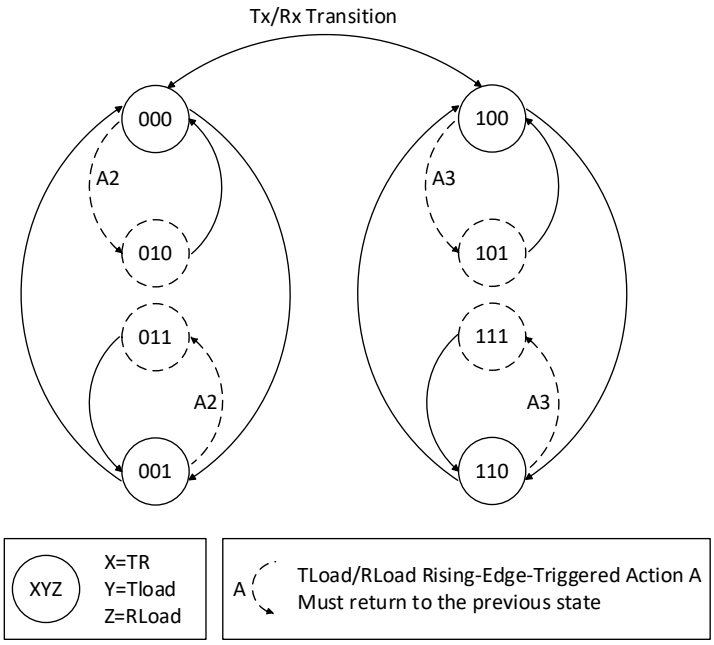


Figure 10. Edge-Triggered Operation Flowchart for External Pin Configuration 1–3 and 10–12

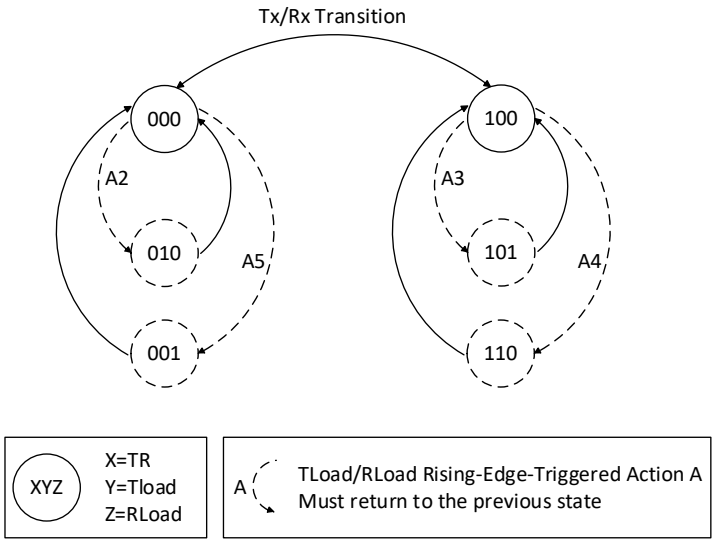


Figure 11. Edge-Triggered Operation Flowchart for External Pin Configuration 4–9

Table 9. Summary of Rising-Edge-Triggered Actions for Each External Pin Configuration

PIN_CFG. EXT_PIN_MODE	Rising-Edge-Triggered Actions			
	A2	A3	A4	A5
1	Latch RX+1	Latch TX+1	N/A	N/A
2	Latch RX+1, TX+1	Latch TX+1, RX+1	N/A	N/A
3	Latch RX buffer	Latch TX buffer	N/A	N/A
4	Latch TX+1	Latch RX+1	Latch TX+1	Latch RX+1
5	Latch TX+1, RX+1	Latch RX+1, TX+1	Latch TX+1, RX+1	Latch RX+1, TX+1
6	Latch TX buffer	Latch RX buffer	Latch TX buffer	Latch RX buffer
7	Latch TX+1	Latch RX+1	Latch TX+1	Latch RX+1
8	Latch TX+1, RX+1	Latch RX+1, TX+1	Latch TX+1, RX+1	Latch RX+1, TX+1
9	Latch TX buffer	Latch RX buffer	Latch TX buffer	Latch RX buffer
10	Latch RX+1	Latch TX+1	N/A	N/A
11	Latch RX+1, TX+1	Latch TX+1, RX+1	N/A	N/A
12	Latch RX buffer	Latch TX buffer	N/A	N/A

Each dashed arrow line in Figure 10 and Figure 11 represent a state transition due to a rising edge of TLoad or RLoad pins that will trigger a set of LUT-based actions. Refer to Table 9 for specific detail of action sets (A2–A5) for each external pin configuration.

Note: States represented by dashed circles are only transition states. Once a rising-edge trigger happens, a falling edge will need to follow to return to the previous operating state (a solid circle) so the operation can continue.

4.13.2.1 Edge-Triggered Action: Latch TX/RX+1

Figure 12 illustrates the edged-triggered Latch TX/RX+1 action. The active LUT index is increased by 1 and the phase/gain set data stored at the new pointer is copied to the associated buffer and active registers. Depending on the operation mode and enabled polarization, the corresponding HLUT_INFO/VLUT_INFO register is automatically incremented by 1 to reflect the new active LUT index. When the associated HLUT_STOP/VLUT_STOP register value is reached, HLUT_INFO/VLUT_INFO register will be set back to the corresponding HLUT_START/VLUT_START.

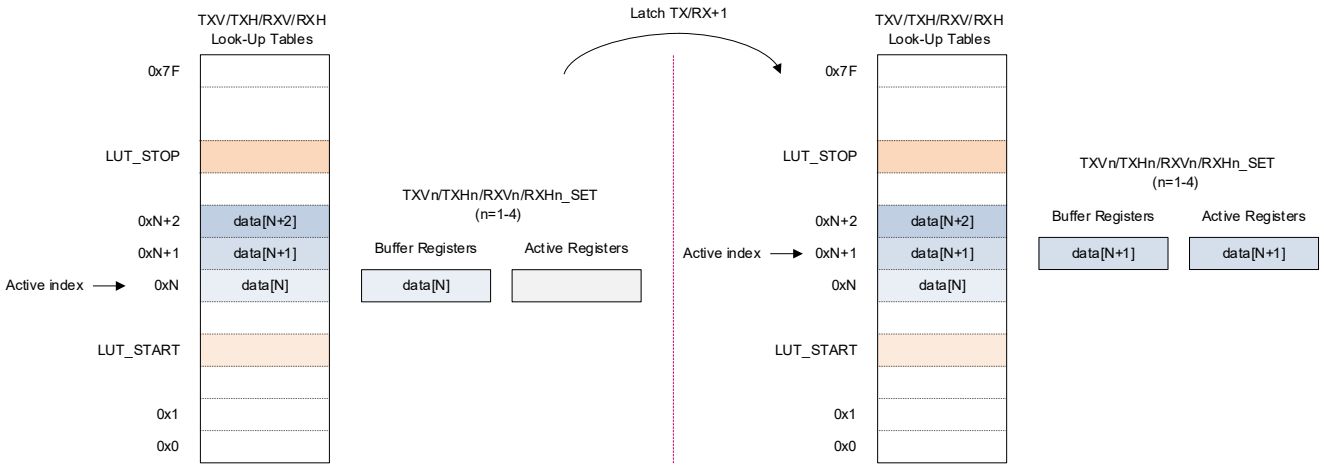


Figure 12. Edge-Triggered Action: Latch TX/RX+1

4.13.2.2 Edge-Triggered Action: TX/RX+1

Figure 13 illustrates the edged-triggered TX/RX+1 action. The operation is similar to the Latch TX/RX+1 action described in section 4.13.2.1 but only the associated buffer registers will be updated with the data store at the new LUT pointer. The active registers will not be latched.

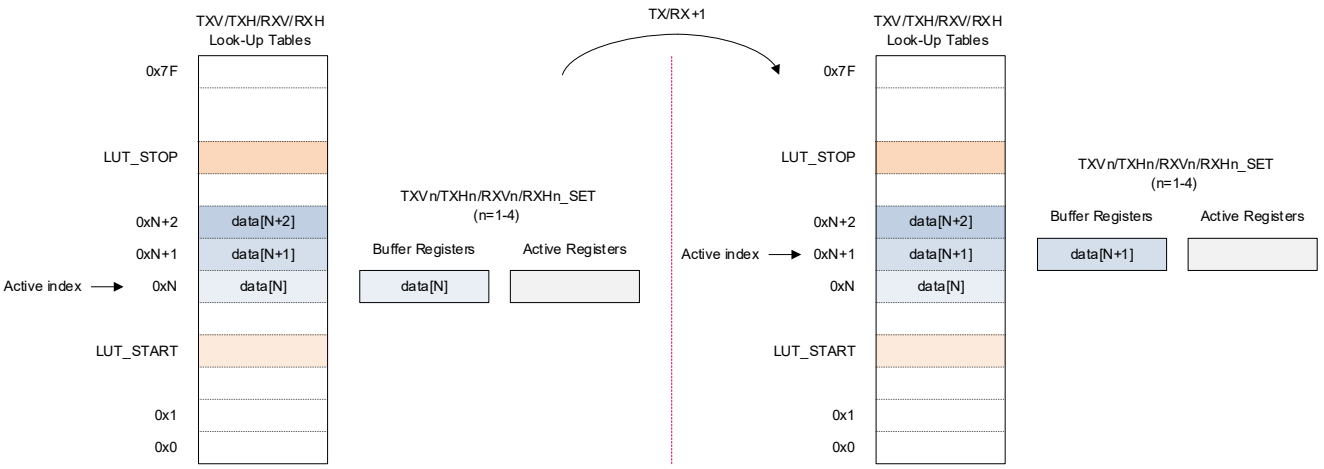


Figure 13. Edge-Triggered Action: TX/RX+1

4.13.2.3 Edge-Triggered Action: Latch TX/RX Buffer

Figure 14 illustrates the edged-triggered Latch TX/RX Buffer action. The active LUT index and buffer registers will stay unchanged. The active registers are latched with data from the associated buffer registers.

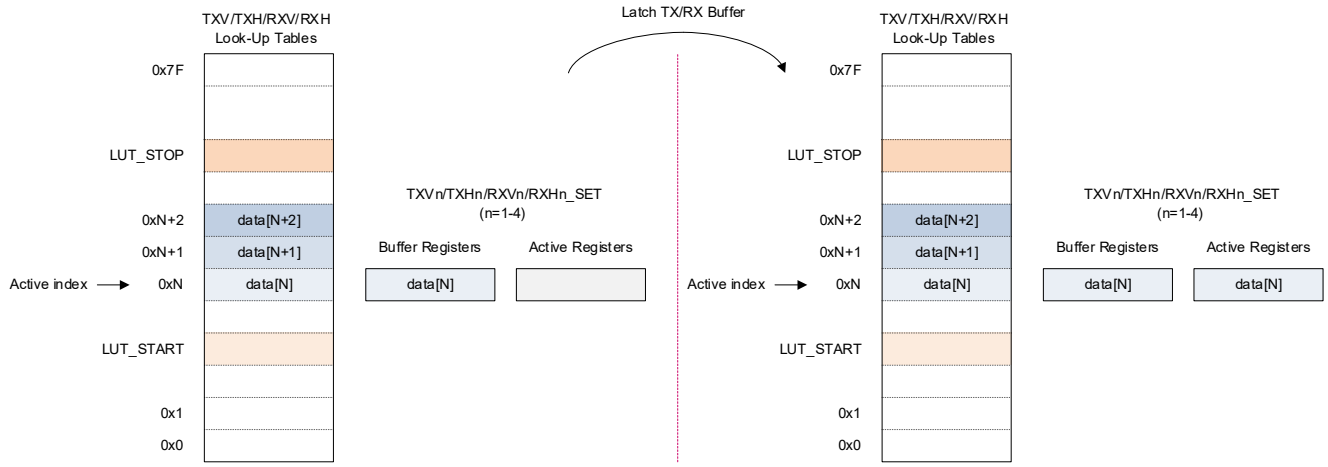


Figure 14. Edge-Triggered Action: Latch TX/RX Buffer

5. Programming

The F6413 uses a standard Serial Peripheral Interface (SPI) protocol for synchronous serial communication. The SPI bus consists of four wire signals: Serial Clock (SCLK), Serial Data In (SDI), Serial Data Out (SDO), and Chip Select Bit (CSB). The SPI clock operates up to 50MHz and the SCLK pin is associated with the clock signal rising edge. The input data stream (addresses, commands, messages, and data) is received on the SDI pin, while the output data stream is transmitted from the SDO pin. The SDO pin shows a high-Z impedance level when the device is in listen mode. The CSB pin acts as a chip-select pin. All SPI bus pins are synchronous and compatible with multi-chip connection.

There are eight general SPI modes defined by the three mode control bits of all SPI commands as summarized in Table 10. Data is loaded with MSB first and transferred to the input register on the rising edges of SCLK.

Table 10. SPI Modes

Mode Control Bits	Mode of Operation	Description
000	LCL_REG_RD	Local Register Read
001	LCL_REG_WR	Local Register Write
010	GBL_REG_WR	Global Register Write
011	LCL_LUT_RD	Local LUT Read
100	LCL_LUT_WR	Local LUT Write
101	GBL_LUT_WR	Global LUT Write
110	LCL_FBS	Local Fast Beam Steering
111	GBL_FBS	Global Fast Beam Steering

5.1 Register Read/Write

LCL_REG_RD, LCL_REG_WR, and GBL_REG_WR modes provide access to the available registers for configuring and controlling the chip. Continuous write to consecutive registers is supported for both LCL_REG_WR and GBL_REG_WR modes by appending additional data sets at the end. Similarly, continuous read is supported and data from the consecutive register is read until the CSB is set to high again.

5.1.1 LCL_REG_RD

With the command bit sequence shown in Figure 15, 16-bit data can be read from any register of a device specified by the chip address and register address bits. For continuous read, once the last register address has been read, the address pointer rolls back to read the first address and the sequence continues.

Byte1								Byte2								Byte3	Byte4
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7:0	7:0
Mode			Chip Address					Register Address								Read Data	
0	0	0	ADD4	ADD3	ADD2	ADD1	ADD0	A7	A6	A5	A4	A3	A2	A1	A0	D[15:8]	D[7:0]

Figure 15. LCL_REG_RD Command Bit Sequence

Table 11. LCL_REG_RD Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Register Read, mode = 000.
1	4:0	Chip Address	Select device address to be accessed by SPI command.
2	7:0	Register Address	8-bit address of internal register to be accessed. Continuous read and address roll back is supported.
3	7:0	Data byte 1 – D[15:8]	16-bit read data received on the SDO line. Data from the consecutive register is read every 16 clock cycles at the end until the CSB is set to high again.
5	7:0	Data byte 2 – D[7:0]	

5.1.2 LCL_REG_WR

With the command bit sequence shown in Figure 16, 16-Bit data can be written to any writable register of a device specified by the chip address and register address bits. For continuous write, once the last register address has been written, the address pointer rolls back to write the first address and the sequence continues. Please note that “PH Set” and “GA Set” bits are only relevant to channel phase/gain set registers (registers 0x16 – 0x25) and both bits should be set to 1 so that the command sequence is valid for 16-bit data write to any register.

Byte1								Byte2								Byte3								Byte4	Byte5
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7:0	7:0
Mode			Chip Address					Register Address								RF Load		DAC Load		PH Set	GA Set	Error Correction Bits		Write Data	
0	0	1	ADD4	ADD3	ADD2	ADD1	ADD0	A7	A6	A5	A4	A3	A2	A1	A0	TRL	RRL	TAL	RAL	1	1	NB1	NB0	D[15:8]	D[7:0]

Figure 16. LCL_REG_WR Command Bit Sequence for 16-Bit Data Write

Table 12. LCL_REG_WR Command Bit Definition for 16-Bit Data Write

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Register Write, mode = 001.
1	4:0	Chip Address	Select device address to be accessed by SPI command.
2	7:0	Register Address	8-bit address of internal register to be accessed. Continuous write and address roll back is supported.
3	7	TRL	Set to 1 to latch buffer data to Tx channels.
3	6	RRL	Set to 1 to latch buffer data to Rx channels.
3	5	TAL	Set to 1 to latch buffer data to Tx DACs.
3	4	RAL	Set to 1 to latch buffer data to Rx DACs.
3	3	PH Set (PSS)	Set both bits to 1 for 16-bit data write to any register.
3	2	GA Set (GAS)	
3	1	NB1	Correction bits for error detection.
3	0	NB0	
4	7:0	Data byte 1 – D[15:8]	16-bit write data sent on the SDI line. Additional 16-bit data streams would be written to consecutive registers.
5	7:0	Data byte 2 – D[7:0]	

Only for channel phase/gain set registers (registers 0x16 – 0x25), an 8-bit phase-only or gain-only data write is supported by setting “PH Set” and “GA Set” bits to either ‘10’ or ’01’, respectively. Continuous write is supported by streaming additional 8-bit data, which will be written to either phase or gain portions of subsequent-channel set registers, depending on “PH Set” and “GA Set” bits. See Figure 17 for the command bit sequence.

Byte1								Byte2								Byte3								Byte4
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7:0
Mode			Chip Address					Register Address								RF Load		DAC Load		PH Set	GA Set	Error Correction Bits		Write Data
0	0	1	ADD4	ADD3	ADD2	ADD1	ADD0	A7	A6	A5	A4	A3	A2	A1	A0	TRL	RRL	TAL	RAL	PSS	GAS	NB1	NB0	D[7:0]

Figure 17. LCL_REG_WR Command Bit Sequence for 8-Bit Phase/Gain Data Write

Table 13. LCL_REG_WR Command Bit Definition for 8-Bit Phase/Gain Data Write

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Register Write, mode = 001.
1	4:0	Chip Address	Select device address to be accessed by SPI command.
2	7:0	Register Address	8-bit address of internal register to be accessed. Continuous write and address roll back is supported.
3	7	TRL	Set to 1 to latch buffer data to Tx channels.
3	6	RRL	Set to 1 to latch buffer data to Rx channels.
3	5	TAL	Set to 1 to latch buffer data to Tx DACs.
3	4	RAL	Set to 1 to latch buffer data to Rx DACs.
3	3	PH Set (PSS)	Set to ‘10’ or ‘01’ for 8-bit phase-only or gain-only data write.
3	2	GA Set (GAS)	

Byte	Bit	Description	Comment
3	1	NB1	Correction bits for error detection.
3	0	NB0	
4	7:0	Data byte – D[7:0]	8-bit phase or gain set data sent on the SDI line. Additional 8-bit data streams would be written to phase or gain set registers of subsequent channels.

5.1.3 GBL_REG_WR

With the command bit sequence shown in Figure 18, 16-Bit data can be written globally to any writable register of all devices on the SPI bus, or the specified sub-array if the sub-array enable bit is set. For continuous write, once the last register address has been written, the address pointer rolls back to write the first address and the sequence continues. Please note that “PH Set” and “GA Set” bits are only relevant to channel phase/gain set registers (registers 0x16 – 0x25) and both bits should be set to 1 so that the command sequence is valid for 16-bit data write to any register.

Byte1								Byte2								Byte3								Byte4	Byte5
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7:0	7:0
Mode			SA Enable	Sub-Array Index				Register Address								RF Load		DAC Load		PH Set	GA Set	Error Correction Bits		Write Data	
0	1	0	SE	SA3	SA2	SA1	SA0	A7	A6	A5	A4	A3	A2	A1	A0	TRL	RRL	TAL	RAL	1	1	NB1	NB0	D[15:8]	D[7:0]

Figure 18. GBL_REG_WR Command Bit Sequence for 16-Bit Data Write

Table 14. GBL_REG_WR Command Bit Definition for 16-Bit Data Write

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Register Write, mode = 010.
1	4	SA Enable	Set to 1 to enable sub-array feature.
1	3:0	Sub-Array Index	Select sub-array to be accessed by SPI command. Sub-array index information for each chip is stored in the CHIP_INFO register.
2	7:0	Register Address	8-bit address of internal register to be accessed. Continuous write and address roll back is supported.
3	7	TRL	Set to 1 to latch buffer data to Tx channels.
3	6	RRL	Set to 1 to latch buffer data to Rx channels.
3	5	TAL	Set to 1 to latch buffer data to Tx DACs.
3	4	RAL	Set to 1 to latch buffer data to Rx DACs.
3	3	PH Set (PSS)	Set both bits to 1 for 16-bit data write to any register.
3	2	GA Set (GAS)	
3	1	NB1	Correction bits for error detection.
3	0	NB0	
4	7:0	Data byte 1 – D[15:8]	16-bit write data sent on the SDI line. Additional 16-bit data streams would be written to consecutive registers.
5	7:0	Data byte 2 – D[7:0]	

Only for channel phase/gain set registers (registers 0x16 – 0x25), an 8-bit phase-only or gain-only data write is supported by setting “PH Set” and “GA Set” bits to either 10 or 01, respectively. Continuous write is supported by streaming additional 8-bit data, which will be written to either phase or gain portions of subsequent-channel set registers, depending on “PH Set” and “GA Set” bits. See Figure 19 for the command bit sequence.

Byte1								Byte2								Byte3								Byte4
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7:0
Mode			SA Enable	Sub-Array Index				Register Address								RF Load		DAC Load		PH Set	GA Set	Error Correction Bits		Write Data
0	1	0	SE	SA3	SA2	SA1	SA0	A7	A6	A5	A4	A3	A2	A1	A0	TRL	RRL	TAL	RAL	PSS	GAS	NB1	NB0	D[7:0]

Figure 19. GBL_REG_WR Command Bit Sequence for 8-Bit Phase/Gain Data Write

Table 15. GBL_REG_WR Command Bit Definition for 8-Bit Phase/Gain Data Write

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Register Write, mode = 010.
1	4	SA Enable	Set to 1 to enable sub-array feature.
1	3:0	Sub-Array Index	Select sub-array to be accessed by SPI command. Sub-array index information for each chip is stored in the CHIP_INFO register.
2	7:0	Register Address	8-bit address of internal register to be accessed. Continuous write and address roll back is supported.
3	7	TRL	Set to 1 to latch buffer data to Tx channels.
3	6	RRL	Set to 1 to latch buffer data to Rx channels.
3	5	TAL	Set to 1 to latch buffer data to Tx DACs.
3	4	RAL	Set to 1 to latch buffer data to Rx DACs.
3	3	PH Set (PSS)	Set to ‘10’ or ‘01’ for 8-bit phase-only or gain-only data write.
3	2	GA Set (GAS)	
3	1	NB1	Correction bits for error detection.
3	0	NB0	
4	7:0	Data byte – D[7:0]	8-bit phase or gain set data sent on the SDI line. Additional 8-bit data streams would be written to phase or gain set registers of subsequent channels.

5.2 Look-Up Table (LUT) Read/Write

LCL_LUT_RD, LCL_LUT_WR, and GBL_LUT_WR modes provide access to the four available LUTs (TXV, TXH, RXV, and RXH LUTs), where each LUT stores 4-channel gain and phase settings for the corresponding Tx/Rx mode and polarization. The user can specify which LUTs to be accessed by setting bits [7:4] of the second byte of the command sequence. For each LUT, the 7-bit LUT address points to 128 locations total with each location storing 4 × 16 bits of data (4 channels × 16 bits), as illustrated in Figure 20.

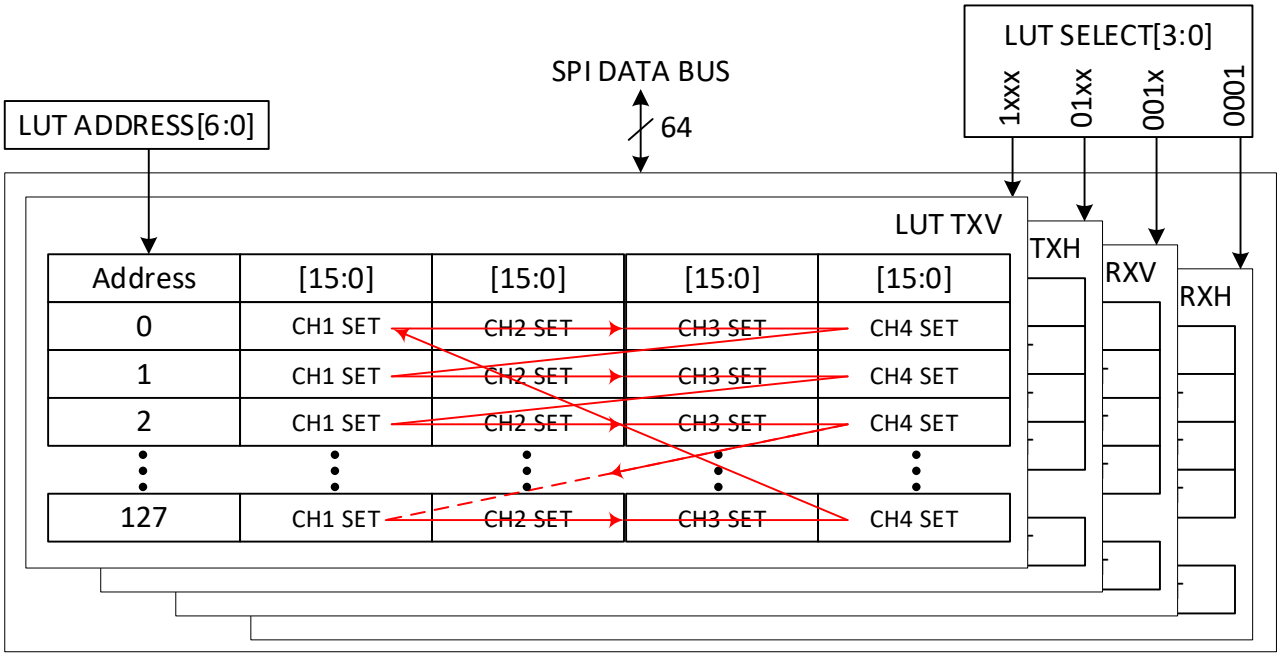


Figure 20. LUT Memory Structure

5.2.1 LCL_LUT_RD

Byte1								Byte2					Byte3								Byte4	Byte5
7	6	5	4	3	2	1	0	7	6	5	4	3…0	7	6	5	4	3	2	1	0	7:0	7:0
Mode			Chip Address					LUT Select				Reserved	LUT Address							RSV	Read Data	
0	1	1	ADD4	ADD3	ADD2	ADD1	ADD0	LS3	LS2	LS1	LS0	0000	LA6	LA5	LA4	LA3	LA2	LA1	LA0	0	D[15:8]	D[7:0]

Figure 21. LCL_LUT_RD Command Bit Sequence

Table 16. LCL_LUT_RD Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Register Write, mode = 011.
1	4:0	Chip Address	Select device address to be accessed by SPI command.
2	7:4	LUT Select	Select one LUT to read (x = can be either 0 or 1). 1xxx = Enable TXV LUT pointer. 01xx = Enable TXH LUT pointer. 001x = Enable RXV LUT pointer. 0001 = Enable RXH LUT pointer.
2	3:0	RSV	Reserved.
3	7:1	LUT Address	7-bit LUT address to be accessed. Continuous read and address roll back is supported.
3	0	RSV	Reserved.
4	7:0	Data byte 1 – D[15:8]	16-bit phase (D[15:8]) and gain (D[7:0]) SET data received on the SDO line. Each LUT location holds 4 × 16 bits (channel 1 to channel 4), and all 64 bits will be completely read after 64 clock cycles. Continuous read is supported and data from the consecutive LUT location is read at the end until the CSB is set to high again.
5	7:0	Data byte 2 – D[7:0]	

5.2.2 LCL_LUT_WR

Byte1								Byte2					Byte3								Byte4	Byte5
7	6	5	4	3	2	1	0	7	6	5	4	3…0	7	6	5	4	3	2	1	0	7:0	7:0
Mode			Chip Address					LUT Select				Reserved	LUT Address							RSV	Write Data	
1	0	0	ADD4	ADD3	ADD2	ADD1	ADD0	LS3	LS2	LS1	LS0	0000	LA6	LA5	LA4	LA3	LA2	LA1	LA0	0	D[15:8]	D[7:0]

Figure 22. LCL_LUT_WR Command Bit Sequence

Table 17. LCL_LUT_WR Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Register Write, mode = 100.
1	4:0	Chip Address	Select device address to be accessed by SPI command.
2	7:4	LUT Select	Select one LUT to write (x = can be either 0 or 1). 1xxx = Enable TXV LUT pointer. 01xx = Enable TXH LUT pointer. 001x = Enable RXV LUT pointer. 0001 = Enable RXH LUT pointer.
2	3:0	RSV	Reserved.
3	7:1	LUT Address	7-bit LUT address to be accessed. Continuous write and address roll back is supported.
3	0	RSV	Reserved.
4	7:0	Data byte 1 – D[15:8]	16-bit phase (D[15:8]) and gain (D[7:0]) SET data sent on the SDI line. Each LUT location holds 4 × 16 bits (channel 1 to channel 4), and all 64 bits will be completely written after 64 clock cycles. Continuous write is supported, and additional data would be uploaded to the sequential LUT locations.
5	7:0	Data byte 2 – D[7:0]	

5.2.3 GBL_LUT_WR

Byte1								Byte2					Byte3								Byte4	Byte5
7	6	5	4	3	2	1	0	7	6	5	4	3…0	7	6	5	4	3	2	1	0	7:0	7:0
Mode			SA Enable	Sub-Array Index				LUT Select				Reserved	LUT Address							RSV	Write Data	
1	0	1	SE	SA3	SA2	SA1	SA0	LS3	LS2	LS1	LS0	0000	LA6	LA5	LA4	LA3	LA2	LA1	LA0	0	D[15:8]	D[7:0]

Figure 23. GBL_LUT_WR Command Bit Sequence

Table 18. GBL_LUT_WR Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Register Write, mode = 101.
1	4	SA Enable	Set to 1 to enable sub-array feature.
1	3:0	Sub-Array Index	Select sub-array to be accessed by SPI command. Sub-array index information for each chip is stored in the CHIP_INFO register.

Byte	Bit	Description	Comment
2	7:4	LUT Select	Select one LUT to write (x = can be either 0 or 1). 1xxx = Enable TXV LUT pointer. 01xx = Enable TXH LUT pointer. 001x = Enable RXV LUT pointer. 0001 = Enable RXH LUT pointer.
2	3:0	RSV	Reserved.
3	7:1	LUT Address	7-bit LUT address to be accessed. Continuous write and address roll back is supported.
3	0	RSV	Reserved.
4	7:0	Data byte 1 – D[15:8]	16-bit phase (D[15:8]) and gain (D[7:0]) SET data sent on the SDI line. Each LUT location holds 4 × 16 bits (channel 1 to channel 4), and all 64 bits will be completely written after 64 clock cycles. Continuous write is supported, and additional data would be uploaded to the sequential LUT locations.
5	7:0	Data byte 2 – D[7:0]	

5.3 Fast Beam Steering (FBS)

Fast Beam Steering mode allows for fast configuration of gain and phase settings in the chip through pre-loaded gain and phase states in memory. The LCL_FBS command sequence programs a single chip with the use of the device address. The GBL_FBS command programs all chips connected to the SPI master or just selected chips within a sub-array, specified by the Sub-Array Index bits, if the sub-array feature is enabled.

5.3.1 LCL_FBS

Byte1								Byte2								Byte3		Byte4	
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7:1	0	7:1	0
Mode			Chip Address					LUT Enable		LUT Pointer		RSV	GLEN	TRX	RSV	LUT Address	Tx/Rx/GL	LUT Address	Tx/Rx/GL
1	1	0	ADD4	ADD3	ADD2	ADD1	ADD0	V_POL_EN	H_POL_EN	PVER	PHOR	0	GLEN	TRX	0	LA[6:0]	TRX_GL	LA[6:0]	TRX_GL

Figure 24. LCL_FBS Command Bit Sequence

Table 19. LCL_FBS Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Register Write, mode = 111.
1	4:0	Chip Address	Select device address to be accessed by SPI command.
2	7	V_POL_EN	Enable vertical LUTs. If enabled, data will be latched to vertical channels.
2	6	H_POL_EN	Enable horizontal LUTs. If enabled, data will be latched to horizontal channels.
2	5	PVER	Select LUT pointer for each polarization. ▪ [PVER, PHOR] = [1, 1], set both vertical and horizontal LUT pointers with the same LUT address. ▪ [PVER, PHOR] = [1, 0], set vertical LUT address only. ▪ [PVER, PHOR] = [0, 1], set horizontal LUT address only. ▪ [PVER, PHOR] = [0, 0], set vertical LUT pointer with the first LUT address and set horizontal LUT pointer with the second LUT address.
2	4	PHOR	

Byte	Bit	Description	Comment
2	3	RSV	Reserved.
2	2	GLEN	Enable global latch at the end of the command sequence. Set to 0 for local (only the specified chip address).
2	1	TRX	For global latch mode (GLEN = 1), select Tx or Rx mode at the end of the command sequence. 0 = Rx 1 = Tx Not used for local latch mode (GLEN = 0).
2	0	RSV	Reserved.
3	7:1	LUT Address	7-bit LUT address to be accessed.
3	0	TRX_GL	For global latch mode, set to 1 if this is the last byte of the command sequence for global latch mode. For local latch mode, use this bit for Tx/Rx selection. 0 = Rx 1 = Tx
4	7:1	LUT Address	7-bit LUT address to be accessed.
4	0	TRX_GL	For global latch mode, set to 1 if this is the last byte of the command sequence for global latch mode. For local latch mode, use this bit for Tx/Rx selection. 0 = Rx 1 = Tx

5.3.2 GBL_FBS

Byte1								Byte2								Byte3		Byte4	
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7:1	0	7:1	0
Mode			SA Enable	Sub-Array Index				LUT Enable		LUT Pointer		RSV	GLEN	TRX	RSV	LUT Address	Tx/Rx/GL	LUT Address	Tx/Rx/GL
1	1	1	SE	SA3	SA2	SA1	SA0	V_POL_EN	H_POL_EN	PVER	PHOR	0	GLEN	TRX	0	LA[6:0]	TRX_GL	LA[6:0]	TRX_GL

Figure 25. GBL_FBS Command Bit Sequence

Table 20. GBL_FBS Command Bit Definition

Byte	Bit	Description	Comment
1	7:5	Mode Control	For Local Register Write, mode = 111.
1	4	SA Enable	Set to 1 to enable sub-array feature.
1	3:0	Sub-Array Index	Select sub-array to be accessed by SPI command. Sub-array index information for each chip is stored in the CHIP_INFO register.
2	7	V_POL_EN	Enable vertical LUTs. If enabled, data will be latched to vertical channels.
2	6	H_POL_EN	Enable horizontal LUTs. If enabled, data will be latched to horizontal channels.
2	5	PVER	Select LUT pointer for each polarization. ▪ [PVER, PHOR] = [1, 1], set both vertical and horizontal LUT pointers with the same LUT address. ▪ [PVER, PHOR] = [1, 0], set vertical LUT address only. ▪ [PVER, PHOR] = [0, 1], set horizontal LUT address only. ▪ [PVER, PHOR] = [0, 0], set vertical LUT pointer with the first LUT address and set horizontal LUT pointer with the second LUT address.
2	4	PHOR	
2	3	RSV	Reserved.
2	2	GLEN	Enable global latch at the end of the command sequence. Set to 0 for local (only the specified sub-array).
2	1	TRX	For global latch mode (GLEN = 1), select Tx or Rx mode at the end of the command sequence. 0 = Rx 1 = Tx Not used for local latch mode (GLEN = 0).
2	0	RSV	Reserved.
3	7:1	LUT Address	7-bit LUT address to be accessed.
3	0	TRX_GL	For global latch mode, set to 1 if this is the last byte of the command sequence for global latch mode. For local latch mode, use this bit for Tx/Rx selection. 0 = Rx 1 = Tx
4	7:1	LUT Address	7-bit LUT address to be accessed.
4	0	TRX_GL	For global latch mode, set to 1 if this is the last byte of the command sequence for global latch mode. For local latch mode, use this bit for Tx/Rx selection. 0 = Rx 1 = Tx

Timing requirements for general Read/Write SPI operations are shown and described for a V_{DD} of +2.5V and 50°C ambient temperature.

Table 21. SPI Timing Typical Specifications

Symbol	Test Condition	Minimum	Typical	Maximum	Unit
t_S	CSB to SCLK setup time	TBD	-	-	ns
t_{DS}	SDI data setup time	TBD	-	-	ns
t_{DH}	SDI data hold time	TBD	-	-	ns
t_{CLK}	SCLK period	TBD	-	-	ns
t_{HI}	SCLK high time	TBD	-	-	ns
t_{DO}	SCLK falling edge to valid SDO (first valid output bit in a READ operation)	-	-	TBD	ns
t_H	SCLK to CSB hold time	TBD	-	-	ns
t_{CSB_HI}	CSB high time	TBD	-	-	ns

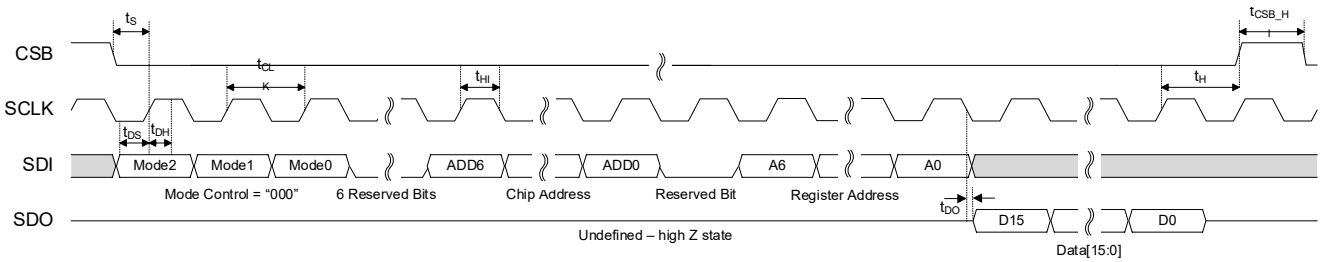


Figure 26. Timing Specification Diagram

6. Register Information

6.1 Control Configuration Register (CTRL_CFG)

Address: 0x00 Reset: 0x0049

Bit	Field	Type	Description
15:13	RSV	RW	Reserved.
12	LUT_IND_START	WO	1 = Sets the LUT pointer for both Tx and Rx to the start address defined in HLUT_START (for horizontal polarization) and VLUT_START (for vertical polarization).
11	SHIFTREG_ADDR_EN	RO	1 = Shift register address is programmed and effective.
10	SHIFTREG_ADDR_PROG	WO	8-bit shift register is placed between ADD0 pin (in) and ADD1 pin (out). To program the address, set this bit, then, without releasing CSB, send in 8-bit data to ADD0 pin starting with LSB. Existing data is pushed out of ADD1 pin. New chip address = shift_reg[7:0].
9	IO_PROTOCOL	RO	Set by the external SPIB_LVDS pin. 0 = SPI mode (ADD0 - ADD3 pins are used for the chip address). 1 = LVDS mode (ADD2 pin is defined as SDIB pin and ADD3 is defined as SCLKB pin; only ADD0 and ADD1 will be used for the chip address).
8	ERR_STATUS_BIT	R/W1C	0 = No error observed. 1 = Error observed. Write 1 to clear the bit.
7	ERR_DET_EN	RW	0 = Disable error check. 1 = Enable error check (additional 16-bit CRC data to be sent at the end).
6	TAL_RAL_EN	RW	0 = Disable the TAL or RAL functionality. 1 = Enable the TAL or RAL functionality in LCL_REG_WR or GBL_REG_WR commands.
5	RESET	WO	1 = Reset the chip (auto self-reset to 0)
4	IO_TEST	WO	Enable IO test mode for IOs' VIH/VIL and MOSI's VOL/VOH tests, only reset by power-on and hardware reset. In IO test mode, SDO pin is output pin and its logic is one of the following: • CSB • SCLK • SDI • ADD0-ADD3 • TR • TLOAD • RLOAD • STDBY
3	MANUAL_EN	RW	0 = All channels are controlled by TRX operation. 1 = Individual channel can be enabled/disabled by CH_ENS bits.
2	SCAN_MODE	WO	1 = Enable scan test mode; only reset by power-on and hardware reset.
1	SYNC_TRX	RW	0 = Front-end modules and internal switches are controlled by SW_TRX. 1 Front-end modules and internal switches are controlled by TRX bit (SW_TRX[7]) or TR(pin). Check TRX_CONT_MODE.
0	TRX_CONT_MODE	RW	0 = Enable the External Pin Configuration Mode (PIN_CFG Register active). 1 = SPI control.

6.2 Chip Configuration Register (CHIP_INFO)

Address: 0x01 Reset: 0x0000

Bit	Field	Type	Description
15:8	RSV	RW	Reserved.
7:6	OSC_FREQ	RW	Oscillator frequency selection: 0 = 80MHz; 1 = 40MHz; 2 = 20MHz; 3 = OFF.
5	OSC_EN	RW	Enable oscillator.
4	OTP_FSM_START	WO	Start OTP state machine.
3:0	SA_INDEX	RW	Sub-array index for the chip.

6.3 External Pin Configuration Register (PIN_CFG)

Address: 0x02 Reset: 0x0000

Bit	Field	Type	Description
15:7	RSV	RW	Reserved.
6:2	EXT_PIN_MODE	RW	Set the mode for external pin functionality.
1:0	RSV	RW	Reserved.

6.4 HLUT Active Index Storage Register (HLUT_INFO)

Address: 0x03 Reset: 0x0000

Bit	Field	Type	Description
15	RSV	RO	Reserved.
14:8	TXH_LUT_IND	RO	Stores the active LUT index for horizontal TX SRAM. This will be updated automatically by the FBS modes and external TLOAD/RLOAD pins.
7	RSV	RO	Reserved.
6:0	RXH_LUT_IND	RO	Stores the active LUT index for horizontal RX SRAM. This will be updated automatically by the FBS modes and external TLOAD/RLOAD pins.

6.5 VLUT Active Index Storage Register (VLUT_INFO)

Address: 0x04 Reset: 0x0000

Bit	Field	Type	Description
15	RSV	RO	Reserved.
14:8	TXV_LUT_IND	RO	Stores the active LUT index for vertical TX SRAM. This will be updated automatically by the FBS modes and external TLOAD/RLOAD pins.
7	RSV	RO	Reserved.
6:0	RXV_LUT_IND	RO	Stores the active LUT index for vertical RX SRAM. This will be updated automatically by the FBS modes and external TLOAD/RLOAD pins.

6.6 HLUT Start Pointer Storage Register (HLUT_START)

Address: 0x05 Reset: 0x0000

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14:8	TXH_LUT_START	RW	LUT start index for horizontal TX SRAM. The user can change LUT location starting from this index by TLOAD and RLOAD pins.
7	RSV	RW	Reserved.
6:0	RXH_LUT_START	RW	LUT start index for horizontal RX SRAM. The user can change LUT location starting from this index by TLOAD and RLOAD pins.

6.7 HLUT Stop Pointer Storage Register (HLUT_STOP)

Address: 0x06 Reset: 0x7F7F

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14:8	TXH_LUT_STOP	RW	LUT stop index for horizontal TX SRAM. The user can change LUT location up to this index by TLOAD and RLOAD pins. After this index, the pointer will go back to the start index.
7	RSV	RW	Reserved.
6:0	RXH_LUT_STOP	RW	LUT stop index for horizontal RX SRAM. The user can change LUT location up to this index by TLOAD and RLOAD pins. After this index, the pointer will go back to the start index.

6.8 VLUT Start Pointer Storage Register (VLUT_START)

Address: 0x07 Reset: 0x0000

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14:8	TXV_LUT_START	RW	LUT start index for vertical TX SRAM. The user can change LUT location starting from this index by TLOAD and RLOAD pins.
7	RSV	RW	Reserved.
6:0	RXV_LUT_START	RW	LUT start index for vertical RX SRAM. The user can change LUT location starting from this index by TLOAD and RLOAD pins.

6.9 VLUT Stop Pointer Storage Register (VLUT_STOP)

Address: 0x08 Reset: 0x7F7F

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14:8	TXV_LUT_STOP	RW	LUT stop index for vertical TX SRAM. The user can change LUT location up to this index by TLOAD and RLOAD pins. After this index, the pointer will go back to the start index.
7	RSV	RW	Reserved.
6:0	RXV_LUT_STOP	RW	LUT stop index for vertical RX SRAM. The user can change LUT location up to this index by TLOAD and RLOAD pins. After this index, the pointer will go back to the start index.

6.10 SRAM BIST Register (BIST)

Address: 0x09 Reset: 0x0000

Bit	Field	Type	Description
15:12	RSV	RO	Reserved.
11	SRAM_DONE	RO	SRAM access status (initialization, BIST or CRC): 0 = When any of SRAM_CRC or SRAM_BIST or SRAM INIT is set to 1, an SRAM access is ongoing. Otherwise, there is no SRAM access ongoing. 1 = SRAM access is done.
10:8	SRAM_ERR	RO	Number of errors during SRAM BIST: 0 = No error. 4 = One stuck-at-1 fault at an even-bit location or one stuck-at-0 fault at an odd-bit location. 5 = One stuck-at-1 fault at an odd-bit location or one stuck-at-0 fault at an even-bit location. 7 = More than one error.
7:5	RSV	RO	Reserved.
4:3	SRAM_SEL	RW	00 = Vertical TX SRAM. 01 = Horizontal TX SRAM. 10 = Vertical RX SRAM. 11 = Horizontal RX SRAM.
2	SRAM_CRC	RW	Request an SRAM CRC check by writing 1. The SRAM CRC algorithm is as follows: 1. Initial value is 0xFFFF. 2. CRC generator polynomial is $x^{16} + x^{12} + x^5 + 1$. 3. The sequence is: a. N = SRAM_SEL[4:3] and ADDR = 0. b. Get data from LUT[N](ADDR). c. Calculate CRC for each channel starting with MSB. d. If ADDR = 2^7-1, finish CRC check. Otherwise, ADDR = ADDR + 1 and go to step b.
1	SRAM_BIST	RW	Request an SRAM BIST by writing 1.
0	SRAM_INIT	RW	Request an SRAM initialization by writing 1. All of SRAM data will be initialized to 0.

6.11 SRAM CRC Result Register (CRC_RESULT)

Address: 0x0A Reset: 0xFFFF

Bit	Field	Type	Description
15:0	CRC_RESULT	RO	16-bit SRAM CRC result.

6.12 TRX Switch Control Register (SW_TRX)

Address: 0x0B Reset: 0x0C00

Bit	Field	Type	Description
15:12	RSV	RW	Reserved.
11	MB_EN	RW	Enable chip reference bias. 0 = Disable chip bias. 1 = Enable chip bias.
10	STANDBY	RW	0 = Operation mode. 1 = Put the chip in standby mode (all channels are power-disabled).
9	H_POL_EN	RW	0 = Disable channels with horizontal polarization. 1 = Enable channels with horizontal polarization.
8	V_POL_EN	RW	0 = Disable channels with vertical polarization. 1 = Enable channels with vertical polarization.
7	TRX	RW	Software TRX Control. 0 = RX mode. 1 = TX mode. This bit is overwritten by TR Pin if CTRL_CFG[0] = 0. State of the TR pin can be read back from this bit.
6	SW_FEM_TR_MODE	RW	0 = Negative pins are floating. 1 = Positive pins are floating.
5	SW_DRV_TR_STATE	RW	0 = Outputs are GND. 1 = Outputs are High/Low.
4	SW_DRV_EN_TR	RW	0 = TRX pins for FEMs are disabled (floating). 1 = Enable TRX pins.
3	TRX_EXTH	RW	This bit controls the external FEM switches for horizontal polarization. 0 = RX mode. 1 = TX mode.
2	TRX_EXTV	RW	This bit controls the external FEM switches for vertical polarization. 0 = RX mode. 1 = TX mode.
1	TRX_BFH	RW	This bit controls the beamformer switches for horizontal polarization. 0 = RX mode. 1 = TX mode.
0	TRX_BFV	RW	This bit controls the beamformer switches for vertical polarization. 0 = RX mode. 1 = TX mode.

6.13 Channel Power Enable Register (CH_ENS)

Address: 0x0C Reset: 0x0000

Bit	Field	Type	Description
15	RXH4_EN	RW	0 = Disable. 1 = Enable.
14	RXH3_EN	RW	0 = Disable. 1 = Enable.
13	RXH2_EN	RW	0 = Disable. 1 = Enable.
12	RXH1_EN	RW	0 = Disable. 1 = Enable.
11	RXV4_EN	RW	0 = Disable. 1 = Enable.
10	RXV3_EN	RW	0 = Disable. 1 = Enable.
9	RXV2_EN	RW	0 = Disable. 1 = Enable.
8	RXV1_EN	RW	0 = Disable. 1 = Enable
7	TXH4_EN	RW	0 = Disable. 1 = Enable
6	TXH3_EN	RW	0 = Disable. 1 = Enable
5	TXH2_EN	RW	0 = Disable. 1 = Enable
4	TXH1_EN	RW	0 = Disable. 1 = Enable
3	TXV4_EN	RW	0 = Disable. 1 = Enable
2	TXV3_EN	RW	0 = Disable. 1 = Enable
1	TXV2_EN	RW	0 = Disable. 1 = Enable
0	TXV1_EN	RW	0 = Disable. 1 = Enable

6.14 Chip ID Register (CHIP_ID)

Address: 0x0D Reset: 0x0000

Bit	Field	Type	Description
15:14	ID_CLASS	RO	0: Beamformer.
13:12	ID_FREQ	RO	0 = X/Ku band. 1 = Ku band. 2 = Ka band.
11:8	BASE_REV	RO	Base revision.

Bit	Field	Type	Description
7:4	METAL_REV	RO	Metal revision.
3:0	VARIANTS	RO	Variants.

6.15 Master Bias Control Register (MBIAS)

Address: 0x0E Reset: 0x0093

Bit	Field	Type	Description
15:8	RSV	RW	Reserved.
7:5	PTAT2_SLOPE	RW	PTAT2 slope control.
4:2	PTADJ	RW	Internal reference current generator level control (±30% adjustment).
1	MB_BG_SEL	RW	0 = BG source from PTAT generator. 1 = BG source from POR.
0	MB_EN	RO	Shadow bit of SW_TRX[11] (MB_EN). 0 = Chip bias disabled. 1 = Chip bias enabled.

6.16 ADC Clock Configuration Register (CLK_CFG)

Address: 0x0F Reset: 0xFB30

Bit	Field	Type	Description
15:12	ADC_START_DELAY	RW	Determines the delay between ADC source selection and acquisition start in multiples of ADC clock (ADC_CLK) cycles.
11:8	BASE_CLK_CTRL	RW	Select base clock (BASE_CLK) as OSC_FREQ/(N+1). N = BASE_CLK_CTRL.
7:4	ADC_CLK_HIGH	RW	Select ADC clock's high width as BASE_CLK*(N+1). N = ADC_CLK_HIGH.
3:0	ADC_CLK_LOW	RW	Select ADC clock's low width as BASE_CLK*(N+1). N = ADC_CLK_LOW.

6.17 ADC Configuration Register (ADC_CFG)

Address: 0x10 Reset: 0x0380

Bit	Field	Type	Description
15:11	ADC_SEL	RW	ADC Mux Selection Bits. 31 = ADC channel 32: VSENS4 30 = ADC channel 31: VSENS3 29 = ADC channel 30: VSENS2 28 = ADC channel 29: VSENS1 27 = ADC channel 28: Unused 26 = ADC channel 27: AVDDn 25 = ADC channel 26: VDDPA 24 = ADC channel 25: DVDD 23 = ADC channel 24: VDD 22 = ADC channel 23: IDC 21 = ADC channel 22: TSENS2 20 = ADC channel 21: TSENS1 19 = ADC channel 20: PREF10 18 = ADC channel 19: PDET10 17 = ADC channel 18: PREF9 16 = ADC channel 17: PDET9 15 = ADC channel 16: PREF8 14 = ADC channel 15: PDET8 13 = ADC channel 14: PREF7 12 = ADC channel 13: PDET7 11 = ADC channel 12: PREF6 10 = ADC channel 11: PDET6 9 = ADC channel 10: PREF5 8 = ADC channel 9: PDET5 7 = ADC channel 8: PREF4 6 = ADC channel 7: PDET4 5 = ADC channel 6: PREF3 4 = ADC channel 5: PDET3 3 = ADC channel 4: PREF2 2 = ADC channel 3: PDET2 1 = ADC channel 2: PREF1 0 = ADC channel 1: PDET1
10	ADC_SEL_SOURCE	RW	ADC mux selector source. 0 = SRQ (recommended setting) 1 = ADC_SEL
9:7	ADC_AVG	RW	0: No averaging. 1–6 = Averaging count = 2^{ADC_AVG} 7 = Averaging count = 2^6
6	PD_DIFF_MODE	RW	0 = Difference between measured PREF and measured PDET is calculated and stored in PDET. Registered PDET = measured PREF - measured PDET. 1 = No difference calculated. Measured PDET data is stored. Registered PDET = measured PDET.

Bit	Field	Type	Description
5:4	ADC_AOUT_SEL	RW	AOUT ADC Mux Selection Bits. 0 = ADC_MUX 1 = cbn1_test 2 = vref(v1p5) 3 = vcm(v0p9)
3	ADC_AOUT_EN	RW	Enable AOUT mux.
2	LSB_SEL	RW	0 = LSB is Vref/1023 1 = LSB is Vref/1055
1	CHOPPER_EN	RW	Chopper Enable. Can be set to either 0 or 1 (for slightly improved ADC performance with averaging).
0	ADC_I_2X	RW	Double ADC bias current.

6.18 Sensor Activation Register 1 (ADC_SRQ1)

Address: 0x11 Reset: 0x0000

Bit	Field	Type	Description
15	VSENS_3_4	WO	Set to read VSENS3 and VSENS4 external pins (ADC channel 31, 32).
14	VSENS_1_2	WO	Set to read VSENS1 and VSENS2 external pins (ADC channel 29, 30).
13	VSENS_NEG	WO	Set to read the negative voltage supply (ADC channel 27).
12	DC_SENS	WO	Set to read sensors for internal reference current, VDD, DVDD and VDDPA [1] (ADC channel 23, 24, 25, 26).
11	TSENS2	WO	Set to read TSENS2 (ADC channel 22).
10	TSENS1	WO	Set to read TSENS1 (ADC channel 21).
9	PDET_RFC_H	WO	Set to read PDET10 and PREF10 (ADC channel 19, 20).
8	PDET_TX4_H	WO	Set to read PDET9 and PREF9 (ADC channel 17, 18).
7	PDET_TX3_H	WO	Set to read PDET8 and PREF8 (ADC channel 15, 16).
6	PDET_TX2_H	WO	Set to read PDET7 and PREF7 (ADC channel 13, 14).
5	PDET_TX1_H	WO	Set to read PDET6 and PREF6 (ADC channel 11, 12).
4	PDET_RFC_V	WO	Set to read PDET5 and PREF5 (ADC channel 9, 10).
3	PDET_TX4_V	WO	Set to read PDET4 and PREF4 (ADC channel 7, 8).
2	PDET_TX3_V	WO	Set to read PDET3 and PREF3 (ADC channel 5, 6).
1	PDET_TX2_V	WO	Set to read PDET2 and PREF2 (ADC channel 3, 4).
0	PDET_TX1_V	WO	Set to read PDET1 and PREF1 (ADC channel 1, 2).

1. V200 release.

6.19 Sensor Activation Register 2 (ADC_SRQ2)

Address: 0x12 Reset: 0x0000

Bit	Field	Type	Description
15:0	RSV	WO	Reserved.

6.20 Sensor Enable Register (SENSOR_EN)

Address: 0x13 Reset: 0x0000

Bit	Field	Type	Description
15	VSENS_3_4_EN	RW	Enable the sensor for VSENS3 and VSENS4.
14	VSENS_1_2_EN	RW	Enable the sensor for VSENS1 and VSENS2.
13	VSENS_NEG_EN	RW	Enable the sensor for negative supply.
12	DC_SENS_EN	RW	Enable the sensor for DC current, VDD, and DVDD.
11	TSENS2_EN	RW	Enable the sensor for TSENS2.
10	TSENS1_EN	RW	Enable the sensor for TSENS1.
9	PDET_RFC_H_EN	RW	Enable the sensor for PDET10 and PREF10.
8	PDET_TX4_H_EN	RW	Enable the sensor for PDET9 and PREF9.
7	PDET_TX3_H_EN	RW	Enable the sensor for PDET8 and PREF8.
6	PDET_TX2_H_EN	RW	Enable the sensor for PDET7 and PREF7.
5	PDET_TX1_H_EN	RW	Enable the sensor for PDET6 and PREF6.
4	PDET_RFC_V_EN	RW	Enable the sensor for PDET5 and PREF5.
3	PDET_TX4_V_EN	RW	Enable the sensor for PDET4 and PREF4.
2	PDET_TX3_V_EN	RW	Enable the sensor for PDET3 and PREF3.
1	PDET_TX2_V_EN	RW	Enable the sensor for PDET2 and PREF2.
0	PDET_TX1_V_EN	RW	Enable the sensor for PDET1 and PREF1.

6.21 Sensor Configuration Register (SENSOR_CFG)

Address: 0x14 Reset: 0x0524

Bit	Field	Type	Description
15:14	IREF_SEL	RW	Reference current selection. 00 = BG 01 = PTAT 10 = PTAT2 11 = Not valid
13:12	TSENS_POL_CFG	RW	Temperature sensor polarization control. 00 = Averaging 01 = Horizontal polarization only 10 = Vertical polarization only 11 = Not valid
11	RSV	RW	Reserved.
10:9	PDET_BUFF_PROF	RW	PDET buffer current profile.
8:7	PDET_CORE_PROF	RW	PDET core current profile.
6:4	PDET_CORE_BIAS	RW	PDET block bias tuning.
3:1	PDET_BUFFER_BIAS	RW	PDET buffer bias tuning.
0	PDET_EN	RW	Enable PDET.

6.22 Scratch Register (SCRATCH)

Address: 0x15 Reset: 0x0000

Bit	Field	Type	Description
15:0	RSV	RW	Reserved for random R/W by the user.

6.23 TX Vertical Set Register (TXVn_SET) (n = 1–4)

Address: 0x16 + (n-1) Reset: 0x003F

Bit	Field	Type	Description
15:8	TX_PHASE_CTRL	RW	Phase control.
7:0	TX_GAIN_CTRL	RW	Gain control.

6.24 TX Horizontal Set Register (TXHn_SET) (n = 1–4)

Address: 0x1A + (n-1) Reset: 0x003F

Bit	Field	Type	Description
15:8	TX_PHASE_CTRL	RW	Phase control.
7:0	TX_GAIN_CTRL	RW	Gain control.

6.25 RX Vertical Set Register (RXVn_SET) (n = 1–4)

Address: 0x1E + (n-1) Reset: 0x003F

Bit	Field	Type	Description
15:8	RX_PHASE_CTRL	RW	Phase control.
7:0	RX_GAIN_CTRL	RW	Gain control.

6.26 RX Horizontal Set Register (RXHn_SET) (n = 1–4)

Address: 0x22 + (n-1) Reset: 0x003F

Bit	Field	Type	Description
15:8	RX_PHASE_CTRL	RW	Phase control.
7:0	RX_GAIN_CTRL	RW	Gain control.

6.27 TX Vertical Offset Register (TXVn_OFFSET) (n = 1–4)

Address: 0x26 + (n-1) Reset: 0x0408

Bit	Field	Type	Description
15:14	RSV	RW	Reserved.
13:11	PDET_ATEST_CTRL	RW	Control the testing scheme.
10:8	TX_CH_BIAS	RW	Channel bias setting. *Note*: This is an absolute value and not an offset value as the register name may suggest.
7:4	TX_PH_OFF	RW	Phase offset. The stored data is in two's complement format.
3:1	TX_ALIGN_OFF	RW	Align offset. The stored data is an absolute value.
0	RSV	RW	Reserved.

6.28 TX Horizontal Offset Register (TXHn_OFFSET) (n = 1–4)

Address: 0x2A + (n-1) Reset: 0x0408

Bit	Field	Type	Description
15:14	RSV	RW	Reserved.
13:11	PDET_ATEST_CTRL	RW	Control the testing scheme.
10:8	TX_CH_BIAS	RW	Channel bias setting. *Note*: This is an absolute value and not an offset value as the register name may suggest.
7:4	TX_PH_OFF	RW	Phase offset. The stored data is in two's complement format.
3:1	TX_ALIGN_OFF	RW	Align offset. The stored data is an absolute value.
0	RSV	RW	Reserved.

6.29 RX Vertical Offset Register (RXVn_OFFSET) (n = 1–4)

Address: 0x2E + (n-1) Reset: 0x0408

Bit	Field	Type	Description
15:14	RSV	RW	Reserved.
13:11	RSV	RW	Reserved.
10:8	RX_CH_BIAS	RW	Channel bias setting. *Note*: This is an absolute value and not an offset value as the register name may suggest.
7:4	RX_PH_OFF	RW	Phase offset. The stored data is in two's complement format.
3:1	RX_ALIGN_OFF	RW	Align offset. The stored data is an absolute value.
0	RSV	RW	Reserved.

6.30 RX Horizontal Offset Register (RXHn_OFFSET) (n = 1–4)

Address: 0x32 + (n-1) Reset: 0x0408

Bit	Field	Type	Description
15:14	RSV	RW	Reserved.
13:11	RSV	RW	Reserved.
10:8	RX_CH_BIAS	RW	Channel bias setting. *Note*: This is an absolute value and not an offset value as the register name may suggest.
7:4	RX_PH_OFF	RW	Phase offset. The stored data is in two's complement format.
3:1	RX_ALIGN_OFF	RW	Align offset. The stored data is an absolute value.
0	RSV	RW	Reserved.

6.31 TX Common Tune Register (TXCOM_TUNE)

Address: 0x36 Reset: 0x1520

Bit	Field	Type	Description
15:14	TX_PA_C2B	RW	PA cascode capacitance tuning bits.
13	TX_PA_RFB	RW	PA feedback resistance tuning bits.
12:11	TX_PA_RBB1	RW	PA bias resistance tuning bits.
10:9	TX_DA_CISM1	RW	DA-PA interstage frequency tuning bits.
8:6	TX_DA_RIM1	RW	DA gain tuning bits.
5:4	TX_DA_CIM1	RW	DA input frequency tuning bits.
3:2	RSV	RW	Reserved.
1:0	TX_VGA_TUNE	RW	VGA tuning bits.

6.32 TX Common Configuration Register (TXCOM_CFG)

Address: 0x37 Reset: 0x01E0

Bit	Field	Type	Description
15:14	RSV	RW	Reserved.
13	TX_CASC_EN	RW	Enable TX cascode.
12:10	PDET_ATEST_CTRL	RW	Control the testing scheme.
9	PDET_DIFF	RW	0 = PDET difference calculation. 1 = No PDET difference calculation.
8	TX_VGA_PT	RW	Select temperature profile.
7	TX_AMP_BG	RW	Select temperature profile.
6	TX_DA_PT	RW	Select temperature profile.
5	TX_PA_BG	RW	Select temperature profile.
4	TX_VGA_EN	RW	Enable VGA block.
3	TX_AMP_EN	RW	Enable AMP block.

Bit	Field	Type	Description
2	TX_DA_EN	RW	Enable DA block.
1	TX_PA_EN	RW	Enable PA block.
0	RSV	RW	Reserved.

6.33 TX Common Bias Register 1 (TXCOM_BIAS1)

Address: 0x38 Reset: 0x4924

Bit	Field	Type	Description
15:12	RSV	RW	Reserved.
11:9	TX_VGA_BIAS	RW	VGA bias current.
8:6	TX_AMP_BIAS	RW	AMP bias current.
5:3	TX_DA_BIAS	RW	DA bias current.
2:0	TX_PA_BIAS	RW	PA bias current.

6.34 TX Common Bias Register 2 (TXCOM_BIAS2)

Address: 0x39 Reset: 0x024A

Bit	Field	Type	Description
15:14	RSV	RW	Reserved.
13:12	TX_PS_TUNE	RW	PS trim bits.
11:9	TX_VGA_CASC_BIAS	RW	VGA cascode bias current.
8:6	TX_AMP_CASC_BIAS	RW	AMP cascode bias current.
5:3	TX_PA_CASC_BIAS	RW	PA cascode bias current.
2:0	TX_DA_CASC_BIAS	RW	DA cascode bias current.

6.35 RX Common Tune Register (RXCOM_TUNE)

Address: 0x3A Reset: 0x0000

Bit	Field	Type	Description
15:8	RSV	RW	Reserved.
7:6	RSV	RW	Reserved.
5:4	RSV	RW	Reserved.
3:2	RX_LNA2_TUNE	RW	LNA2 tuning bits.
1:0	RX_LNA1_TUNE	RW	LNA1 tuning bits.

6.36 RX Common Configuration Register (RXCOM_CFG)

Address: 0x3B Reset: 0x0F00

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14:13	TRX_SW_CTRL	RW	TRX Switch Bias control.
12	RX_CASC_EN	RW	Enable cascode.
11	RX_AMP_PT	RW	AMP temperature profile.
10	RX_VGA_PT	RW	VGA temperature profile.
9	RX_LNA2_PT	RW	LNA2 temperature profile.
8	RX_LNA1_PT	RW	LNA1 temperature profile.
7	RX_AMP_EN	RW	Enable AMP block.
6	RX_VGA_EN	RW	Enable VGA block.
5	RX_LNA2_EN	RW	Enable LNA2 block.
4	RX_LNA1_EN	RW	Enable LNA1 block.
3:2	RSV	RW	Reserved.
1	HIGH_LIN_MODE	RW	Enable high-linearity mode.
0	RSV	RW	Reserved.

6.37 RX Common Bias Register 1 (RXCOM_BIAS1)

Address: 0x3C Reset: 0x4924

Bit	Field	Type	Description
15	RSV	RW	Reserved.
14:12	RX_PS_BIAS	RW	PS bias current.
11:9	RX_AMP_BIAS	RW	AMP bias current.
8:6	RX_VGA_BIAS	RW	VGA bias current.
5:3	RX_LNA2_BIAS	RW	LNA2 bias current.
2:0	RX_LNA1_BIAS	RW	LNA1 bias current.

6.38 RX Common Bias Register 2 (RXCOM_BIAS2)

Address: 0x3D Reset: 0x0091

Bit	Field	Type	Description
15:14	RSV	RW	Reserved.
13:12	RX_PS_TUNE	RW	PS trim bits
11:8	RSV	RW	Reserved.
7:5	RX_AMP_CASC_BIAS	RW	AMP cascode bias current.
4:2	RX_VGA_CASC_BIAS	RW	VGA cascode bias current.
1:0	RX_LNA_CASC_BIAS	RW	LNA cascode bias current.

6.39 Spare Channel Register (TX_RX_SPARE)

Address: 0x3E Reset: 0x0000

Bit	Field	Type	Description
15:8	RSV	RW	Reserved.
7	PDET_CPL_RX_EN	RW	Enable Rx common PDET coupler.
6	PDET_CPL_TX_EN	RW	Enable Tx common PDET coupler.
5:3	PDET_COM_ATEST_CTRL	RW	Control the testing scheme for both TX and RX. 0 = PDET reference voltage (Vref). 1 = PDET output voltage (Vout). 2 = Vout-Vref difference with amplification. 3–7 = No connection.
2	PDET_DIFF	RW	0 = Difference between measured PREF and measured PDET is calculated and stored in PDET. Registered PDET = measured PREF - measured PDET. 1 = No difference calculated. Measured PDET data is stored. Registered PDET = measured PDET.
1:0	PDET_HP_EN	RW	PDET power range setting. 0 = Low-power mode. 3 = High-power mode.

6.40 ADC channel-n Data Register (ADC_DATA_CHn) (n = 1–32)

Address: 0x3F + (n-1) Reset: 0x0000

Bit	Field	Type	Description
15:11	RSV	RO	Reserved.
10	DONE	RO	ADC status.
9:0	VALUE	RO	ADC data.

6.41 DAC Configuration Register 1 (PA_LNA_DAC_CFG1)

Address: 0x5F Reset: 0x037B

Bit	Field	Type	Description
15:13	RSV	RW	Reserved.
12:10	BUFFER_CONTROL	RW	Reserved.
9:0	PA_LNA_CONTROL	RW	Select either PA or LNA modes for each DAC channel. PA_LNA_CONTROL[n-1] makes selection for DAC channel n. PA_LNA_CONTROL[n-1] = 0: LNA DAC. PA_LNA_CONTROL[n-1] = 1: PA DAC.

6.42 DAC Configuration Register 2 (PA_LNA_DAC_CFG2)

Address: 0x60 Reset: 0x014A

Bit	Field	Type	Description
15:10	RSV	RW	Reserved.
9:0	V_H_CONTROL	RW	Select polarization for each DAC channel. V_H_CONTROL[n-1] makes selection for DAC channel n. V_H_CONTROL[n-1] = 0: Vertical polarization. V_H_CONTROL[n-1] = 1: Horizontal polarization.

6.43 DAC Configuration Register 3 (PA_LNA_DAC_CFG3)

Address: 0x61 Reset: 0x0000

Bit	Field	Type	Description
15:10	RSV	RW	Reserved.
9	PA_LNA_EN10	RW	Enable DAC channel 10. 0 = Disable 1 = Enable.
8	PA_LNA_EN9	RW	Enable DAC channel 9. 0 = Disable. 1 = Enable.
7	PA_LNA_EN8	RW	Enable DAC channel 8. 0 = Disable 1 = Enable.
6	PA_LNA_EN7	RW	Enable DAC channel 7. 0 = Disable 1 = Enable.
5	PA_LNA_EN6	RW	Enable DAC channel 6. 0 = Disable 1 = Enable.
4	PA_LNA_EN5	RW	Enable DAC channel 5. 0 = Disable 1 = Enable.

Bit	Field	Type	Description
3	PA_LNA_EN4	RW	Enable DAC channel 4. 0 = Disable 1 = Enable.
2	PA_LNA_EN3	RW	Enable DAC channel 3. 0 = Disable 1 = Enable.
1	PA_LNA_EN2	RW	Enable DAC channel 2. 0 = Disable 1 = Enable.
0	PA_LNA_EN1	RW	Enable DAC channel 1. 0 = Disable 1 = Enable.

6.44 DAC Configuration Register 4 (PA_LNA_DAC_CFG4)

Address: 0x62 Reset: 0x0000

Bit	Field	Type	Description
15:12	LNA_DAC_RES_CONTROL	RW	Reserved.
11:8	PA_DAC_RES_CONTROL	RW	Reserved.
7:4	LNA_DAC_REF_VOLTAGE	RW	Reserved.
3:0	PA_DAC_REF_VOLTAGE	RW	Reserved.

6.45 ON-Mode PA/LNA DAC Channel-n Data Register (DAC_ONn) (n = 1–10)

Address: 0x63 + (n-1) Reset: 0x0000

Bit	Field	Type	Description
15:9	RSV	RW	Reserved.
8:0	DAC_FINE_ON_CONT	RW	9-bit DAC data for ON-mode PA/LNA.

6.46 OFF-Mode PA DAC Data Register (DAC_PA_OFF)

Address: 0x6D Reset: 0x0000

Bit	Field	Type	Description
15:9	RSV	RW	Reserved.
8:0	DAC_PA_OFF_CONT	RW	9-bit DAC data for OFF-mode PA.

6.47 OFF-Mode LNA DAC Data Register (DAC_LNA_OFF)

Address: 0x6E Reset: 0x0100

Bit	Field	Type	Description
15:9	RSV	RW	Reserved.
8:0	DAC_PA_OFF_CONT	RW	9-bit DAC data for OFF-mode LNA.

6.48 DAC Bias Control Register (DAC_BIAS_CTRL)

Address: 0x6F Reset: 0x0000

Bit	Field	Type	Description
15:10	RSV	RW	Reserved.
9:0	RSV	RW	Reserved.

6.49 DAC Status Register (DAC_STATUS)

Address: 0x70 Reset: 0x0000

Bit	Field	Type	Description
15	TX_DAC_EN	RO	TX DAC enable status.
14	RX_DAC_EN	RO	RX DAC enable status.
13	TAL	RO	Registered TAL bit status. This bit will be updated according to the TX DAC Load (TAL) bit value in byte3 of a LCL/GBL_FBS command.
12	RAL	RO	Registered RAL bit status. This bit will be updated according to the RX DAC Load (RAL) bit value in byte3 of a LCL/GBL_FBS command.
11:10	RSV	RO	Reserved.
9:0	DAC_STATE	RO	DAC state status for each DAC channel. DAC_STATE[n-1] is DAC state status for DAC channel n. DAC_STATE[n-1] = 0: DAC bias is OFF (DAC_BIAS_CTRL[n-1] = 0). DAC_STATE[n-1] = 1: DAC bias is ON (DAC_BIAS_CTRL[n-1] = 1).

6.50 OTP Configuration Register (OTP_CFG)

Address: 0x71 Reset: 0x0014

Bit	Field	Type	Description
15	OTP_FSM_START	RO	OTP FSM start pin.
14	RSV	RW	Reserved for random R/W by the user.
13	OTP_DIN_LATCH	WO	Latch OTP output data (otp_din[7:0]) to OTP_DATAn registers. Read the previously-latched data and latch at the same time.
12:10	OTP_WR_BIT	RW	Bit number to burn during program mode. Note that fuses can only be burned one at a time.
9:6	OTP_RW_ADDRESS	RW	OTP read/write address bank to be selected.
5	OTP_PROG	RW	Enable OTP program mode. When this bit is set to 1, fuse i, selected by OTP_WR_BIT of the bank selected by OTP_RW_ADDRESS, will be burned.
4	OTP_POR	RW	OTP power-on reset. Only set this OTP_POR bit to 0 during programming. At all other times, set this bit to 1 to prevent an accidental fuse burn.
3:2	OTP_CUR	RW	OTP current control. These two bits are used to test the robustness of the read operation. 00 = Reduced reference current. 01 = Normal read operation (default). 10 = Enhanced reference current. 11 = Extremely-enhanced reference current (not used).
1	OTP_READ	RW	0 = No OTP read. 1 = Enable OTP read. All 8 fuses of the selected bank are read.
0	OTP_EN	RW	0 = Disable OTP. 1 = Enable OTP. The current generation circuit used in the read mode is activated.

6.51 OTP Data Register (OTP_DATAn) (n = 1–8)

Address: 0x72 + (n-1) Reset: 0x0000

Bit	Field	Type	Description
15:8	OTP_DATA_BYTE1	RW	High-byte OTP data at address 2^n.
17:0	OTP_DATA_BYTE0	RW	Low-byte OTP data at address 2^n.

7. Evaluation Board

7.1 Evaluation Board Image

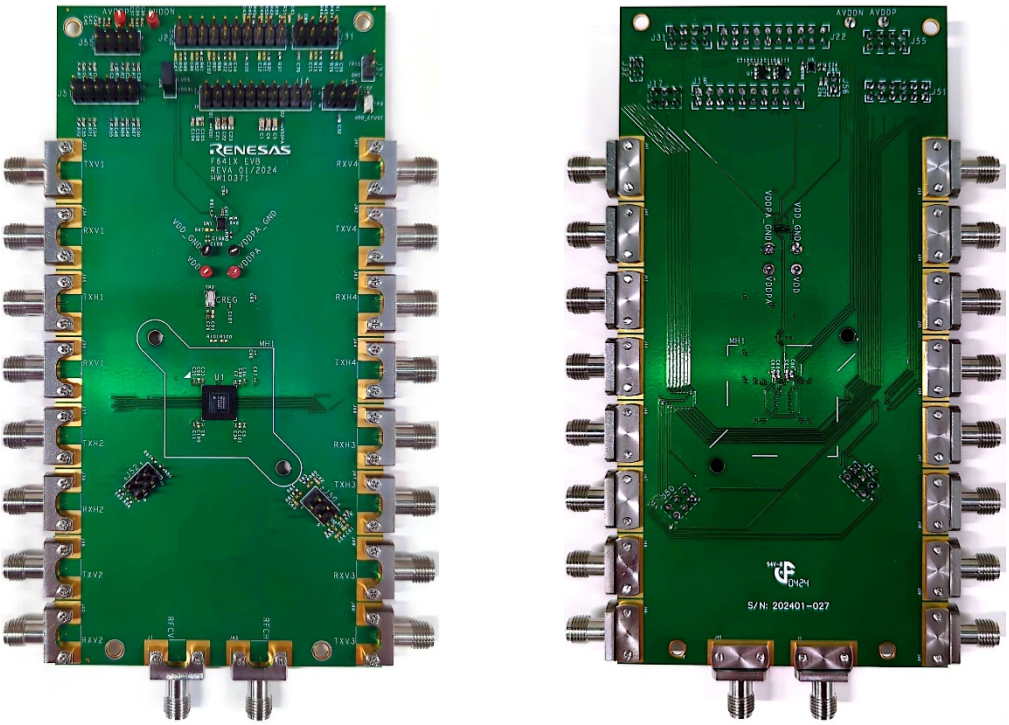


Figure 27. Evaluation Board – Top and Bottom View

7.2 Evaluation Board Applications Circuits

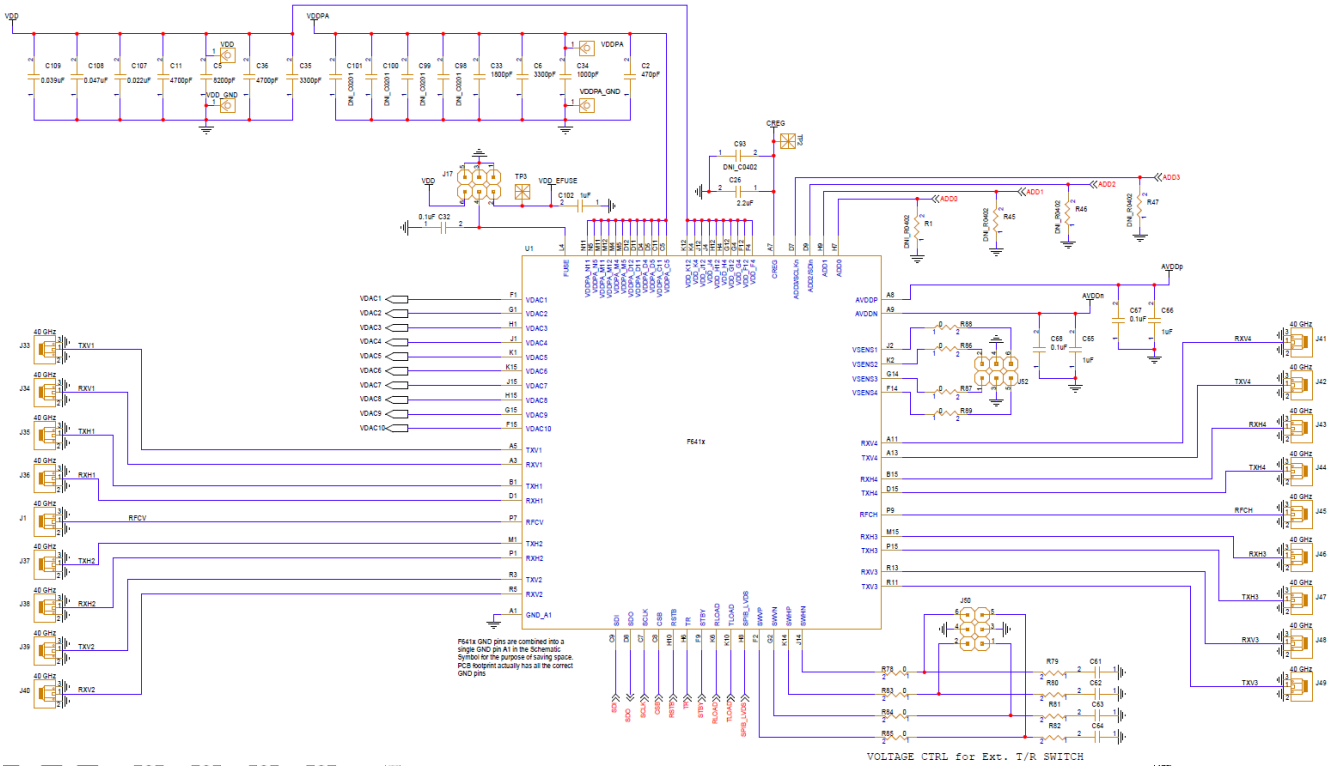


Figure 28. Evaluation Board Schematic (Part 1)

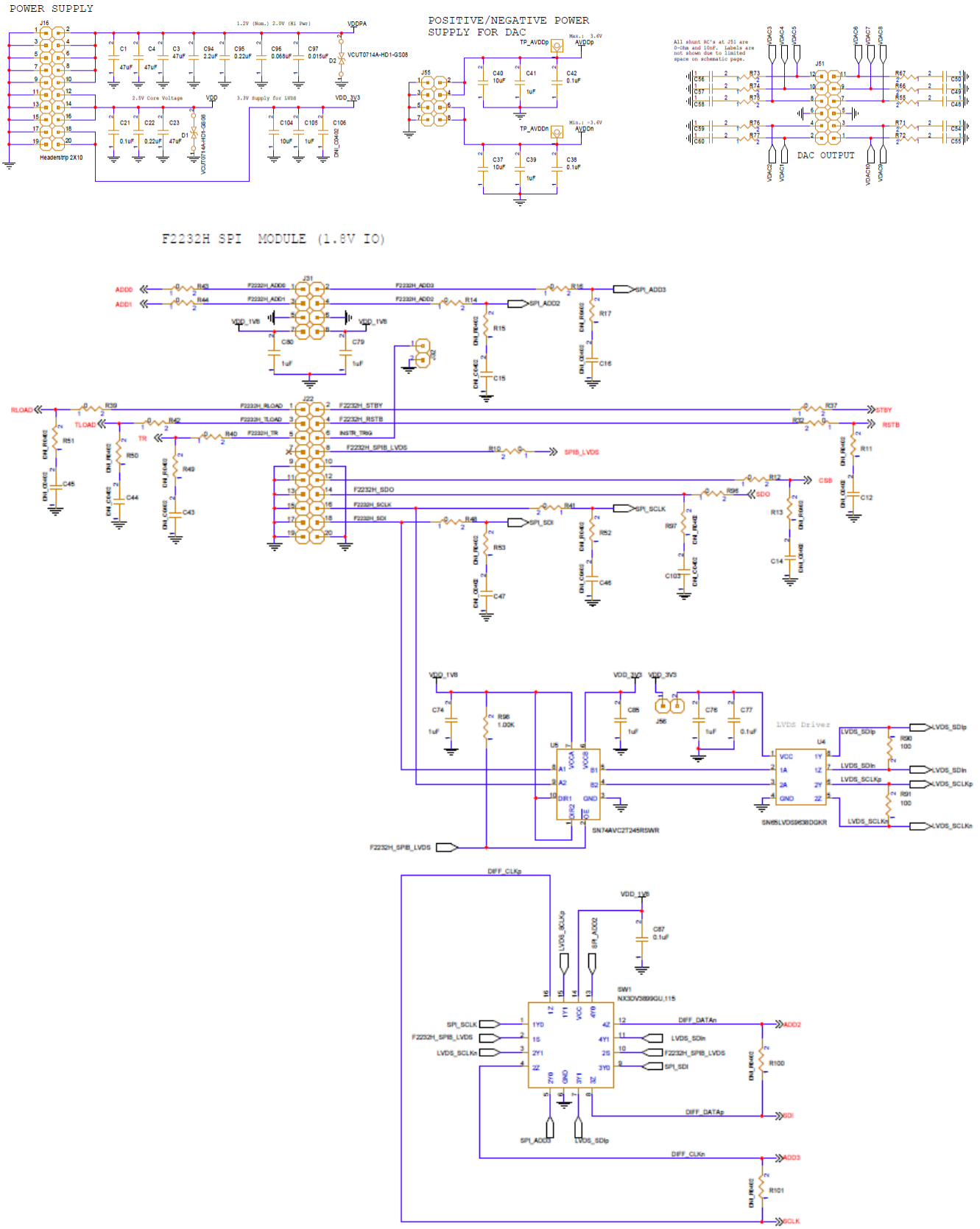


Figure 29. Evaluation Board Schematic (Part 2)

7.3 Evaluation Board Bill of Material (BOM)

Part Reference	Qty	Description	Part Number	Manufacturer
C1, C3, C4	3	X5R Surface Mount Capacitor, 47µF, 0603, 6.3V, 20%	GRM188R60J476ME15D	Murata Electronics
C2	1	COG Surface Mount Capacitor, 470pF, 0201, 25V, 5%	GRM0335C1E471J	Murata Electronics
C5	1	X5R Surface Mount Capacitor, 8200pF, 0201, 25V, 10%	GRM033R61E822K	Murata Electronics
C6, C35	2	X7R Surface Mount Capacitor, 3300pF, 0201, 25V, 10%	GRM033R71E332K	Murata Electronics
C11, C36	2	X7R Surface Mount Capacitor, 4700pF, 0201, 25V, 10%	GRM033R71E472K	Murata Electronics
C12, C14, C15, C16, C43, C44, C45, C46, C47, C61, C62, C63, C64, C93, C103, C106	16	TBD Surface Mount Capacitor, 0402	DNI_C0402	-
C21	1	X7R Surface Mount Capacitor, 0.1µF, 0603, 16V, 10%	GCM188R71C104KA37D	Murata Electronics
C22	1	X7R Surface Mount Capacitor, 0.22µF, 0603, 50V, 10%	GRM188R71H224KAC4D	Murata
C23	1	X6S Surface Mount Capacitor, 47µF, 0603, 2.5V, 20%	GRM188C80E476M	Murata Electronics
C26	1	X5R Surface Mount Capacitor, 2.2µF, 0402, 25V, 10%	GRM155R61E225K	Murata Electronics
C32, C38, C42, C67, C68, C77, C87	7	X7R Surface Mount Capacitor, 0.1µF, 0402, 16V, 10%	GRM155R71C104KA88D	Murata Electronics
C33	1	X7R Surface Mount Capacitor, 1800pF, 0201, 16V, 10%	GRM033R71C182K	Murata Electronics
C34	1	X7R Surface Mount Capacitor, 1000pF, 0201, 25V, 5%	GRM033R71E102JA01D	Murata Electronics
C37, C40, C104	3	X5R Surface Mount Capacitor, 10µF, 0402, 6.3V, 20%	GRM155R60J106M	Murata Electronics
C39, C41, C65, C66, C74, C76, C79, C80, C85, C102, C105	11	X5R Surface Mount Capacitor, 1µF, 0402, 25V, 10%	CL05A105KA5NQNC	Samsung
C48, C49, C50, C54, C55, C56, C57, C58, C59, C60	10	X7R Surface Mount Capacitor, 0.01µF, 0402, 25V, 5%	GRM155R71E103JA01D	Murata Electronics
C94	1	X5R Surface Mount Capacitor, 2.2µF, 0201, 10V, 10%	GRM033R61A225K	Murata Electronics
C95	1	X5R Surface Mount Capacitor, 0.22µF, 0201, 6.3V, 10%	CC0201KRX5R5BB	Yageo
C96	1	X6S Surface Mount Capacitor, 0.068µF, 0201, 6.3V, 10%	GRM033C80J683KE84D	Murata Electronics
C97	1	X5R Surface Mount Capacitor, 0.015µF, 0201, 50V, 10%	GRM033R61C153K	Murata Electronics
C98, C99, C100, C101	4	TBD Surface Mount Capacitor, DNI_C0201, 0201	DNI_0201	-
C107	1	X6S Surface Mount Capacitor, 0.022µF, 0201, 6.3V, 20%	GRM033C80J223ME01D	Murata Electronics
C108	1	X5R Surface Mount Capacitor, 0.047µF, 0201, 10V, 10%	GRM033R61A473K	Murata Electronics
C109	1	X5R Surface Mount Capacitor, 0.039µF, 0201, 16V, 10%	GRM033R61C393K	Murata Electronics

Part Reference	Qty	Description	Part Number	Manufacturer
D1, D2	2	Vishay: 17V, 30V Clamp 5A, 2A (8/20µs) Ipp Tvs Diode Surface Mount LLP1006-2L, VCUT0714A-HD1-GS08, SMD, 17V, 30V	VCUT0714A-HD1-GS08	Vishay
J1, J33, J34, J35, J36, J37, J38, J39, J40, J41, J42, J43, J44, J45, J46, J47, J48, J49	18	Signal Microwave: 2.92mm edge launch, Female Standard Profile, ELF40-002 F6212, EDGE_STR, 40 GHz	ELF40-002	Signal Microwave
J16, J22	2	Molex: Header Dual, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240-inch contact mating length, Header strip 2 × 10, Vertical, Male, 100mil Pitch	10-89-7200	Molex
J17, J50, J52	3	Molex: Unshrouded Header Vertical, 100mil, Header strip 2 × 3, Vertical, Male, 100mil Pitch	10-89-7062	Molex
J31, J55	2	Molex: C-Grid Header Dual, Gold, Unshrouded, Breakaway, 100mil pitch, Header strip 2 × 4, Vertical, Male, 100mil Pitch	10-89-7080	Molex
J32, J56	2	Molex: Header, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240-inch contact mating length, Header strip 1 × 2, Vertical, Male, 100mil Pitch	22-28-4023	Molex
J51	1	Molex C-Grid Header Dual, Gold, Unshrouded, Breakaway, 100mil pitch, Header strip 2 × 6, Vertical, Male, 100mil Pitch	10-89-7120	Molex
MH1	1	ATS: HEATSINK 25 × 25 × 15mm L-TAB CP Aluminum Top Mount, ATS-CPX025025015-138-C2-R0, Thru Hole, 25 × 25 × 15 mm	ATS-CPX025025015-138-C2-R0	Advanced Thermal Solutions Inc.
R1, R11, R13, R15, R17, R45, R46, R47, R49, R50, R51, R52, R53, R79, R80, R81, R82, R97, R100, R101	20	Surface Mount Resistor, 0402	DNI_R0402	
R10, R12, R14, R16, R32, R37, R39, R40, R41, R42, R43, R44, R48, R78, R83, R84, R85, R86, R87, R88, R89, R96	22	Surface Mount Resistor, 0Ω, 0402, 1/10W	ERJ-2GE0R00	Panasonic
R55, R66, R67, R71, R72, R73, R74, R75, R76, R77	10	Surface Mount Resistor, 0Ω, 0402, 1/10W	ERJ-2GE0R00X	Panasonic
R90, R91	2	Surface Mount Resistor, 100Ω, 0402, 1/16W, 1%	CRCW0402100RFK	Vishay
R98	1	Surface Mount Resistor, 1KΩ, 0402, 1/10W, 5%	ERJ-2GEJ102X	Panasonic
SO1, SO2, SO3, SO4	4	Hex Standoff Threaded M3 Nylon 0.984" (25.00mm) Natural, Standoff 25mm, Male/Female	25506	Keystone
SW1	1	2 Circuit IC Switch 2:2 3.3Ω 16-XQFN (1.8 ×2.6)	NX3DV3899GU,115	NXP
TP2, TP3	2	Phosphor Bronze Loop, Silver Plating Mini SMD	5019	Keystone
U1	1	8-Channel Dual-Polarized TRx Active Beamforming IC, 12GHz – 18GHz, BGA180	F641x	Renesas
U4	1	2/0 Driver LVDS 8-VSSOP, 3V – 3.6V	SN65LVDS9638DGKR	Texas Instruments
U5	1	Translation Transceiver 1 Element 2 Bit per Element 3-State Output 10-UQFN (1.8 × 1.4), UQFN10, 1.2V – 3.6V	SN74AVC2T245RSWR	Texas Instruments
AVDDN, AVDDP, VDD, VDDPA, VDDPA_GND, VDD_GND	6	Phosphor Bronze Wire Loop, TP_AVDDn, Thru Hole, Red	5000	Keystone

8. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

9. Marking Diagram

- Line 1: manufacturer (Renesas).
- Line 2: part number.
- Line 3:
  - $ denotes mark code.
  - Y and WW indicates the year and week of manufacture.
  - *** denotes the lot sequence.

10. Ordering Information

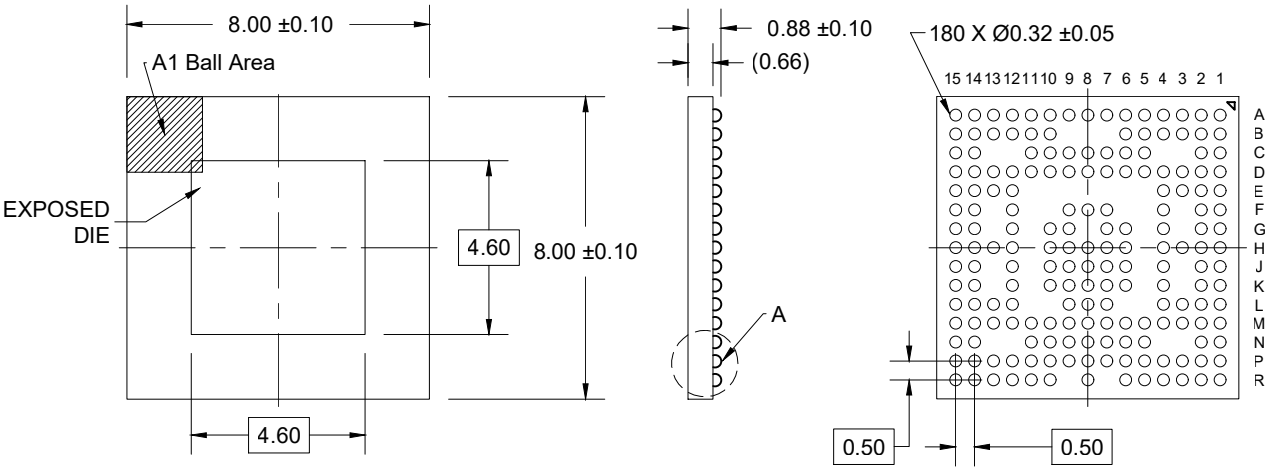
Part Number	Package Description	MSL Rating	Carrier Type	Temperature Range
RRF64130-B00	180-FCCSP, 8.00 × 8.00 × 0.88 mm	3	Tray	-40°C to +95°C
RRF64130-K00		3	Reel	
RTKRF64130-000	Evaluation Kit			

11. Revision History

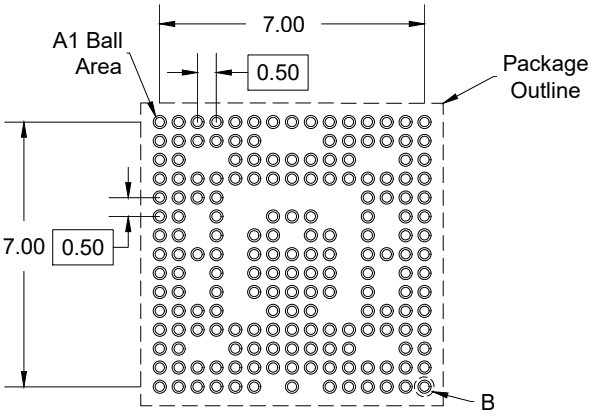
Revision	Date	Description
0.05	Jan 16, 2025	▪ Updated absolute maximum ratings for analog supplies ▪ Added recommended load conditions for VDAC outputs ▪ Updated gain control range ▪ Updated register information section ▪ Updated feature description ▪ Updated fast beam steering memory LUT diagram ▪ Updated ADD0 internal resistor type; applies to V200 variant only ▪ Updated Evaluation Board photos
0.04	Aug 9, 2024	Fixed definition for register 0x0E in section 6.15.
0.03	Jan 25, 2024	▪ Updated Pin Descriptions. ▪ Added Feature Description, Programming and Register Information sections. ▪ Added EVB image, schematics, and BOM. ▪ Added marking diagram. ▪ Updated Recommended Operating Conditions, ▪ DC Electrical Specifications, RF Electrical Specifications – Rx Mode, RF Electrical Specifications – Tx Mode
0.02	Sep 7, 2023	▪ Updated Figure 3 Pin Assignments. Replaced row “Q” with “R”. ▪ Replaced “Q” with “R” in the Pin Descriptions table. ▪ Updated Ordering Information part numbers. Added “0” after “RF6413”. ▪ Updated package height to 0.88mm from 0.9mm in two places, per the latest POD.
0.01	Jul 21, 2023	Initial release.

Package Outline Drawing

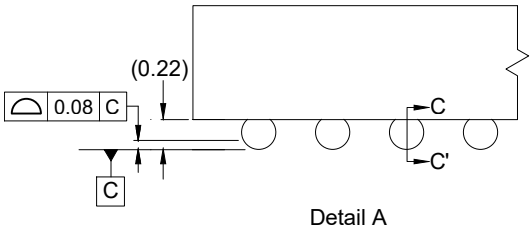
Package Code: FC0180AA
180-FCCSP (FCBGA) 8.00 x 8.00 x 0.88 mm Body, 0.50 x 0.50mm Pitch
PSC-4990-01, Revision: 00, Date Created: Sep. 1, 2023



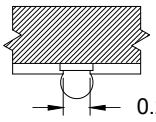
TOP VIEW SIDE VIEW BOTTOM VIEW

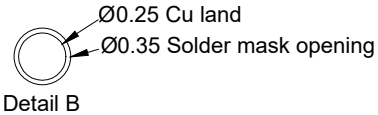


RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)



Detail A
(Rotated 90° CW)





Detail B

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Pre-reflow solderball diameter is Ø0.3 mm.

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