Description

The Renesas RapidWave RWM6050 modem IC is an IEEE 802.11ad based multi-gigabit mixed signal wireless SoC solution targeted to the wireless network infrastructure in the mmWave frequency band. The device enables highly differentiated solutions for network operators and wireless ISP vendors through a range of value added features while minimizing the overall system-level CAPEX and OPEX for the customers.

The network architects can reduce the overall system-level cost and power by leveraging RWM6050's dual-modem architecture with two channels per modem (I/Q), mixed signal PLL and VCO, on-chip network synchronization, and a high-performance PCIe interface with integrated SerDes supporting data rates up to 10Gbps per device.

The RWM6050 based wireless solution enables operators to offer better cost per GB to their consumers by leveraging advanced QoS features, range enhancement techniques, and interference mitigation functions based on flexible scheduling, channelization, wide-band signal processing (1.76GBaud per modem) and real-time radio control interface for a range of RF devices in multiple frequency bands. The device simplifies network deployment models by offering TDD-based PtP and PtMP architectures with various scheduling techniques and autonomous phased array beamforming, making this an ideal solution for roof-top access and backhaul in unlicensed 5G applications including small cell and fixed wireless access.

The RWM6050 supports both x86 and ARM architectures and comes with a well-defined software API that delivers a rich set of attributes and functionality configurable within the modem and reduces the time to market for the OEMs.

Typical Applications

- Small cell backhaul
- mmWave mesh networking and distribution network
- Fixed wireless access
- Residential broadband backhaul and aggregation
- Enterprise and smart city networking

Features

Dual Modem Support

- PHY Subsystem
  - Symbol Rate up to 1.76GBaud per modem
  - Modulation order up to 64-QAM
  - Interference mitigation through flexible channelization
  - Beamforming support with Phased Array Antenna
  - Extensions to support long-distance transmission
  - Mixed Signal Front End with integrated converters
  - IEEE 802.11ad single carrier PHY
- MAC Subsystem
  - Flexible real-time scheduler
  - Secured networking based on AES-GCM
  - IEEE 1588v2 transparent clock support

Interfaces

- PCI Express Gen2
- Flash SPI
- I^2C/SPI/UART
- GPIO
- JTAG
- Analog Front End: integrated DACs and ADCs

For a complete list of device features, see Main Features.

Block Diagram

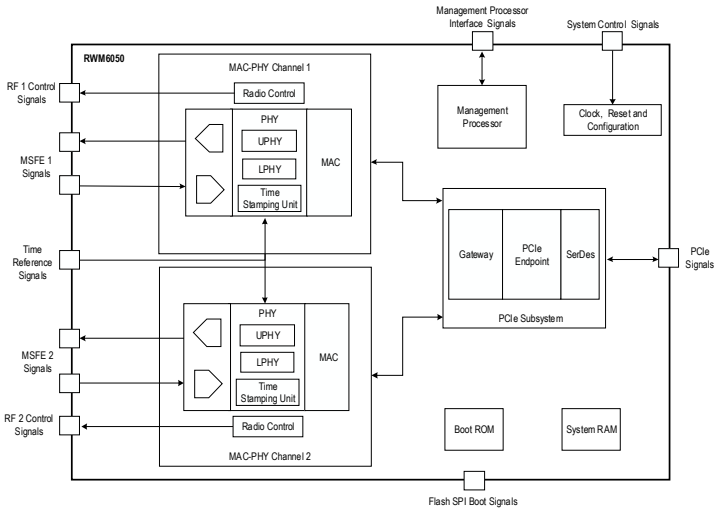


Table of Contents

1. Functional Overview 6
- 1.1 Block Diagram 6
- 1.2 Main Features 7
  - 1.2.1 Dual PHY Subsystems 7
  - 1.2.2 Dual MAC Subsystems 8
  - 1.2.3 Interfaces 8
  - 1.2.4 Mixed Signal Front End 8
- 1.3 MAC PHY Channel Architecture 8
- 1.4 Typical Applications 9

2. Pin Assignments 10
- 2.1 Pin Descriptions 11
  - 2.1.1 Functional Signals 11
  - 2.1.2 Supply Signals 19
  - 2.1.3 Ground Signals 21
  - 2.1.4 Do Not Connect Signals 21

3. Electrical Specifications 22
- 3.1 Absolute Maximum Ratings 22
- 3.2 Recommended Operating Conditions 23
- 3.3 Supply Currents and Power 24
- 3.4 Power Supply Sequencing 24
  - 3.4.1 Ramp-up Time 24
  - 3.4.2 Power-up Sequencing 24
  - 3.4.3 Power-down Sequencing 25
- 3.5 DC Electrical Characteristics 25
  - 3.5.1 LVCMOS I/Os 25
  - 3.5.2 LVDS I/O 26
- 3.6 LVCMOS and LVDS I/O AC Specifications 26
  - 3.6.1 AC Timing Test Conditions 26
  - 3.6.2 Reference Clock Timing Specification 27
  - 3.6.3 Reset Signal Timing Specifications 28
  - 3.6.4 JTAG Signal Timing Specifications 29
  - 3.6.5 Radio Control Interface Signal Timing Specifications 30
  - 3.6.6 Flash SPI (FSPI) Boot Interface Signal Timing Specifications 33
  - 3.6.7 System SPI Interface Signal Timing Specifications 34
  - 3.6.8 I^2C Interface Signal Timing Specifications 35
- 3.7 Mixed Signal Front End Interface Characteristics 36
  - 3.7.1 MSFE ADC Specifications 36
  - 3.7.2 MSFE DAC Specifications 38
  - 3.7.3 MSFE Reference Clock 39
- 3.8 PCIe Interface Characteristics 41
  - 3.8.1 PCIe Reference Clock 41
  - 3.8.2 PCIe Differential Receiver and Transmitter Specifications 42

4. System Clocking 45
- 4.1 System Oscillator 45
- 4.2 System PLLs 45
- 4.3 PHY Clocks 45

5. Package Specifications 47
- 5.1 Package Information 47
- 5.2 Package Outline Drawings 47
- 5.3 Thermal Characteristics 47

6. Marking Diagram 49
7. Ordering Information 49
8. Partner Acknowledgment 49
Revision History 50

List of Figures

Figure 1. RWM6050 Block Diagram 6
Figure 2. Dual RWM6050 Wireless Node – N-E-S-W Configuration 9
Figure 3. Pin Assignments – Top View 10
Figure 4. Circuit for the System XTAL 27
Figure 5. Single-ended System Reference Clock 28
Figure 6. JTAG Signal Timing Diagram 29
Figure 7. RCI LVCMOS AC Timing Diagram 30
Figure 8. RCI LVDS AC Timing Diagram 31
Figure 9. RCIx_GPIO_n, n = 2:6, AC Timing Diagram – SDR Operation 32
Figure 10. RCIx_GPIO_n, n = 2:6, AC Timing Diagram – DDR Operation 32
Figure 11. FSPI AC Timing Diagram 33
Figure 12. System SPI AC Timing Diagram 34
Figure 13. I^2C AC Timing Diagram 36
Figure 14. Differential MSFE Reference Clock with AC Coupling – An Example 39
Figure 15. Single-ended MSFE Reference Clock Coupling 40
Figure 16. Circuit for the MSFE XTAL 40
Figure 17. PHY Clocks – RWM6050 Master, RF Slave 45
Figure 18. PHY Clocks – RF Master, RWM6050 Slave 46
Figure 19. PHY Clocks – RWM6050 and RF Slave 46

List of Tables

Table 1. Signal Function Key 11
Table 2. System Control Signals 11
Table 3. PCIe Interface Signals 12
Table 5. Radio Control Interface (RCI) Signals 13
Table 4. Auxiliary Signals 13
Table 6. Flash SPI Boot Interface Signals 15
Table 7. Management Processor Interface Signals 16
Table 8. MSFE Signals 18
Table 10. Power Supply and Reference Signals 19
Table 9. JTAG/Test Signals 19
Table 11. Ground Signals 21
Table 12. DNC Signals 21
Table 13. Absolute Maximum Ratings 22
Table 14. Recommended Operating Conditions 23
Table 15. Supply Currents and Power 24
Table 16. 1.8V LVCMOS I/O DC Parameters 25
Table 17. LVDS I/O DC Parameters 26
Table 18. LVCMOS AC Test Conditions for VDDIO = 1.8V 26
Table 19. LVDS AC Test Conditions for LVDS_VDDIO = 1.8V 26
Table 20. Recommended Values for System XTAL Oscillator 27
Table 21. Reference Clock Specification 28
Table 22. Reset Signal Timing Specifications 28
Table 23. JTAG Signal Timing Specifications 29
Table 24. RCI LVCMOS AC Timing Parameters 30
Table 25. RCI LVDS AC Timing Parameters 31
Table 27. RCIx_GPIO_n, n = 2:6, AC Timing Parameters – DDR Operation 32
Table 26. RCIx_GPIO_n, n = 2:6, AC Timing Parameters – SDR Operation 32
Table 28. FSPI Interface AC Timing Parameters 33
Table 29. System SPI Interface AC Timing Parameters 34
Table 30. I^2C Interface Signal Timing Specifications 35
Table 31. ADC Characteristics 36
Table 32. ADC Full-scale Input Configuration 37
Table 33. IQ DAC Characteristics 38
Table 34. MSFE Reference Clock Specifications 39
Table 35. Recommended Values for Single-ended MSFE Reference Clock Coupling 40
Table 36. Recommended Values for MSFE XTAL Oscillator 40
Table 37. PCIe PCIE_CLKP/PCIE_CLKN Requirements 41
Table 38. PCIe Differential Receiver Specifications 42
Table 39. PCIe Differential Transmitter Specifications 43
Table 40. Package Information 47
Table 41. Junction to Board/Case Thermal Characteristics (Theta JB/JC) 47
Table 42. Junction to Ambient Thermal Characteristics (Theta JA) 48
Table 43. With External Heat Sink 48

1. Functional Overview

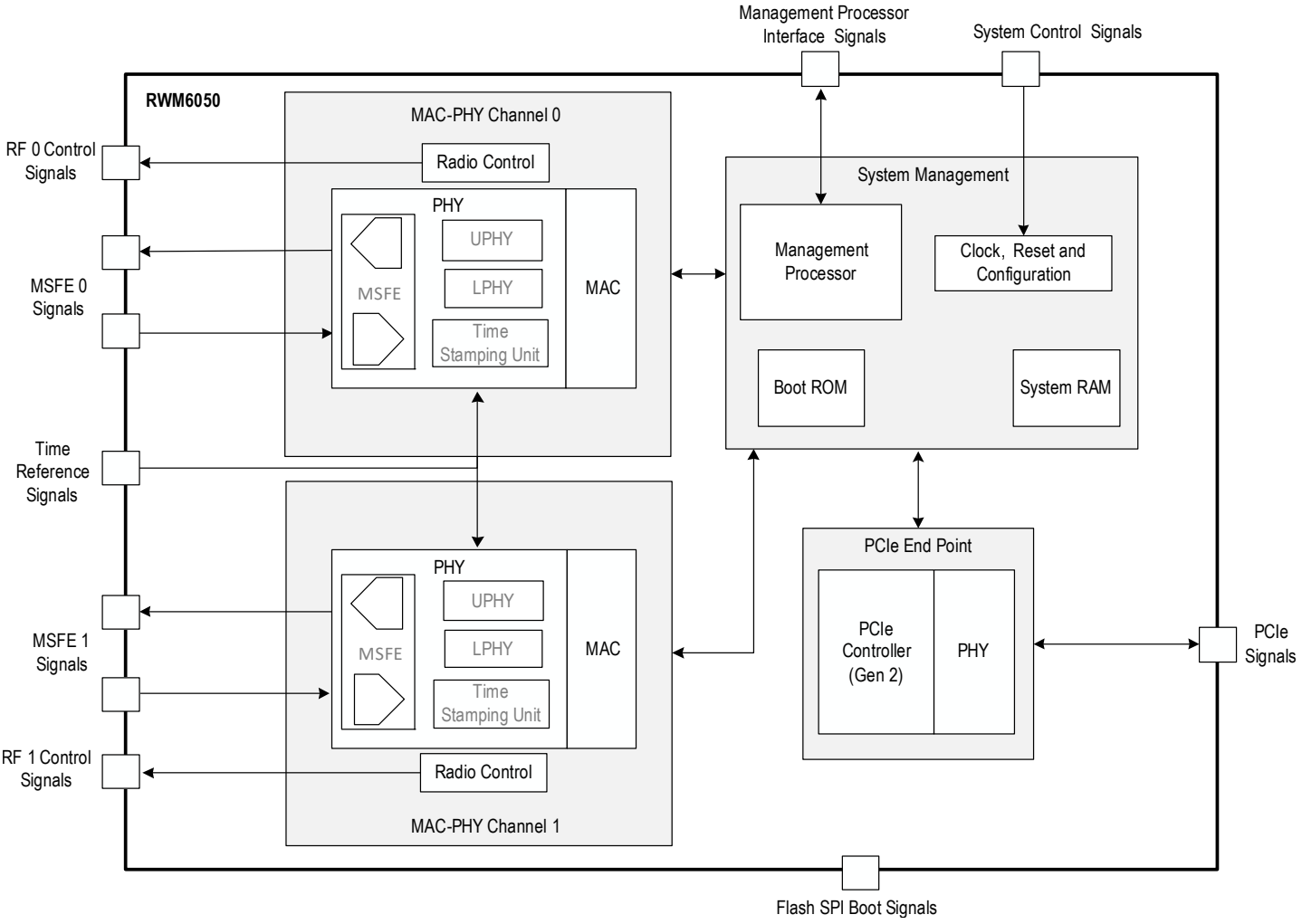
1.1 Block Diagram

A high-level block diagram of the RWM6050 is shown in Figure 1. The device supports two independent MAC PHY channels that can each process wireless signal with up to 2.16GHz channel bandwidth, and interfaces with an external host CPU over the common PCIe subsystem that can support data rates up to 10GBaud (2 lanes, 5Gbaud/lane).

Each MAC PHY channel is comprised of the following functional blocks:

- Physical Layer processor (PHY), containing a mixed signal front-end (MSFE), Lower PHY (LPHY), and Upper PHY (UPHY) processing functions
- MAC processor (MAC), containing upper and lower MACs and a set of hardware off-load engines
- Radio control interface (RCI), containing radio control and management functions for phased array RF transceivers

Figure 1. RWM6050 Block Diagram



In addition to the MAC PHY channels, the RWM6050 contains the following system functions:

- High-speed PCIe Gen2 endpoint for connection to an appropriate host
- One supervisory RISC processor
- Common system RAM
- Primary Boot ROM
- System interfaces such as I2C, SPI, UART, and JTAG
- PLLs for clock generation
- System peripherals such as system timers, a real-time clock, and a watchdog supervisor

1.2 Main Features

1.2.1 Dual PHY Subsystems

1.2.1.1 Firmware Supporting

- 802.11ad MCS 0 (π/2 DBPSK)
- 802.11ad MCS 1–5 (π/2 BPSK)
- 802.11ad MCS 6–9 (π/2 QPSK)
- 802.11ad MCS 10–12 (π/2 16-QAM)
- Extended MCS 12 (π/2 64-QAM)
- Optimized PHY for long range transmission

1.2.1.2 Lower PHY

- Digital Signal processing
  - Radio artifact compensation:
    - DC offset
    - IQ imbalance
    - Time and frequency synchronization
    - Receiver automatic gain control (AGC)
  - Programmable digital channel bandwidth:
    - Full band
    - Half-band
    - Quarter-band
  - Programmable digital intermediate frequency (IF) within baseband channel in half-band and quarter-band modes
  - IQ data egress pulse shaping and ingress matched filtering
  - Channel estimation
- Radio interface control
- Time stamping unit

1.2.1.3 Upper PHY

- Vector Processing Elements
- FFT/IFFT units: 512 points
- Single Carrier Frequency Domain Equalization (SC-FDE)
- LDPC encode/decode unit: Configurable maximum number of decoding iterations

1.2.2 Dual MAC Subsystems

- Flexible data plane and real-time scheduler
  - Encryption based on AES-GCM
  - CBAP and SP scheduling
- Network Synchronization using IEEE 1588v2 transparent clock

1.2.3 Interfaces

- *PCI Express Base Specification (Revision 2.1)*
  - Two lanes
  - 5 or 2.5 GT/s per lane
  - 256-byte maximum payload size
  - Two physical functions
- SPI Flash Interface
  - Boot from SPI NOR Flash
  - Single, Dual, Quad I/O modes up to 50MHz
- UART with flow control
- JTAG
- General purpose I/Os
- Multi-vendor radio control interface

1.2.4 Mixed Signal Front End

- IQ DACs and IQ ADCs
  - 7-bit DAC and 7-bit ADC
  - ENOB: 6-bit
  - Sampling Clock: 3.52, 1.76, or 0.880 GHz
- Differential IQ signaling
- 3.52 GHz PLL
  - Jitter < 1.0ps
  - Typical reference: 45MHz

1.3 MAC PHY Channel Architecture

The PHY Channel is a heterogeneous multiprocessing technology. It uses multiple levels of parallelism and pipelining with an optimum mixture of programmable and fixed function units. This architecture allows a conventional software model to control the PHY processing resources in an optimally efficient way, while providing a “Region of Programmability” to cover the various modulation and coding schemes. The PHY differs from a conventional wireless processor pipeline design because it has a scalable multiprocessor arrangement in the PHY section. The design and operating model of the cluster of Physical Processing Units (PPUs) enables the very intensive DSP load required for the modulation and coding of multi-gigabit data rates to be controlled by a conventional embedded software model.

The MAC function is similarly comprised of a hardware/software processing scheme with all data path and latency critical functions implemented in hardware. Other functions run as software on an array of embedded RISC processors. This hybrid of software and hardware enables the use of a wide range of MAC protocol and frame formats, including 802.11ad compatible schemes.

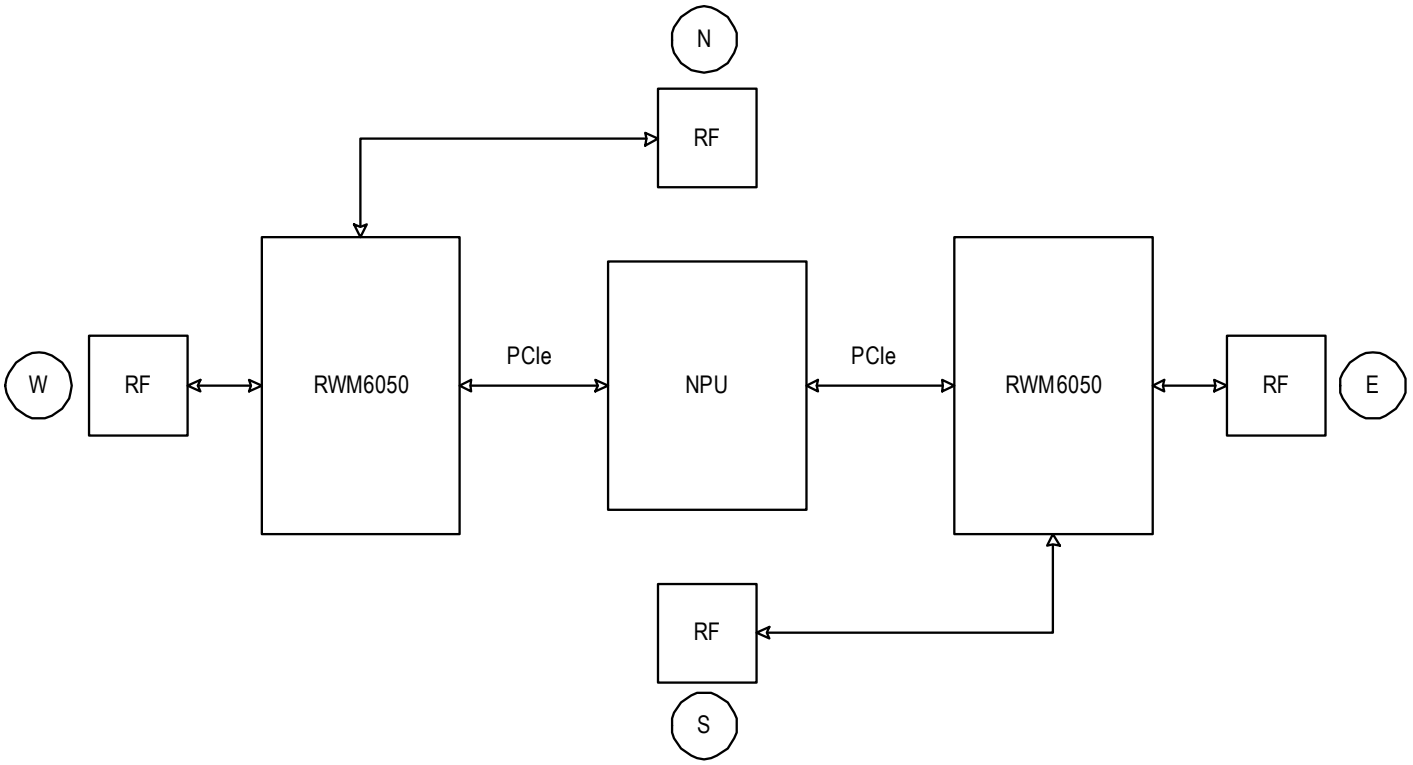
1.4 Typical Applications

Typical applications for the RWM6050 include the following:

- Small cell backhaul
- mmWave mesh networking and distribution network
- Fixed wireless access
- Residential broadband backhaul and aggregation
- Enterprise and smart city networking

Figure 2 shows a backhaul wireless node using two RWM6050 devices in a North/East/South/West (N-E-S-W) configuration. Each RWM6050 can support two 90° sectors simultaneously. The RWM6050 connects to a local NPU Processor via PCIe to provide bridge/switch capabilities between the MACs. This dual TDD PHY/MAC modem supports 360° azimuth coverage with four mmWave RF/Antenna arrays.

Figure 2. Dual RWM6050 Wireless Node – N-E-S-W Configuration



2. Pin Assignments

Figure 3. Pin Assignments – Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	VSSIO	SPI_CSN	DNC	A4	A5	DNC	DNC	PCIE_CLKP	PCIE_TX0_N	PCIE_RX0_N	PCIE_RX0_P	PCIE_TX1_N	PCIE_RX1_N	PCIE_PERSTN	VSS	SYSOSC_XO	SYSOSC_XI	RESET_N	PWM_0	I2C_SCL	I2C_SDA	VSSIO	A
B	SPI_SCLK	SPI_MISO	A2	A3	VSS	A6	VSS	PCIE_CLKN	VSS	PCIE_TX0_P	VSS	PCIE_TX1_P	VSS	PCIE_RX1_P	PCIE_WAKEN	REFCLK_TSYNC0	REFCLK_TSYNC1	VSSIO	PWM_1	JTAG_TDO	JTAG_TCK	RESET_OUT	B
C	SPI_MOSI	GPIO_0	A1	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	PCIE_CLKREQN	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	JTAG_TDI	JTAG_TMS	MODE0	C
D	GPIO_1	GPIO_2	VDDIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	PLL1_VDDH	VSSIO	VSSIO	PLL0_VDDH	VSSIO	VDDIO	JTAG_SELECT	JTAG_TRSTN	MODE1	D
E	GPIO_3	GPIO_4	GPIO_5	VSS	VSSIO	A7	VSS	DNC	VSS	PCIE_VPH	VSS	PCIE_RBIAS	VSS	PLL1_VDDA	PLL1_AVSS	PLL0_AVSS	PLL0_VDDA	RCI0_CSN7_S	VSSIO	DEBUG_TCK	FSPI_CLK	FSPI_CSN	E
F	GPIO_6	GPIO_7	GPIO_8	VSSIO	VSSIO	VSSIO	DNC	VSS	DNC	VSS	PCIE_VPTX	VSS	PCIE_VP	PLL1_DVDD	PLL1_DVSS	PLL0_DVSS	PLL0_DVDD	RCI0_CSN6_S	VDDIO	VSSIO	FSPI_D0	FSP1_D1_DO	F
G	GPIO_9	GPIO_10	VSSIO	VSSIO	VSSIO	TSENSE_AVDDH	TSENSE_AVSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	VSSIO	VDD	VSSIO	RCI0_CSN5_S	RCI0_CSN4_S	DEBUG_TDO	FSPI_D2_WPN	FSPI_D3_HN	G
H	GPIO_11	GPIO_12	VDDIO	VSSIO	VSSIO	VSSIO	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	RCI0_CSN3_S	VSSIO	DEBUG_TDI	UART_RTS	UART_RX	H
J	GPIO_13	GPIO_14	GPIO_15	RCI1_CSN6_S	RCI1_CSN7_S	VDDIO	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	RCI0_CSN2_S	RCI0_MISO7_S	DEBUG_TMS	UART_CTS	UART_TX	J
K	RCI1_GPIO0	RCI1_GPIO1	RCI1_GPIO2	RCI1_CSN4_S	RCI1_CSN5_S	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSSIO	VSSIO	DEBUG_TRSTN	RCI0_GPIO1	RCI0_GPIO0	K
L	RCI1_GPIO3	RCI1_GPIO4	RCI1_GPIO5	RCI1_CSN2_S	RCI1_CSN3_S	VDDIO	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	RCI0_GPIO5	RCI0_GPIO4	RCI0_GPIO3	RCI0_GPIO2	L
M	RCI1_CSN0_N	RCI1_CSN0_P	LVDS_VDDIO	VSSIO	RCI1_MISO7_S	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	LVDS_VDDIO	VSSIO	RCI0_CSN0_P	RCI0_CSN0_N	M
N	RCI1_SCLK_N	RCI1_SCLK_P	RCI1_GPIO6	RCI1_GPIO7	RCI1_GPIO8	VDDIO	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	RCI0_GPIO8	RCI0_GPIO7	RCI0_GPIO6	RCI0_SCLK_P	RCI0_SCLK_N	N
P	RCI1_MOSI0_N	RCI1_MOSI0_P	VSSIO	LVDS_VDDIO	RCI1_GPIO9	VSSIO	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	RCI0_GPIO9	LVDS_VDDIO	VSSIO	RCI0_MOSI0_P	RCI0_MOSI0_N	P
R	RCI1_MOSI1_N	RCI1_MOSI1_P	RCI1_REF	RCI1_SCLK_S	RCI1_CSN0_S	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	RCI0_CSN0_S	RCI0_SCLK_S	RCI0_REF	RCI0_MOSI1_P	RCI0_MOSI1_N	R
T	RCI1_MOSI2_N	RCI1_MOSI2_P	RCI1_MISO0_S	RCI1_MISO1_S	RCI1_VDDIO	MSFE1_AVSS	MSFE1_PLL_AVDD	MSFE1_AVSS	MSFE1_OSC_AVDDH	MSFE1_AVSS	MSFE1_AVDD	MSFE0_AVDD	MSFE0_AVSS	MSFE0_OSC_AVDDH	MSFE0_AVSS	MSFE0_PLL_AVDD	MSFE0_AVSS	VSSIO	RCI0_MISO1_S	RCI0_MISO0_S	RCI0_MOSI2_P	RCI0_MOSI2_N	T
U	RCI1_MOSI3_N	RCI1_MOSI3_P	RCI1_MOSI0_S	RCI1_MOSI1_S	VSSIO	MSFE1_AVDDH	MSFE1_AVSS	MSFE1_PLL_AVDDH	MSFE1_AVSS	MSFE1_AVDD	MSFE1_AVSS	MSFE0_AVSS	MSFE0_AVDD	MSFE0_AVSS	MSFE0_PLL_AVDDH	MSFE0_AVSS	MSFE0_AVDDH	RCI0_VDDIO	RCI0_MOSI1_S	RCI0_MOSI0_S	RCI0_MOSI3_P	RCI0_MOSI3_N	U
V	RCI1_CSN1_N	RCI1_CSN1_P	RCI1_MOSI2_S	RCI1_MOSI3_S	RCI1_CSN1_S	MSFE1_AVSS	MSFE1_AVDDH	MSFE1_AVSS	MSFE1_AVDD	MSFE1_AVSS	MSFE1_AVSS	MSFE0_AVSS	MSFE0_AVSS	MSFE0_AVDD	MSFE0_AVSS	MSFE0_AVDDH	MSFE0_AVSS	RCI0_CSN1_S	RCI0_MOSI3_S	RCI0_MOSI2_S	RCI0_CSN1_P	RCI0_CSN1_N	V
W	VSSIO	LVDS_VDDIO	VSSIO	VDDIO	MSFE1_AVSS	MSFE1_AVDDH	MSFE1_AVSS	MSFE1_AVDDH	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE0_AVSS	MSFE0_AVSS	MSFE0_AVSS	MSFE0_AVDDH	MSFE0_AVSS	MSFE0_AVDDH	MSFE0_AVSS	VDDIO	VSSIO	LVDS_VDDIO	VSSIO	W
Y	MSFE1_ADC_IN	MSFE1_AVSS	RCI1_MISO6_S	RCI1_MISO5_S	RCI1_MISO4_S	RCI1_MISO3_S	RCI1_MISO2_S	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE0_AVSS	MSFE0_AVSS	MSFE0_AVSS	MSFE0_AVSS	RCI0_MISO2_S	RCI0_MISO3_S	RCI0_MISO4_S	RCI0_MISO5_S	RCI0_MISO6_S	MSFE0_AVSS	MSFE0_ADC_IN	Y
AA	MSFE1_ADC_IP	MSFE1_ADC_VCM	MSFE1_AVSS	MSFE1_CLKOUT	MSFE1_AVSS	MSFE1_AVSS	DNC	DNC	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE0_AVSS	MSFE0_AVSS	MSFE0_AVSS	DNC	DNC	MSFE0_AVSS	MSFE0_AVSS	MSFE0_CLKOUT	MSFE0_AVSS	MSFE0_ADC_VCM	MSFE0_ADC_IP	AA
AB	MSFE1_AVSS	MSFE1_ADC_QN	MSFE1_ADC_QP	MSFE1_REFCLKN	MSFE1_REFCLKP	MSFE1_XO	MSFE1_XI	MSFE1_DAC_QN	MSFE1_DAC_QP	MSFE1_DAC_IN	MSFE1_DAC_IP	MSFE0_DAC_IP	MSFE0_DAC_IN	MSFE0_DAC_QP	MSFE0_DAC_QN	MSFE0_XI	MSFE0_XO	MSFE0_REFCLKP	MSFE0_REFCLKN	MSFE0_ADC_QP	MSFE0_ADC_QN	MSFE0_AVSS	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

2.1 Pin Descriptions

2.1.1 Functional Signals

Table 1. Signal Function Key

Symbol	Meaning
I	LVCMOS input
O	LVCMOS output
IO	LVCMOS input/output
LVDS_I	LVDS input
LVDS_O	LVDS output
CML_I	CML input
A	Analog
PU	Weak pull-up
PD	Weak pull-down
OD	Open-drain output
ST	Schmitt trigger input

Table 2. System Control Signals

Signal Name	Ball	Type		Voltage	Description
RESET_N	A18	I	ST-PU	1.8	Active-low asynchronous system reset input. This pin is a Schmitt trigger input with an internal pull-up.
RESET_OUT	B22	O	-	1.8	Reset indication output. This signal is high when the RWM6050 is being reset.
SYSOSC_XI	A17	I	-	1.8	Crystal Connection input. Accepts a 25MHz reference from a clock oscillator or a resonant crystal.
SYSOSC_XO	A16	O	-	1.8	Crystal Connection output. This pin should be connected to a crystal. If a clock oscillator is connected to SYSOSC_XI, then this pin must be left unconnected.
MODE0	C22	I	PD	1.8	Boot configuration inputs. The RWM6050 boot mode is determined by the state of the pins as follows: ▪ 00: – Primary boot: From the internal Boot ROM – Secondary boot: From FSPI interface. The Flash memory must have valid RWM6050 code. ▪ 01: Reserved. ▪ 10: Reserved. ▪ 11: Reserved. These pins are static inputs and must be set to the required state when the RESET_N is asserted low.
MODE1	D22	I	PD	1.8	

Table 2. System Control Signals (Cont.)

Signal Name	Ball	Type		Voltage	Description
REFCLK_TSYNC0	B16	I	-	1.8	External timing reference input for use with IEEE1588v2. ▪ REFCLK_TSYNC0: This signal provides the reference clock for the RWM6050 time-stamping unit. The required frequency of this signal is nominally 100MHz. *Note*: If this functionality is not being used then pull to ground using a 49.9Ω resistor. ▪ REFCLK_TSYNC1: This signal carries the pulse-per-second (PPS) signal. It is required to pulse high every fixed period to provide physical representation of time. *Note*: If this functionality is not being used then pull to ground using a 49.9Ω resistor.
REFCLK_TSYNC1	B17	I	-	1.8	
DEBUG_TCK	E20	I	ST-PD	1.8	Internal use only; do not connect.
DEBUG_TDI	H20	I	ST-PU	1.8	
DEBUG_TDO	G20	O	OD	1.8	
DEBUG_TMS	J20	I	ST-PU	1.8	
DEBUG_TRSTN	K20	I	ST-PD	1.8	

Table 3. PCIe Interface Signals

Signal Name	Ball	Type		Voltage	Description
PCIE_CLKN	B8	LVDS_I	-	1.8	PCIe differential reference clock. The required nominal PCIE_CLKP/PCIE_CLKN frequency is 100MHz.
PCIE_CLKP	A8		-	1.8	
PCIE_RX0_N	A10	LVDS_I	-	1.8	PCIe differential receive inputs – Receive Lane 0
PCIE_RX0_P	A11		-	1.8	
PCIE_RX1_N	A13	LVDS_I	-	1.8	PCIe differential receive inputs – Receive Lane 1
PCIE_RX1_P	B14		-	1.8	
PCIE_TX0_N	A9	LVDS_O	-	1.8	PCIe differential transmit outputs – Transmit Lane 0
PCIE_TX0_P	B10		-	1.8	
PCIE_TX1_N	A12	LVDS_O	-	1.8	PCIe differential transmit outputs – Transmit lane 1
PCIE_TX1_P	B12		-	1.8	
PCIE_CLKREQN	C13	IO	ST	1.8	PCIe reference clock request signal. This active-low signal has a Schmitt trigger input.
PCIE_PERSTN	A14	I	ST-PU	1.8	PCIe functional reset input.
PCIE_WAKEN	B15	IO	ST	1.8	PCIe wake request. This active-low signal has a Schmitt trigger input.
PCIE_RBIAS	E12	A	-	1.8	External reference resistor connection pin. Attach a 200 ±1% Ohm resistor to ground with a temperature coefficient of resistance α of 1% over 100°C. The external resistor is automatically used for calibration when the RWM6050 comes out of reset.

Table 4. Auxiliary Signals

Signal Name	Ball	Type		Voltage	Description
A1	C3	I	PD	1.8	Internal use only, do not connect.
A2	B3	IO	-	1.8	
A3	B4	LVDS_I	-	1.8	
A4	A4		-	1.8	
A5	A5	LVDS_I	-	1.8	
A6	B6		-	1.8	
A7	E6	A	-	1.8	

Table 5. Radio Control Interface (RCI) Signals

Signal Name[a]	Ball	Type		Voltage	Description
RCIx_SCLK_N	N22, N1	LVDS_O	-	1.8	Differential clock output for RF management interface. When the Radio Control Interface is configured to operate in QPSI-Like mode, the RCIx_SCLK_N/P is a free running signal with a configurable frequency of up to 200MHz.
RCIx_SCLK_P	N21, N2		-	1.8	
RCIx_CSN0_N	M22, M1	LVDS_O	-	1.8	Differential chip select 0 output for RF management interface. When enabled, this signal is asserted low to initiate a management transaction to the connecting RF device.
RCIx_CSN0_P	M21, M2		-	1.8	
RCIx_CSN1_N	V22, V1	LVDS_O	-	1.8	Differential chip select 1 output for RF management interface. When enabled, this signal is asserted low to initiate a management transaction to the connecting RF device.
RCIx_CSN1_P	V21, V2		-	1.8	
RCIx_MOSI0_N	P22, P1	LVDS_O	-	1.8	Differential data output for RF management interface – Bit 0.
RCIx_MOSI0_P	P21, P2		-	1.8	
RCIx_MOSI1_N	R22, R1	LVDS_O	-	1.8	Differential data output for RF management interface – Bit 1.
RCIx_MOSI1_P	R21, R2		-	1.8	
RCIx_MOSI2_N	T22, T1	LVDS_O	-	1.8	Differential data output for RF management interface – Bit 2.
RCIx_MOSI2_P	T21, T2		-	1.8	
RCIx_MOSI3_N	U22, U1	LVDS_O	-	1.8	Differential data output for RF management interface – Bit 3.
RCIx_MOSI3_P	U21, U2		-	1.8	
RCIx_SCLK_S	R19, R4	O	-	1.8	RCIx Single-ended full swing clock output for RF management interface. When the Radio Control Interface is configured to operate in QSPI/SPI mode, the RCIx_SCLK_S runs when the RCIx_CSNx_S is asserted low. The frequency of RCIx_SCLK_S is tunable from 31.42 to 73.33MHz.

Table 5. Radio Control Interface (RCI) Signals (Cont.)

Signal Name[a]	Ball	Type		Voltage	Description
RCIx_CSN*n*_S	R18, R5 V18, V5 J18, L4 H18, L5 G19, K4 G18, K5 F18, J4 E18, J5	PU	-	1.8	RCIx single-ended full swing chip select *n* output for RF management interface. Fist row lists balls of RCI0, second row lists balls of RCI1. When enabled, this signal is asserted low to initiate a management transaction to the connecting RF device.
RCIx_MOSI0_S	U20, U3	O	-	1.8	RCIx single-ended full swing data output for the RF management interface – Bit 0.
RCIx_MOSI1_S	U19, U4	O	-	1.8	RCIx single-ended full swing data output for the RF management interface. Data out, Bit 1, when the interface is configured to operate in quad configuration.
RCIx_MOSI2_S	V20, V3	O	-	1.8	RCIx single-ended full swing data output for the RF management interface. Data out, Bit 2, when the interface is configured to operate in quad configuration.
RCIx_MOSI3_S	V19, V4	O	-	1.8	RCIx single-ended full swing data output for the RF management interface. Data out, Bit 3, when the interface is configured to operate in quad configuration.
RCIx_MISO*n*_S	T20, T3, T19, T4, Y16, Y7 Y17, Y6 Y18, Y5 Y19, Y4 Y20, Y3 J19, M5	I	PD	1.8	RCIx single-ended full swing data input for the RF management interface corresponding to chip select n. This signal carries the read data from the connecting RF device in both QPSI/SPI and QPSI-Like modes.
RCIx_GPIO0	K22, K1	IO	-	1.8	RCIx general purpose and timed I/O for the RF management interface.
RCIx_GPIO1	K21, K2	IO	-	1.8	
RCIx_GPIO2	L22, K3	IO	-	1.8	
RCIx_GPIO3	L21, L1	IO	-	1.8	
RCIx_GPIO4	L20, L2	IO	-	1.8	
RCIx_GPIO5	L19, L3	IO	-	1.8	
RCIx_GPIO6	N20, N3	IO	-	1.8	
RCIx_GPIO7	N19, N4	IO	-	1.8	
RCIx_GPIO8	N18, N5	IO	-	1.8	
RCIx_GPIO9	P18, P5	IO	-	1.8	

[a] RCIx implies both RCI0 and RCI1 interfaces, which are identical; ball names correspond to RCI0 and RCI1 in that order. RCI0 and RCI1 interfaces can be configured independently

Table 6. Flash SPI Boot Interface Signals

Signal Name	Ball	Type		Voltage	Description
FSPI_CLK	E21	O	-	1.8	Flash SPI clock output with a configurable frequency of up to 50MHz. This signal is tri-stated during device reset.
FSPI_CSN	E22	O	-	1.8	Flash SPI chip select. This signal is asserted low to initiate a transaction. This signal is tri-stated during device reset.
FSPI_D0	F21	IO	-	1.8	Flash SPI – data in, Bit 0. This signal carries data in bit 0. It can also be configured as a GPIO with direction and values controlled by registers. This signal is tri-stated during device reset.
FSPI_D1_DO	F22	IO	-	1.8	Flash SPI – data in, Bit 1. This signal carries: ▪ Data in, Bit 1, when the interface is configured to operate in dual or quad configuration, or ▪ Data out serial data This signal can also be configured as a GPIO with direction and values controlled by registers. This signal is tri-stated during device reset.
FSPI_D2_WPN	G21	IO	-	1.8	Flash SPI – data in, Bit 2. This signal: ▪ Carries data in, Bit 2, when the interface is configured to operate in quad configuration ▪ Drives the flash active-low Write-Protect signal This signal can also be configured as a GPIO with direction and values controlled by registers. This signal is tri-stated during device reset.
FSPI_D3_HN	G22	IO	-	1.8	Flash SPI – data in, Bit 3. This signal carries: ▪ Data in, Bit 3, when the interface is configured to operate in quad configuration, or ▪ Drives the flash active-low Hold signal This signal can also be configured as a GPIO with direction and values controlled by registers. This signal is tri-stated during device reset.

Table 7. Management Processor Interface Signals

Signal Name	Ball	Type		Voltage	Description
SPI Interface					
SPI_SCLK	B1	O	-	1.8	Management processor SPI clock output signal with a configurable frequency of up to 62.5MHz.
SPI_CSN	A2	O	-	1.8	Management processor SPI Chip Select. This signal is asserted low to initiate a transaction.
SPI_MISO	B2	I	PD	1.8	Management processor SPI Master In Slave Output Data.
SPI_MOSI	C1	O	-	1.8	Management processor SPI Master Out Slave In Data.
UART Interface					
UART_RX	H22	I	PD	1.8	Management processor UART serial data receive.
UART_TX	J22	O	-	1.8	Management processor UART serial data transmit.
UART_CTS	J21	I	PU	1.8	Management processor UART Clear-To-Send flow control signal.
UART_RTS	H21	O	-	1.8	Management processor UART Request-to-Send flow control signal.
I2C Interface					
I2C_SCL	A20	IO	ST-PU	1.8	Management processor I^2C serial clock with a maximum frequency of 400kHz. This signal has a Schmitt trigger input. It requires an external pull-up resistor.
I2C_SDA	A21	IO	ST-PU	1.8	Management processor I2C serial data. This signal has a Schmitt trigger input. It requires an external pull-up resistor.
PWM Interface					
PWM_0	A19	O	-	1.8	Management processor – Pulse Width Modulation waveform output 0. This signal changes state: ▪ From high to low when an internal 32-bit counter clocked at 250MHz equals a configured value. ▪ From low to high when the 32-bit counter wraps around at a configured value.
PWM_1	B19	O	-	1.8	Management processor – Pulse Width Modulation waveform output 1. This signal changes state: ▪ From high to low when an internal 32-bit counter clocked at 250MHz equals a configured value. ▪ From low to high when the 32-bit counter wraps around at a configured value.

Table 7. Management Processor Interface Signals (Cont.)

Signal Name	Ball	Type		Voltage	Description
GPIO Interface					
GPIO_0	C2	IO	ST	1.8	General purpose I/Os. This signal has an Schmitt trigger input.
GPIO_1	D1	IO	ST	1.8	
GPIO_2	D2	IO	ST	1.8	
GPIO_3	E1	IO	ST	1.8	
GPIO_4	E2	IO	ST	1.8	
GPIO_5	E3	IO	ST	1.8	
GPIO_6	F1	IO	ST	1.8	
GPIO_7	F2	IO	ST	1.8	
GPIO_8	F3	IO	ST	1.8	
GPIO_9	G1	IO	ST	1.8	
GPIO_10	G2	IO	ST	1.8	
GPIO_11	H1	IO	ST	1.8	
GPIO_12	H2	IO	ST	1.8	
GPIO_13	J1	IO	ST	1.8	
GPIO_14	J2	IO	ST	1.8	
GPIO_15	J3	IO	ST	1.8	

Table 8. MSFE Signals

Signal Name[a]	Ball	Type		Voltage	Description
MSFEx_ADC_IN	Y22, Y1	I	A		MSFEx high-speed differential ADC I-channel input. This signal can be swapped in digital domain.
MSFEx_ADC_IP	AA22, AA1	I	A		
MSFEx_ADC_QN	AB21, AB2	I	A		MSFEx high-speed differential ADC Q-channel input. This signal can be swapped in digital domain.
MSFEx_ADC_QP	AB20, AB3	I	A		
MSFEx_ADC_VCM	AA21, AA2	O	A		MSFEx high-speed ADC VCM output. This signal provides internally generated common-mode voltage for use with DC coupled circuits.
MSFEx_DAC_IN	AB13, AB10	O	A		MSFEx high-speed differential DAC I-channel output. This signal can be swapped in digital domain.
MSFEx_DAC_IP	AB12, AB11	O	A		
MSFEx_DAC_QN	AB15, AB8	O	A		MSFEx high-speed differential DAC Q-channel output. This signal can be swapped in digital domain.
MSFEx_DAC_QP	AB14, AB9	O	A		
MSFEx_CLKOUT	AA19, AA4	O	-	1.8	MSFEx single-ended reference clock output from the integrated crystal oscillator.
MSFEx_REFCLKN	AB19, AB4	I	CML_I	1.8	MSFEx IQ DAC and ADC differential reference clock inputs.The required typical clock frequency is 45MHz.
MSFEx_REFCLKP	AB18, AB5	I		1.8	
MSFEx_XI	AB16, AB7	I	A		MSFEx Crystal Connection. Input to high-Q integrated 45MHz crystal oscillator. This signal can be driven with a single-ended reference input clock.
MSFEx_XO	AB17, AB6	O	A		MSFEx Crystal Connection. Output from the integrated crystal oscillator.

[a] MSFEx implies both MSFE0 and MSFE1 interfaces, which are identical; ball names correspond to MSFE0 and MSFE1 in that order.

Table 9. JTAG/Test Signals

Signal Name	Ball	Type		Voltage	Description
JTAG_TCK	B21	I	ST-PD	1.8	IEEE 1149.1/1149.6 test access port. Clock input. This signal is a Schmitt trigger input with internal pull-down.
JTAG_TDI	C20	I	ST-PU	1.8	IEEE 1149.1/1149.6 test access port. Serial data input. This signal is a Schmitt trigger input with internal pull-up.
JTAG_TDO	B20	O	OD	1.8	IEEE 1149.1/1149.6 test access port. Serial data output.
JTAG_TMS	C21	I	ST-PU	1.8	IEEE 1149.1/1149.6 test access port. Mode select input. This signal is a Schmitt trigger input with internal pull-up.
JTAG_TRSTN	D21	I	ST-PD	1.8	IEEE 1149.1/1149.6 test access port. Reset input. This signal is a Schmitt trigger input with internal pull-down.
JTAG_SELECT	D20	I	PD	1.8	JTAG Select. Access to the JTAG TAP controller in the PCIe PHY is controlled by the state of this pin: ▪ 0 = PCIe TAP controller is chained in series following the boundary scan TAP controller ▪ 1 = Exclude PCIe TAP controller. Only the boundary scan TAP controller is accessible. Note: JTAG_SELECT must be set to 1 during boundary scan.

2.1.2 Supply Signals

Table 10. Power Supply and Reference Signals

Signal Name	Ball	Description
VDD	R6, H7, K7, M7, P7, G8, J8, L8, N8, R8, H9, K9, M9, P9, G10, J10, L10, N10, R10, H11, K11, M11, P11, G12, J12, L12, N12, R12, H13, K13, M13, P13, J14, L14, N14, R14, H15, K15, M15, P15, G16, J16, L16, N16, R16, K17, M17, P17	These pins provide 0.9V with respect to VSS for the core digital logic.
VDDIO	D3, H3, W4, J6, L6, N6, G14, H17, L18, D19, F19, W19	These pins provide 1.8V with respect to VSSIO for the digital I/Os.
RCI0_VDDIO	U18	These pins provide 1.8V with respect to VSSIO for the digital RCI0/1 CMOS I/Os.
RCI1_VDDIO	T5	
LVDS_VDDIO	W2, M3, P4, M19, P19, W21	These pins provide 1.8V with respect to VSSIO for the RCI0/1 LVDS I/Os.
PCIE_VP	F13	This pin provides 0.9V analog supply with respect to VSS for the PCIe.
PCIE_VPH	E10	This pin provides 1.8V analog supply with respect to VSS for the PCIe.
PCIE_VPTX	F11	This pin provide 0.9V with respect to VSS for the PCIe PHY transmit.

Table 10. Power Supply and Reference Signals (Cont.)

Signal Name	Ball	Description
PLL0_DVDD	F17	This pin provides 0.9V with respect to PLL0_DVSS for the system PLL0 digital logic.
PLL1_DVDD	F14	This pin provide 0.9V with respect to PLL1_DVSS for the system PLL1 digital logic
PLL0_VDDH	D17	This pin provides 1.8V with respect to PLL0_AVSS for the system PLL0 analog circuitry
PLL0_VDDA	E17	This pin provides 0.9V with respect to PLL0_AVSS for the system PLL0 analog circuitry
PLL1_VDDH	D14	This pin provide 1.8V with respect to PLL1_AVSS for the system PLL1 analog circuitry
PLL1_VDDA	E14	This pin provide 0.9V with respect to PLL1_AVSS for the system PLL1 analog circuitry
MSFE0_AVDD	T12, U13, V14	This pin provide 0.9V with respect to MSFE0_AVSS for the MSFE0 ADC/DAC.
MSFE0_PLL_AVDD	T16	This pin provide 0.9V with respect to MSFE0_AVSS for the MSFE0 PLL.
MSFE0_AVDDH	W15, V16, U17, W17	This pin provide 1.8V with respect to MSFE0_AVSS for the MSFE0 ADC/DAC.
MSFE0_OSC_AVDDH	T14	This pin provides 1.8V with respect to MSFE0_AVSS for the MSFE0 oscillator.
MSFE0_PLL_AVDDH	U15	This pin provides 1.8V with respect to MSFE0_AVSS for the MSFE0 PLL
MSFE1_AVDD	V9, U10, T11	This pin provide 0.9V with respect to MSFE1_AVSS for the MSFE1 ADC/DAC.
MSFE1_PLL_AVDD	T7	This pin provide 0.9V with respect to MSFE1_AVSS for the MSFE1 PLL.
MSFE1_AVDDH	U6, W6, V7, W8	This pin provide 1.8V with respect to MSFE1_AVSS for the MSFE1 ADC/DAC.
MSFE1_OSC_AVDDH	T9	This pin provide 1.8V with respect to MSFE1_AVSS for the MSFE1 oscillator.
MSFE1_PLL_AVDDH	U8	This pin provide 1.8V with respect to MSFE1_AVSS for the MSFE1 PLL
TSENSE_AVDDH	G6	This pin provide 1.8V with respect to TSENSE_AVSS for the Temperature Sensor analog circuitry.
RCI0_REF	R20	This pin provides a reference 1.2V with respect to VSSIO for the RCI0 LVDS I/Os.
RCI1_REF	R3	This pin provide a reference 1.2V with respect to VSSIO for the RCI1 LVDS I/Os.

2.1.3 Ground Signals

Table 11. Ground Signals

Signal Name	Ball	Description
VSS	B5, K6, M6, B7, E7, J7, L7, N7, R7, F8, H8, K8, M8, P8, B9, E9, G9, J9, L9, N9, R9, F10, H10, K10, M10, P10, B11, E11, G11, J11, L11, N11, R11, F12, H12, K12, M12, P12, B13, E13, G13, J13, L13, N13, R13, H14, K14, M14, P14, A15, J15, L15, N15, R15, H16, K16, M16, P16, J17, L17, N17, R17, M18, E4	These pins provide the reference shared ground for the digital core logic and PCIe.
VSSIO	A1, W1, G3, P3, W3, D4, M4, U5, H6, P6, G15, G17, K18, T18, C19, F20, M20, P20, W20, A22, W22, C17, C16, C15, H19, K19, E19, C12, D12, C11, D11, C10, D10, C9, D9, C8, D8, C7, D7, C6, D6, C5, D5, C4, E5, F6, F5, F4, G5, G4, H5, H4, D13, C18, D16, D18, D15, B18, C14	These pins provide the reference shared ground for the digital and LVDS I/Os.
PLL0_DVSS	F16	This pin provides the reference ground for the system PLL0 digital logic.
PLL1_DVSS	F15	This pin provides the reference ground for the system PLL1 digital logic.
PLL0_AVSS	E16	This pin provides the reference ground for the system PLL0 analog circuitry.
PLL1_AVSS	E15	This pin provides the reference ground for the system PLL1 analog circuitry.
MSFE0_AVSS	U12, V12, W12, Y12, AA12, T13, V13, W13, Y13, AA13, U14, W14, Y14, AA14, T15, V15, Y15, U16, W16, T17, V17, AA17, W18, AA18, AA20, Y21, AB22	These pins provide the reference ground for MSFE0 analog circuitry.
MSFE1_AVSS	AB1, Y2, AA3, W5, AA5, T6, V6, AA6, U7, W7, T8, V8, Y8, U9, W9, Y9, AA9, T10, V10, W10, Y10, AA10, U11, V11, W11, Y11, AA11	These pins provide the reference ground for MSFE1 analog circuitry.
TSENSE_AVSS	G7	This pin provides the reference ground for the temperature sensor analog circuitry.

2.1.4 Do Not Connect Signals

Table 12. DNC Signals

Signal Name	Ball	Description
DNC	A3, A6, A7, E8, F7, F9, AA7, AA8, AA15, AA16	Do not connect signals.

3. Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RWM6050 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 13. Absolute Maximum Ratings

Symbol[a]	Parameter	Minimum	Typical	Maximum	Unit
Power Supplies					
VDD, PCIE_VP, PCIE_VPTX, PLLx_VDDA, MSFEx_AVDD, MSFEx_PLL_AVDD,	0.9V Nominal Rated Supplies	-0.4		1.1	V
VDDIO, LVDS_VDDIO, PCIE_VPH, PLLx_VDDH, MSFEx_AVDDH, MSFEx_OSC_AVDDH, MSFEx_PLL_AVDDH, TSENSE_AVDDH	1.8V Nominal Rated Supplies	-0.4		2.2	V
ESD					
VESD_HBM	Human Body Model Electrostatic discharge voltage JESD22-A114	2			kV
VESD_RCDM	Charge Discharge Model Electrostatic discharge voltage JESD22-C101	350			V
Thermal and Power					
T_{STG}	Storage temperature	-65		150	^{o}C
$T_{JUNCTION}$	Operating temperature (junction)	-40		125	^{o}C

[a] RCIx, PLLx and MSFEx represent RCI0 / RCI1, PLL0 / PLL1 and MSFE0 / MSFE1 respectively.

3.2 Recommended Operating Conditions

Table 14. Recommended Operating Conditions[a]

Symbol[b]	Parameter	Minimum	Typical	Maximum	Unit
VDD	Core 0.9V supply	0.8775	0.9	0.9225	V
VDDIO	Digital LVCMOS I/O 1.8V supply	1.755	1.8	1.845	V
LVDS_VDDIO	LVDS I/O 1.8V supply	1.755	1.8	1.845	V
RCIx_REF	LVDS pads 1.2V reference voltage	1.188	1.2	1.212	V
PCIE_VP	PCIe 0.9V analog supply	0.8775	0.9	0.9225	V
PCIE_VPH	PCIe 1.8V high voltage supply	1.71	1.8	1.89	V
PCIE_VPTX	PCIe 0.9V PHY transmit supply	0.8775	0.9	0.9225	V
PLLx_DVDD	PLLx 0.9V digital voltage supply	0.8775	0.9	0.9225	V
PLLx_VDDH	PLLx 1.8V high voltage supply	1.71	1.8	1.89	V
PLLx_VDDA	PLLx 0.9V analog supply	0.8775	0.9	0.9225	V
MSFEx_AVDD	MSFEx ADC/DAC 0.9V analog supply	0.8775	0.9	0.9225	V
MSFEx_PLL_AVDD	MSFEx PLL 0.9V analog supply	0.8775	0.9	0.9225	V
MSFEx_AVDDH	MSFEx ADC/DAC 1.8V supply	1.71	1.8	1.89	V
MSFEx_OSC_AVDDH	MSFEx Oscillator 1.8V supply	1.71	1.8	1.89	V
MSFEx_PLL_AVDDH	MSFEx PLL 1.8V supply	1.71	1.8	1.89	V
TSENSE_AVDDH	Temperature sensor 1.8V analog supply	1.71	1.8	1.89	V

[a] Exposure to conditions outside the recommended operating conditions can affect the operation and/or reliability of the device.

[b] RCIx, PLLx and MSFEx represent RCI0 / RCI1, PLL0 / PLL1 and MSFE0 / MSFE1 respectively.

3.3 Supply Currents and Power

Table 15. Supply Currents and Power

Supply[a]	Description	Current (mA)	Voltage (V)		Power (mW)[b][c]
		Maximum	Typical	Maximum	Maximum
VDD	Core supply	4600	0.9	0.9225	4243.5
VDDIO	Digital I/O supply	210	1.8	1.845	387.5
LVDS_VDDIO	LVDS I/O supply	160	1.8	1.845	295.2
RCIx_REF	RCIx LVDS pad reference	1	1.2	1.212	1.21
PCIE_VP PCIE_VPTX	PCIe analog supply	150	0.9	0.9225	138.4
PCIE_VPH	PCIe high-voltage supply	75	1.8	1.89	141.8
MSFEx_AVDD MSFEx_PLL_AVDD	MSFEx ADC 0.9V analog supply	500	0.9	0.9225	461.3
MSFEx_AVDDH MSFEx_OSC_AVDDH MSFEx_PLL_AVDDH	MSFEx ADC 1.8V supply	350	1.8	1.89	661.5
PLLx_VDDH	Analog PLL supply voltage	50	1.8	1.89	94.5
PLLx_VDDA PLL_DVDD	Analog PLL supply voltage	50	0.9	0.9225	46.1
TSENSE_AVDDH	Temperature sensor analog supply	0.5	1.8	1.89	1.0
Total		**6146.5**			**6471.8**

[a] RCIx, PLLx and MSFEx represent RCI0 / RCI1, PLL0 / PLL1 and MSFE0 / MSFE1 respectively. Reported power of these domains is included twice in the total power.

[b] Maximum power numbers are based on worst case process corner and T_J = 125°C.

[c] All power numbers are based on UDP, MCS12, maximum voltage with 100% traffic on both MSFE interfaces. For power numbers associated with all other configuration, please contact Renesas support.

3.4 Power Supply Sequencing

The voltages on any input or I/O pin cannot exceed its corresponding supply voltage during power supply ramp-up.

3.4.1 Ramp-up Time

All power supplies should ramp up with minimum rise time of 15µs to ensure the ESD structure remains off during power-up. The maximum time spread between the power-up times of all power supplies should not exceed 90ms.

3.4.2 Power-up Sequencing

1. (Recommended) Power up VDDIO before VDD. All LVCMOS outputs are tri-stated when VDD is not powered up.
2. Power up LVDS_VDDIO then VDD.
3. Power up MSFEx_AVDDH, MSFEx_OSC_AVDDH, MSFEx_PLL_AVDDH first followed by VDD and then MSFEx_AVDD, MSFEx_PLL_AVDD.
4. Power up PCIE_VP, PCIE_VPTX, and PCIE_VPH in any order.
5. Power up PLLx_VDDH, PLLx_VDDA, and TSENSE_AVDDH in any order.

3.4.3 Power-down Sequencing

1. (Recommended) Power down MSFEx_AVDD and MSFEx_PLL_AVDD first followed by VDD and then MSFEx_AVDDH, MSFEx_OSC_AVDDH, and MSFEx_PLL_AVDDH.
2. (Recommended) Power down VDD then VDDIO.
3. (Recommended) Power down VDD then LVDSD_VDDIO.
4. Power down PCIE_VP, PCIE_VPTX, and PCIE_VPH in any order.
5. Power down PLLx_VDDH, PLLx_VDDA, and TSENSE_AVDDH in any order.

3.5 DC Electrical Characteristics

DC characteristics for LVCMOS and LVDS I/Os are displayed in Table 16 and Table 17.

3.5.1 LVCMOS I/Os

Table 16. 1.8V LVCMOS I/O DC Parameters

Parameter	Description	Minimum	Maximum	Unit
V_{IL}	Input Low Voltage	-0.3	0.63	V
V_{IH}	Input High Voltage	1.17	1.98	V
V_{TLH}	Schmitt Trigger Low to High Threshold Point	0.95	1.11	V
V_{THL}	Schmitt Trigger High to Low Threshold Point	0.67	0.9	V
V_{TLHPU}	Schmitt Trigger Low to High Threshold with Pull-up Enabled	0.94	1.11	V
V_{THLPU}	Schmitt Trigger High to Low Threshold with Pull-up Enabled	0.67	0.89	V
V_{TLHPD}	Schmitt Trigger Low to High Threshold with Pull-down Enabled	0.95	1.12	V
V_{THLPD}	Schmitt Trigger High to Low Threshold with Pull-down Enabled	0.68	0.9	V
V_{OL}	Output Voltage Low At V_{OL} maximum and default drive strength: ▪ Nominal I_{OL} = 13 mA for SYSOSC_XO ▪ Nominal I_{OL} = 36 mA for all other LVCMOS output and bi-directional pins		0.45	V
V_{OH}	Output Voltage High. At V_{OH} min and default drive strength: ▪ Nominal I_{OH} = -8.8 mA for SYSOSC_XO ▪ Nominal I_{OH} = -33 mA for all other LVCMOS output and bi-directional pins	1.35		V
I_I	Input Leakage Current at input voltage 1.8V or 0V		±10	µA
I_{OZ}	Tri-state Output Leakage Current at output voltage 1.8V or 0V		±10	µA
R_{PU}	Pull-up Resistor	54k	120k	Ω
R_{PD}	Pull-down Resistor	55k	176k	Ω
C_{PIN}	Pin capacitance (typical value ~ 3pF)		10	pF

3.5.2 LVDS I/O

Table 17. LVDS I/O DC Parameters

Parameter	Description	Minimum	Typical	Maximum	Unit
V_{LDVS_OH}	Output Voltage High (Rload = 100Ω)			1.475	V
V_{LDVS_OL}	Output Voltage Low (Rload = 100Ω)	0.925			V
V_{LDVS_OD}	Output Differential Voltage (Rload = 100Ω)	250		400	mV
V_{LDVS_OS}	Output Offset Voltage (Rload = 100Ω)	1.125		1.275	V
R_{LDVS_OI}	Output Impedance	40		140	Ω

3.6 LVCMOS and LVDS I/O AC Specifications

This section contains AC timing specifications and electrical characteristics for the LVCMOS and LVDS I/Os.

3.6.1 AC Timing Test Conditions

The following tables explain the test conditions for the AC timing specifications.

Table 18. LVCMOS AC Test Conditions for VDDIO = 1.8V

Parameter	
Input slew rate	2.4V/ns 10–90%
Input timing reference level	0.9V
Output reference levels	0.9V
Output load ▪ I2C_SCL and I2C_SDA ▪ RCI LVCMOS outputs ▪ All other LVCMOS outputs	 C_{LOAD} = 10nF C_{LOAD} = 10nF C_{LOAD} = 10nF

Table 19. LVDS AC Test Conditions for LVDS_VDDIO = 1.8V

Parameter	
Output reference levels	1.2V
Output load	C_{LOAD} = 25 pF

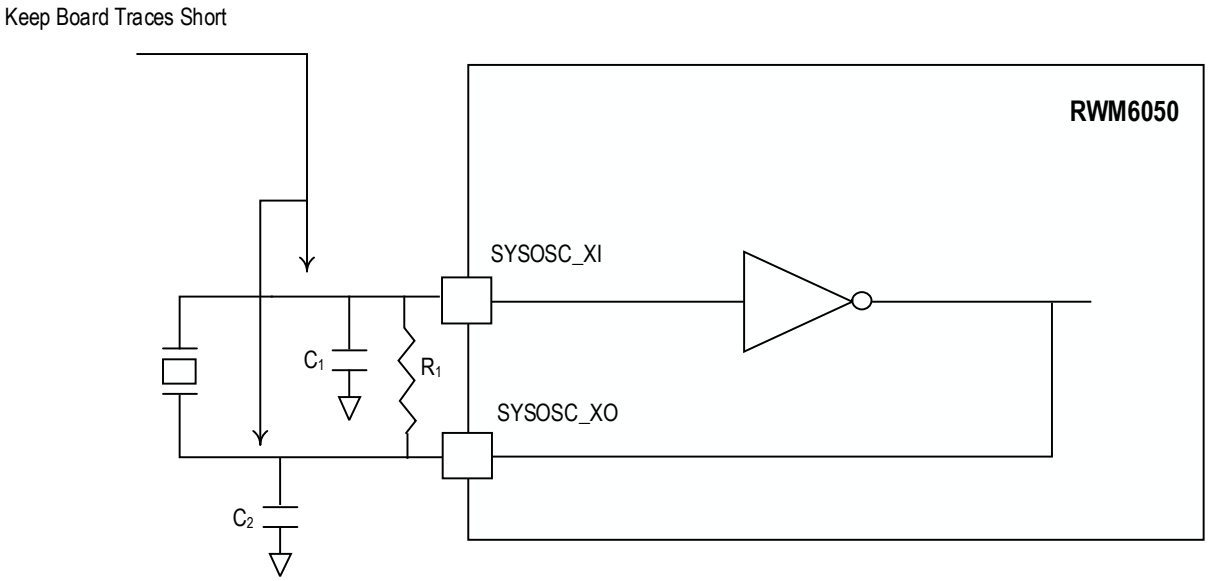
3.6.2 Reference Clock Timing Specification

The RWM6050 contains two system PLLs that are used to generate system clocks. The reference of these two PLL can be sourced internally via an external 25MHz crystal oscillator, or via an external single-ended high quality reference clock with very low jitter.

3.6.2.1 External System Crystal Oscillator

The system external oscillator requires external components as shown in Figure 4. Exact component values in the figure depend on crystal choice and PCB layout. For the recommended capacitor and resistor values, see the manufacturer's datasheet.

Figure 4. Circuit for the System XTAL



3.6.2.2 External Single-ended System Reference Clock

A single-ended reference clock can be provided via the crystal input pin SYSOSC_XI, as displayed in Figure 5. Table 21 lists the reference clock signal timing specifications.

Figure 5. Single-ended System Reference Clock[1]

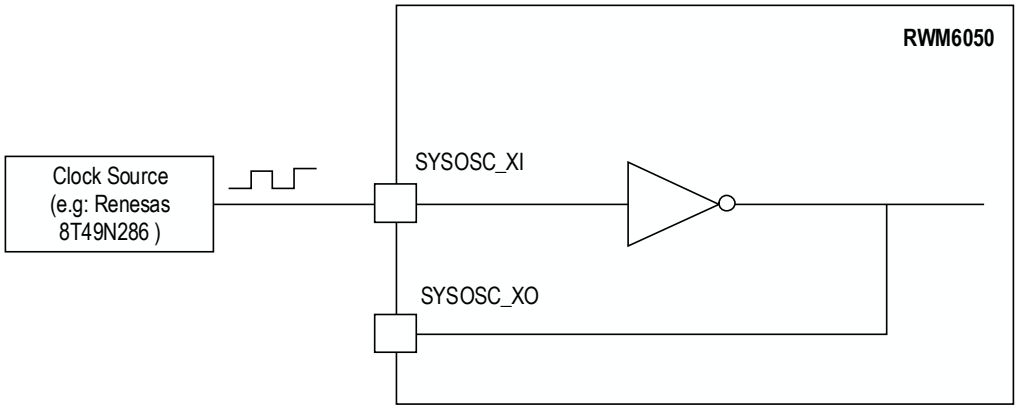


Table 21. Reference Clock Specification

Parameter	Description	Minimum	Typical	Maximum	Unit
F_{SREF}	System reference frequency		25		MHz
T_{PRD}	System reference period		40		ns
T_{DUTY}	System reference duty cycle	40	50	60	%
T_J	System reference phase jitter		0.2		ps, rms
R_{Slew}	Slew Rate		0.2		V/ns
T_{PPM}	System reference clock accuracy	-30		30	ppm

3.6.3 Reset Signal Timing Specifications

The following table lists the reset signal, RESET_N, timing specifications.

Table 22. Reset Signal Timing Specifications[a]

Symbol	Parameter	Minimum	Maximum	Unit
T_{RST}	When asserted, RESET_N must remain asserted at least this long after power becomes valid and the clocks become stable and within the specified frequencies.	100		µs

[a] During device power-up, PCIE_PERSTN must be asserted while RESET_N is asserted.

[1] Refer to the clock source device for the recommended interface to the SYSOSC_XI input.

3.6.4 JTAG Signal Timing Specifications

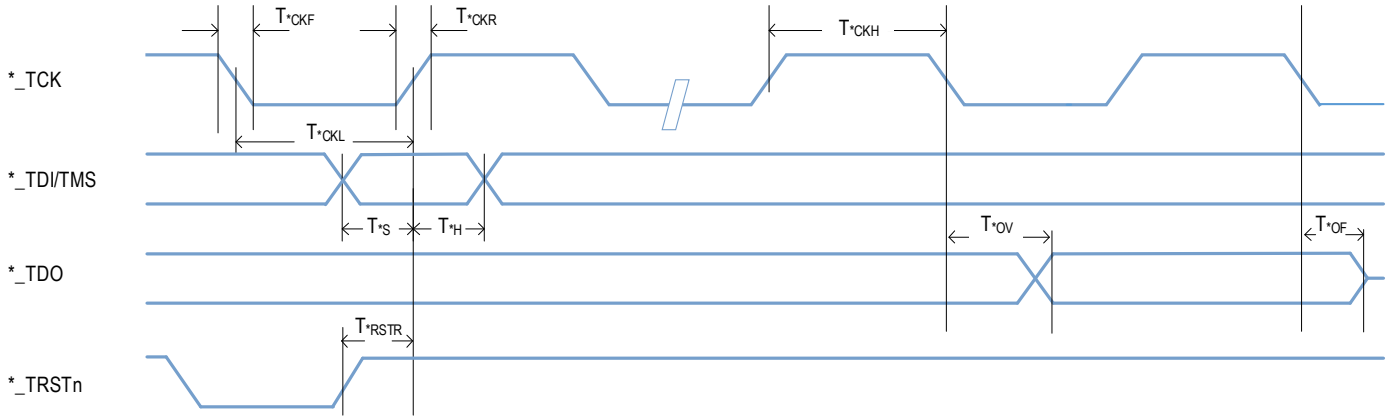
The following table lists the JTAG signal timing specifications.

Table 23. JTAG Signal Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
F_{JCK}	JTAG_TCK frequency		20	MHz
T_{JCKH}	JTAG_TCK high time	20		ns
T_{JCKL}	JTAG_TCK low time	20		ns
T_{JCKR}	JTAG_TCK rise time		5	ns
T_{JCKF}	JTAG_TCK fall time		5	ns
T_{JS}	JTAG_TMS, JTAG_TDI set up to rising edge of JTAG_TCK	10		ns
T_{JH}	JTAG_TMS, JTAG_TDI hold to rising edge of JTAG_TCK	10		ns
T_{JOV}	JTAG_TDO output valid delay from falling edge of JTAG_TCK		13	ns
T_{JOF}	JTAG_TDO output float delay from falling edge of JTAG_TCK		13	ns
T_{JRST}	JTAG_TRSTN minimum low time	16		ns
T_{JRSTR}	JTAG_TRSTN[a] recovery time to rising edge of JTAG_TCK	10		ns

[a] JTAG_TRSTN must be asserted while RESET_N is asserted during device power-up.

Figure 6. JTAG Signal Timing Diagram



3.6.5 Radio Control Interface Signal Timing Specifications

Table 24 and Figure 7 show the RCI LVCMOS signal timing specifications. The LVCMOS I/Os are used when the RWM6050 is configured to operate in QPSI/SPI mode.

Table 25 and Figure 8 show the RCI LVDS signal timing specifications. The LVDS I/Os are used when the RWM6050 is configured to operate in QPSI-Like mode.

Table 26/Table 27 and Figure 9/Figure 10 show the RCI LVCMOS GPIO signal timing specifications. The GPIO I/Os are used as general purpose and timed I/Os.

Table 24. RCI LVCMOS AC Timing Parameters

Symbol	Description	Minimum	Typical	Maximum	Unit
F_{SCLK}	Clock frequency	31.42		73.33	MHz
T_{SCLK}	RCI clock period	13.64		31.83	ns
T_{CSECK}	Chip select setup time	1.5			ns
T_{CKCSD}	Chip select hold time	1.5			ns
T_{DOS}	Data out valid before clock edge	1.5			ns
T_{DOH}	Data out hold time	1.5			ns
T_{DIH}	Data in hold time	1.5			ns
T_{DIS}	Data in setup time	6.5			ns
T_{CSDES}	Chip select de-select time	9.1			ns

Figure 7. RCI LVCMOS AC Timing Diagram

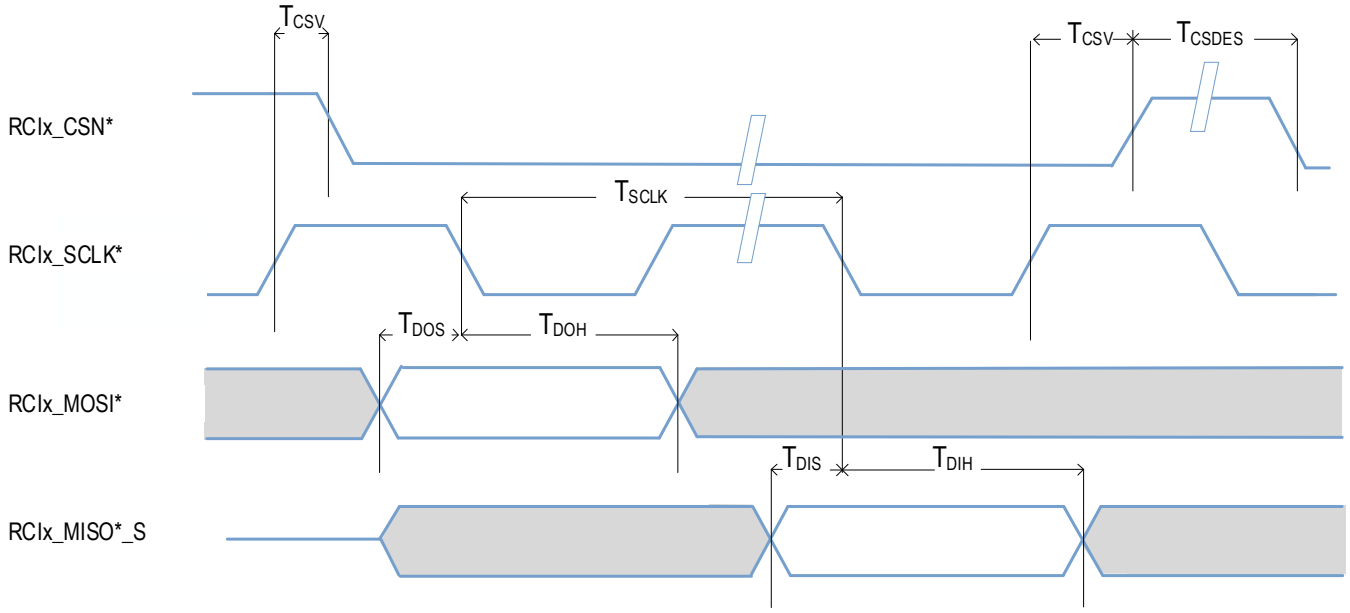


Table 25. RCI LVDS AC Timing Parameters

Symbol	Description	Minimum	Typical	Maximum	Unit
F_{SCLK}	Clock frequency			220	MHz
T_{SCLK}	RCI clock period	4.54			ns
T_{CSV}	Chip select valid after clock edge			1.5	ns
T_{DOS}	Data out valid before clock edge	1.5			ns
T_{DOH}	Data out hold time	1.5			ns
T_{DIH}	Data in hold time	1.5			ns
T_{DIS}	Data in setup time	4.5			ns
T_{CSDES}	Chip select de-select time	4.5			ns

Figure 8. RCI LVDS AC Timing Diagram

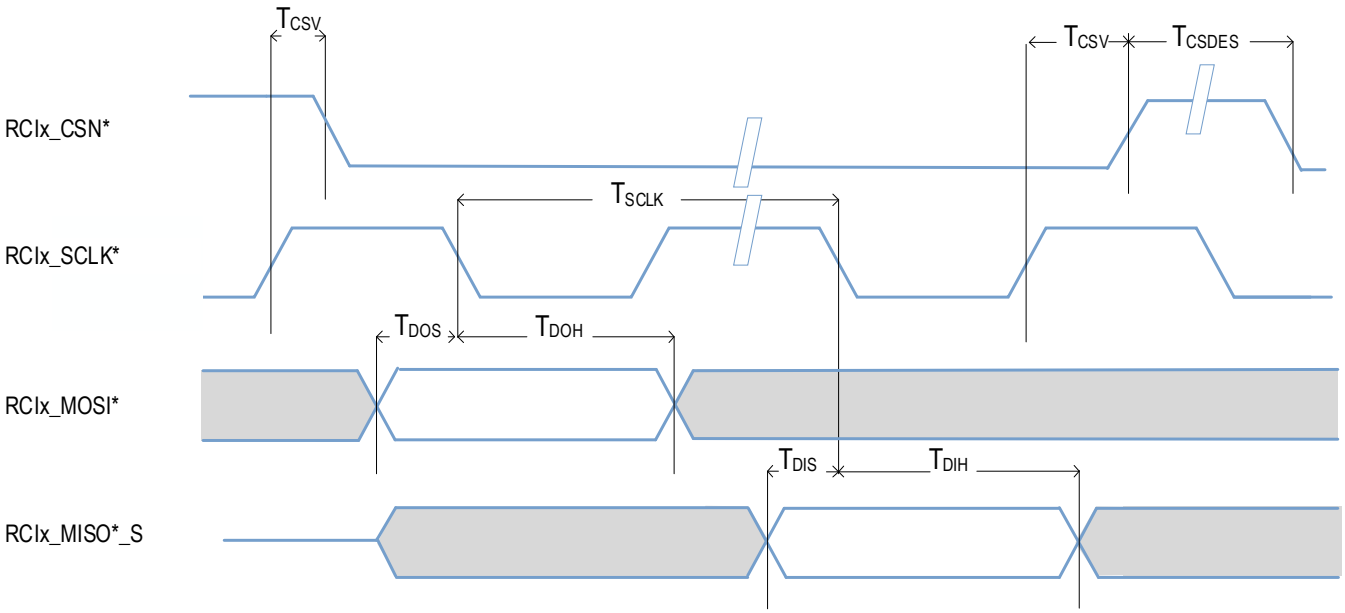


Table 26. RCIx_GPIO_n, n = 2:6, AC Timing Parameters – SDR Operation[a]

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{SWID}	Strobe width	4.6			ns
T_{SR}	Strobe rise time			1.6	ns
T_{SF}	Strobe fall time			1.6	ns
T_{DVAS}	Command word valid time after strobe edge	3.5			ns
T_{DVBS}	Command word valid time before strobe edge	3.5			ns

[a] This interface is intended for Automatic Gain Control of the RF receiver.

Figure 9. RCIx_GPIO_n, n = 2:6, AC Timing Diagram – SDR Operation

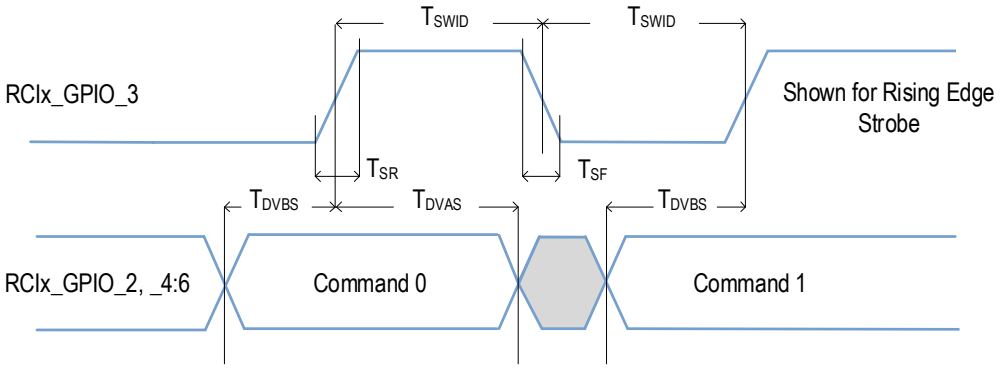
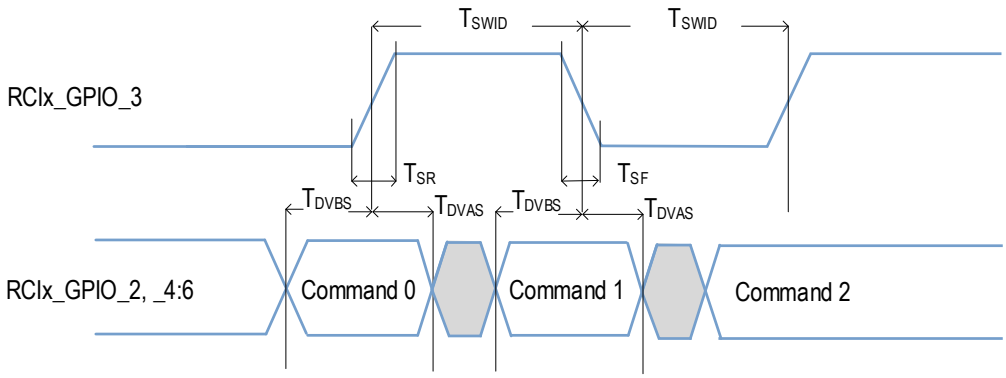


Table 27. RCIx_GPIO_n, n = 2:6, AC Timing Parameters – DDR Operation[a]

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{SWID}	Strobe width	9.2			ns
T_{SR}	Strobe rise time			2	ns
T_{SF}	Strobe fall time			2	ns
T_{DVAS}	Command word valid time after strobe edge	3.5			ns
T_{DVBS}	Command word valid time before strobe edge	3.5			ns

[a] This interface is intended for Automatic Gain Control of the RF receiver.

Figure 10. RCIx_GPIO_n, n = 2:6, AC Timing Diagram – DDR Operation



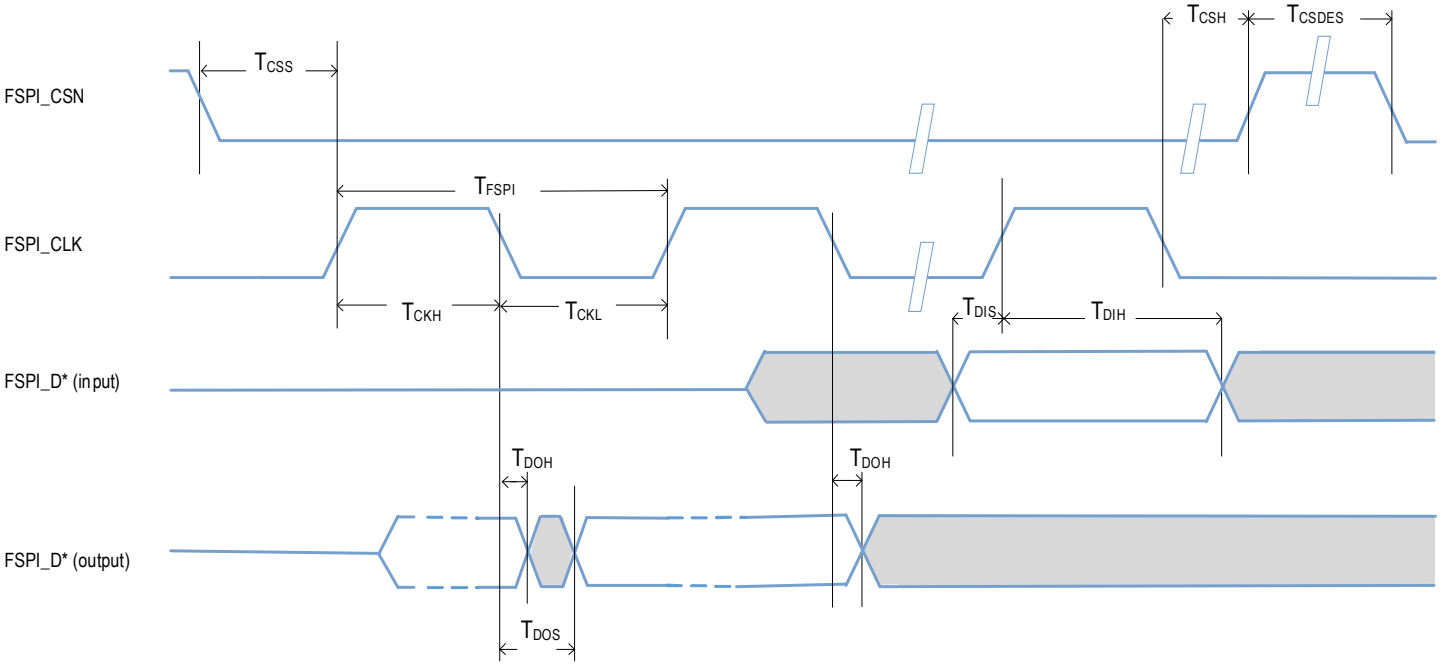
3.6.6 Flash SPI (FSPI) Boot Interface Signal Timing Specifications

The following table lists the Flash SPI Interface signal timing specifications as shown in Figure 11.

Table 28. FSPI Interface AC Timing Parameters

Symbol	Description	Minimum	Typical	Maximum	Unit
F_{FSPI}	FSPI_CLK clock frequency			50	MHz
T_{FSPI}	FSPI_CLK clock period	20			ns
T_{CKH}	FSPI_CLK high time	8			ns
T_{CKL}	FSPI_CLK low time	8			ns
T_{CSS}	Chip select setup time to FSPI_CLK	1			T_{FSPI}
T_{CSH}	Chip select hold time to FSPI_CLK	1			T_{FSPI}
T_{CSDES}	Chip de-select time	1.5			T_{FSPI}
T_{DOS}	FSPI_CLK to FSPI_D* valid	0			ns
T_{DOH}	FSPI_CLK to FSPI_D* invalid			2	ns
T_{DIH}	FSPI_D1_DO invalid from FSPI_CLK	4			ns
T_{DIS}	FSPI_D1_DO valid from FSPI_CLK	4			ns

Figure 11. FSPI AC Timing Diagram



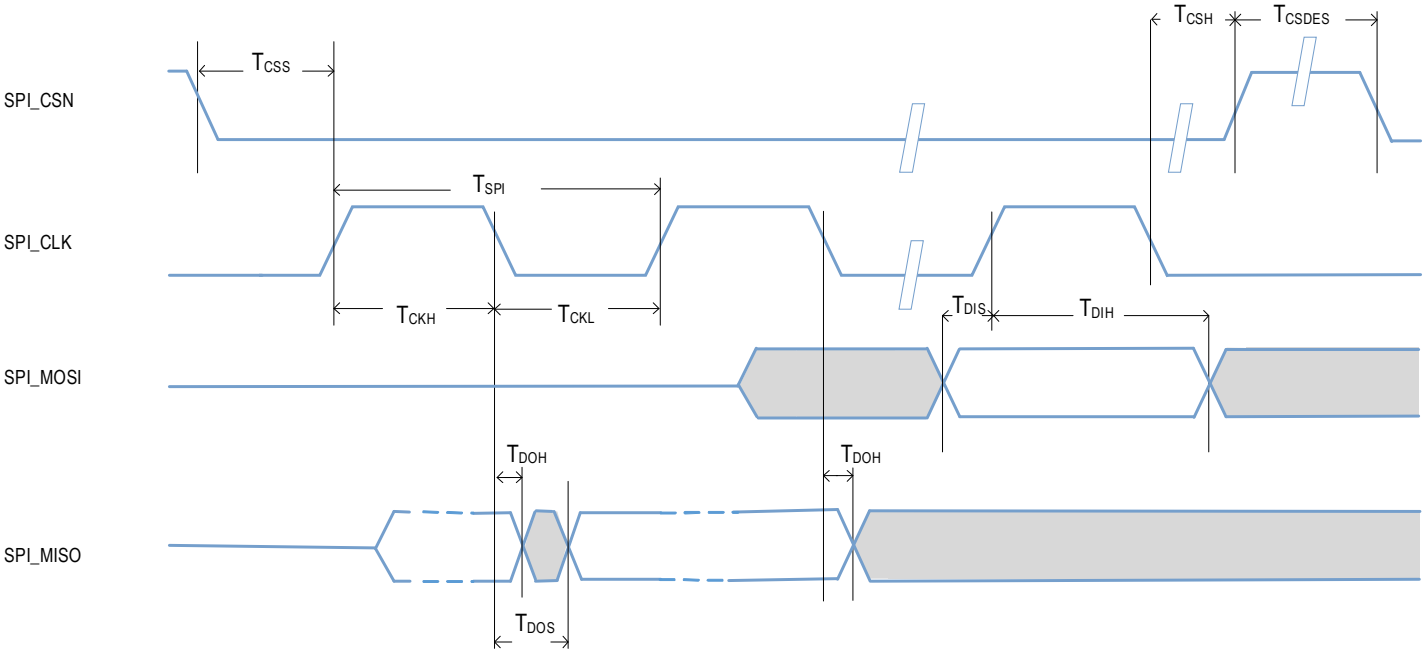
3.6.7 System SPI Interface Signal Timing Specifications

The following table lists the System SPI Interface signal timing specifications as shown in Figure 12.

Table 29. System SPI Interface AC Timing Parameters

Symbol	Description	Minimum	Typical	Maximum	Unit
F_{SPI}	SPI_CLK clock frequency			62.5	MHz
T_{SPI}	SPI_CLK clock period	16			ns
T_{CKH}	SPI_CLK clock high time	6.4			ns
T_{CKL}	SPI_CLK clock low time	6.4			ns
T_{CSS}	Chip select setup time to SPI_CLK	1			T_{SPI}
T_{CSH}	Chip select hold time to SPI_CLK	1			T_{SPI}
T_{CSDES}	Chip de-select time	1.5			T_{SPI}
T_{DOS}	SPI_CLK to MOSI valid			2	ns
T_{DOH}	SPI_CLK to MOSI invalid	0			ns
T_{DIH}	MISO invalid from SPI_CLK	4			ns
T_{DIS}	MISO valid from SPI_CLK	4			ns

Figure 12. System SPI AC Timing Diagram



3.6.8 I²C Interface Signal Timing Specifications

The following table lists the I²C Interface signal timing specifications as shown in Figure 30.

Table 30. I²C Interface Signal Timing Specifications

Symbol	Description[a]	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
F_{SCL}	I2C_SCL clock frequency	0	100		400	kHz
T_{LO}	I2C_SCL clock low time[b],[c]	4.7		1.3		µs
T_{HI}	I2C_SCL clock high time[b],[c]	4.0		0.6		µs
T_{HD}	I2C_SDA hold time[c]	[d]	3.45	[d]	0.9	µs
T_{SD}	I2C_SDA setup time[c]	250		100		ns
T_{SR}	Rise time of I2C_SCL and I2C_SDA[c] (30–70%)		1000	20[e]	300[d]	ns
T_{SF}	Fall time of I2C_SCL and I2C_SDA[c] (70–30%)		300	6.5[f]	300	ns
T_{BF}	Bus free time between STOP and START condition[c]	4.7		1.3		µs
T_{HSTRT}	Hold time (repeated) START condition[c],[g]	4.0		0.6		µs
T_{SSTRT}	Setup time for repeated START condition[c]	4.7		0.6		µs
T_{SSTP}	Setup time for STOP condition[c]	4.0		0.6		µs
T_{SPK}	Pulse width of spikes that must be suppressed by the input filter			0	50	ns

[a] An external pull-up resistor is required for specification compliance. Input reference levels are set as 30% and 70% of VDDIO.

[b] Not tested.

[c] See timing diagram in Figure 13.

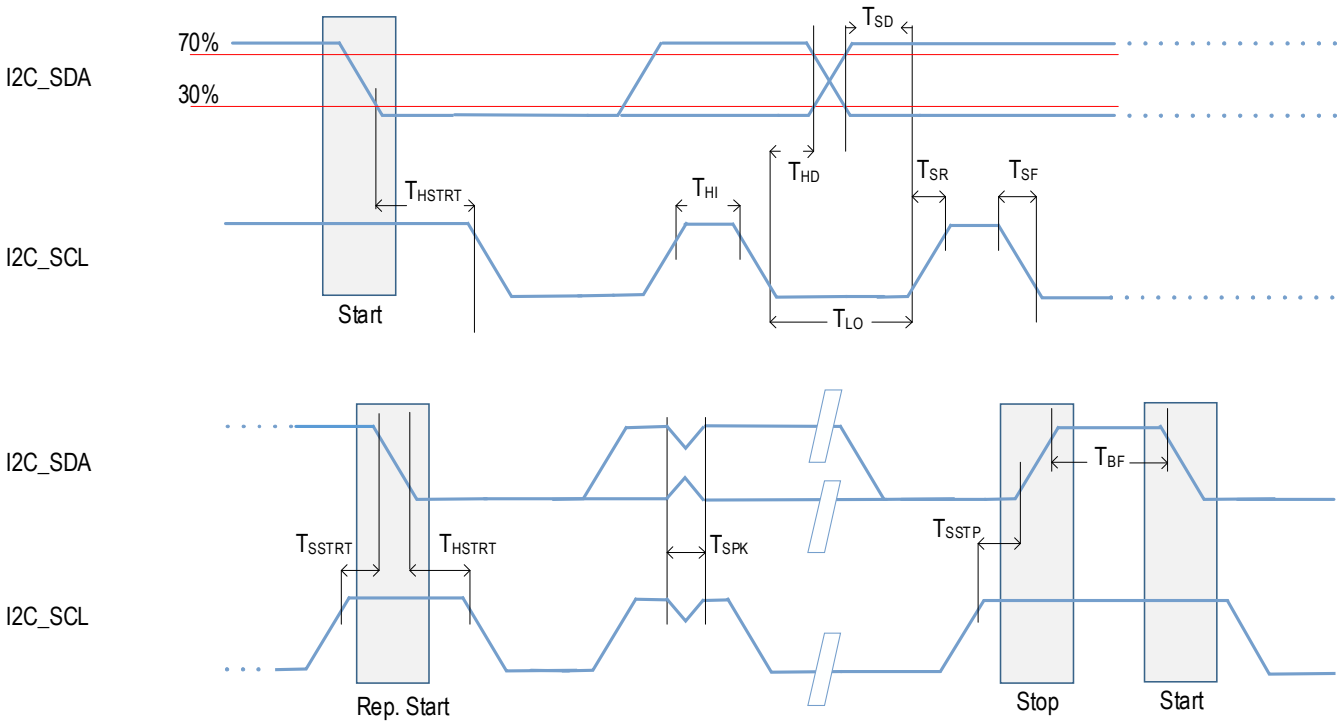
[d] When the RWM6050 drives I2C_SDA, it provides 300ns of hold time. When an external device drives I2C_SDA, it must provide a hold time of at least 300ns for I2C_SDA regarding V_{IH} min of the I2C_SCL.

[e] $20 \le 0.85 \times Rload(k\Omega) \times Cbus(pF) \le 300$.

[f] Cbus ≥ 40 pF.

[g] After this period, the first clock pulse is generated.

Figure 13. I²C AC Timing Diagram



3.7 Mixed Signal Front End Interface Characteristics

The RWM6050 Mixed Signal Front End (MSFE) includes integrated ADC and DAC for signal conversion and an integrated PLL to provide the required sample clock. The reference clock for the PLL is provided either by the RF transceiver or a common external temperature compensated Crystal Oscillator (TCXO).

3.7.1 MSFE ADC Specifications

The ADC can be AC or DC coupled. The target configuration for the RWM6050 is to use DC coupling since this reduces the time constants associated with DC offset changes more than AC coupling. In this configuration, the ADC provides a common mode output voltage as a reference.

The characteristic of the ADCs is given in Table 31. The ADC input range can be configured as shown in Table 32.

Table 31. ADC Characteristics

Parameter	Minimum	Typical	Maximum	Unit
Number of bits		7		
Effective number of bits		6[a]		
Sample rate			3.52	Gsps
Input full scale range (Typical)	0.29		0.69	Vppd
Full scale input at 0.575 Vppd typical	0.51	0.575	0.64	Vppd
Input common mode	0.4	0.6	0.7	V
Input capacitance to ground		0.3	0.4	pF
Differential input impedance	80	100	120	Ω
Integral non linearity	-1.2		1.2	LSB

Table 31. ADC Characteristics (Cont.)

Parameter	Minimum	Typical	Maximum	Unit
Differential non linearity	-1		1	LSB
SNR at 1.4GHz, -1dBfs	34	39		dBc
SINAD at 1.4GHz, -1dBfs	34	37		dBc
SFDR at 1.4GHz, -1dBfs	42	53		dBc
Aperture jitter		200	400	fs rms
IQ gain mismatch	-1.2		1.2	%
Aperture timing mismatch	-10		10	ps

[a] ENOB may be slightly under 6 bits under -20°C operating temperature.

Table 32. ADC Full-scale Input Configuration

Setting	Typical fsd	Unit
1	290	mVppd
2	345	mVppd
3	499	mVppd
4	460	mVppd
5	515	mVppd
6	575	mVppd
7	630	mVppd
8	690	mVppd

3.7.2 MSFE DAC Specifications

The RWM6050 provides a 100Ω on-chip output load to convert the current from the current-steering DAC to voltage. The DAC characteristics are listed in Table 33.

Table 33. IQ DAC Characteristics

Parameter	Minimum	Typical	Maximum	Unit
Number of bits		7		
Effective number of bits		6		
Sample rate		3.52		Gsps
Output full scale range (nominal)	1.84		5.0	mA
Full scale output at 5mA setting	4.75	5	5.25	mA
Gain adjustment resolution (per step)	48	50	52	uA
On-chip Output load (single ended to ground)		100		Ω
Output compliance			0.25	V
Integral non linearity	-1		1	LSB
Differential non linearity	-1		1	LSB
SNR at 800 MHz, -1dBfs	37	38		dBc
SINAD at 800 MHz, -1dBfs	35	36		dBc
SFDR at 800 MHz, -1dBfs	36	39		dBc
Aperture jitter			700	fs rms
IQ gain mismatch	-2		2	%
Aperture timing mismatch	-6		6	ps

3.7.3 MSFE Reference Clock

The integrated PLL is used to generate the 3.52GHz ADC and DAC sample clocks. The reference clock for the MSFE PLL can be sourced via an external CML differential reference input, via a CMOS external single-ended reference input, or via an external crystal oscillator. The two MSFE instances have independent clocking options. The specifications of the MSFE reference clock are listed in Table 34.

Table 34. MSFE Reference Clock Specifications

Parameter	Minimum	Typical	Maximum	Unit
MSFEx_REFCLKN/MSFEx_REFCLKP Differential CML Reference Clock				
Reference clock frequency[a]		45		MHz
Reference clock duty cycle	40		60	%
Reference clock accuracy	-10		10	ppm
CML Ref Clock Common Mode	0.3		0.7	V
CML Ref Clock Input Amplitude	0.6		2	V p-p diff
Differential Reference Load Resistance[b]		100		Ω
MSFEx_XI Single-ended Reference				
Voltage Swing Level [c]		0.9	0.99	V
Reference clock frequency[a]		45		MHz

[a] Required to meet jitter specifications.

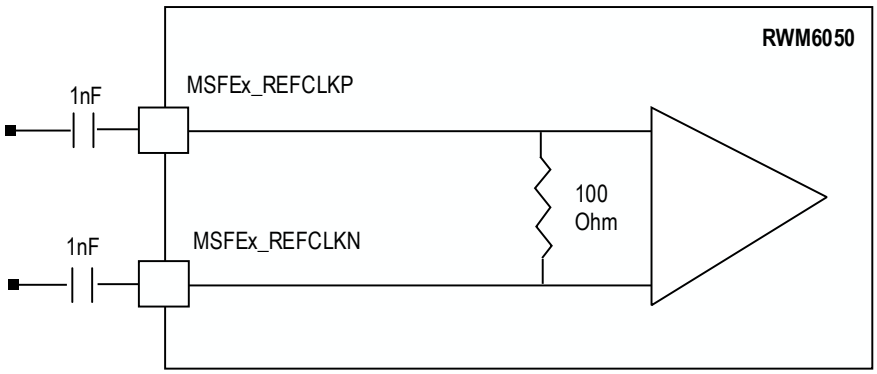
[b] Between MSFEx_REFCLKN and MSFEx_REFCLKP.

[c] Refer to Table 35.

3.7.3.1 MSFE Differential Reference Clock

AC coupling capacitors should be used with an external differential reference, as displayed in Figure 14.

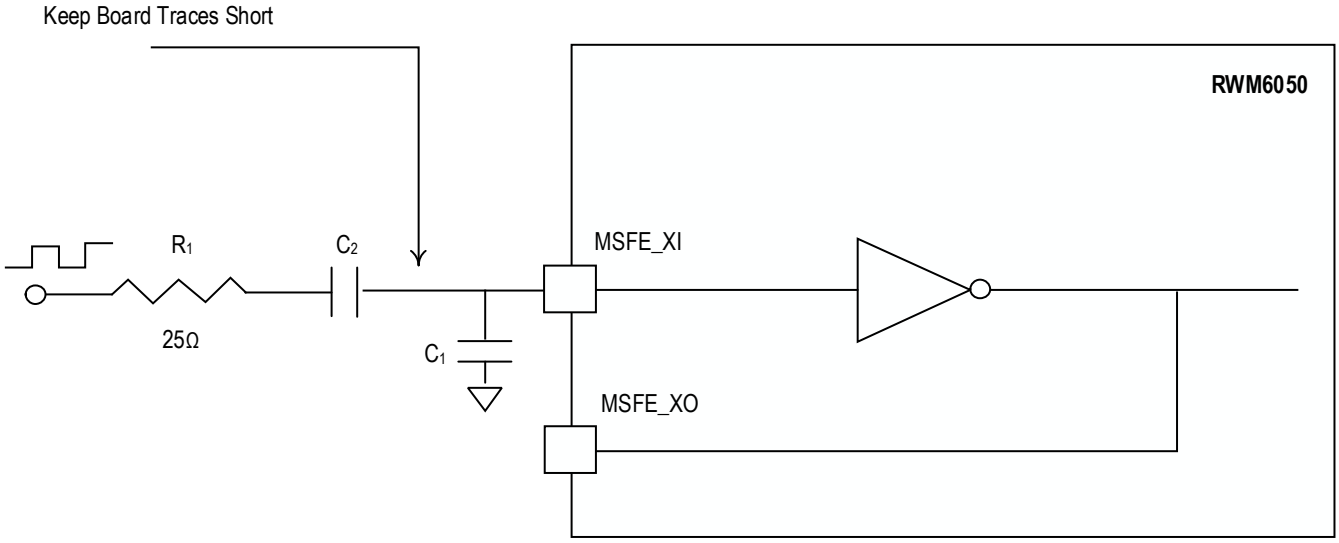
Figure 14. Differential MSFE Reference Clock with AC Coupling – An Example



3.7.3.2 Single-ended MSFE Reference Clock

The MSFE single-ended reference clock requires external components as shown in Figure 15. Exact component values in Figure 15 depend on PCB layout. For the recommended capacitor and resistor values, see the manufacturer's datasheet.

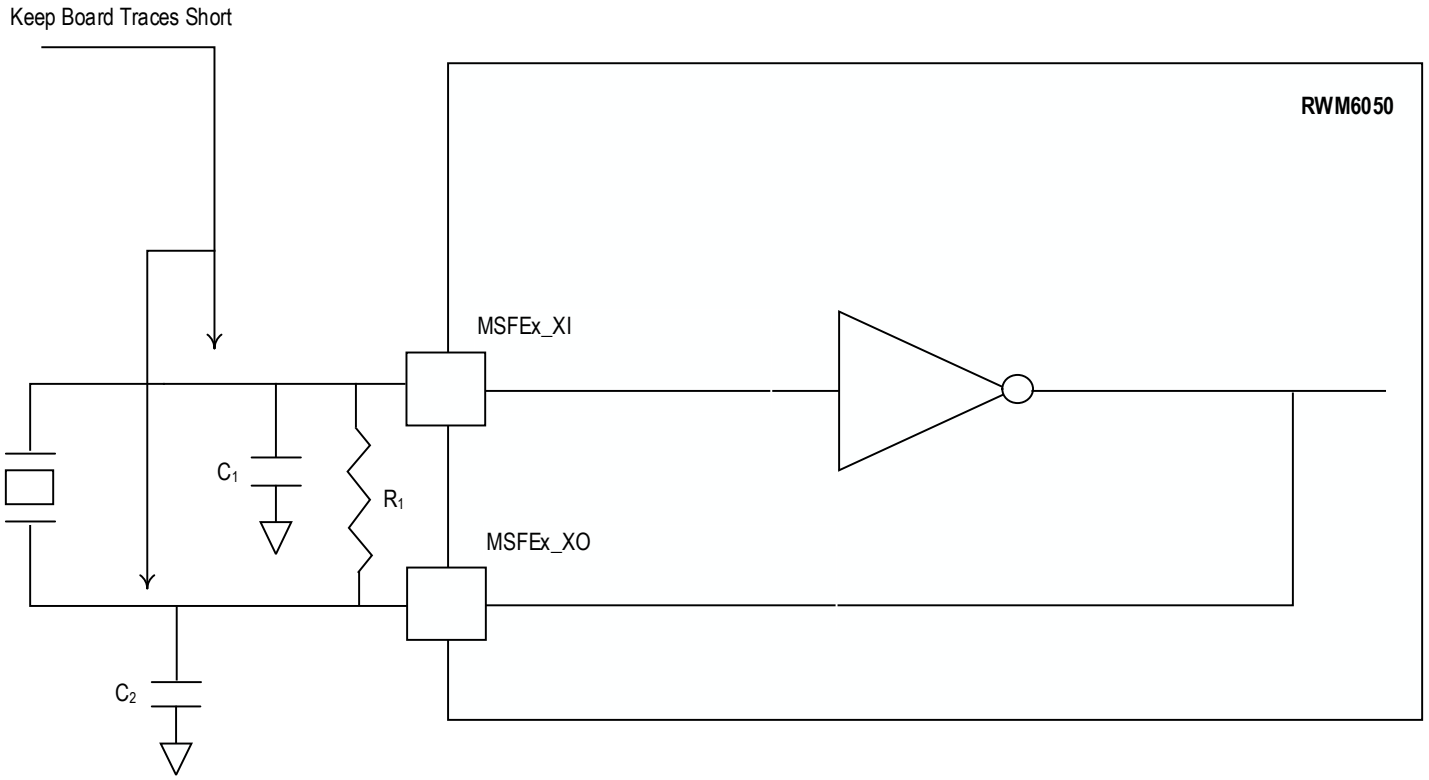
Figure 15. Single-ended MSFE Reference Clock Coupling



3.7.3.3 MSFE Crystal Oscillator

The MSFE external oscillator requires external components as shown in Figure 16. Exact component values in Figure 16 depend on crystal choice and PCB layout.

Figure 16. Circuit for the MSFE XTAL



3.8 PCIe Interface Characteristics

3.8.1 PCIe Reference Clock

The PCIe PHY supports a 100MHz input clock. The PCIe reference clock can be spread. If the reference clock provided to the PHY is spread for EMI purposes, both ends of the link must be spread synchronously. In addition, if the reference clock is a spread-spectrum than a common clock is required at both ends of the link.

When routing the reference clock from an off-chip source, terminated and unterminated clocks can both be used. With terminated clocks, a 50Ω termination resistor should be soldered on the board close to the RWM6050, preventing clock reflections. If the board clocks are unterminated, the clock's signal level doubles as it hits the high-impedance input of the RWM6050 reference clock inputs. This effect can be used to provide a clean clock to the PHY, but care should be taken to ensure that the signal swing of the reference clock is not too high after doubling the amplitude.

The reference clock inputs, PCIE_CLKP/PCIE_CLKN, are differential. If the reference clock requirements are met with a single-ended input clock, tie the unused reference input low or high. Table 37 lists the PCIe PHY reference clock requirements.

Table 37. PCIe PCIE_CLKP/PCIE_CLKN Requirements

Description	Minimum	Typical	Maximum	Unit
Reference clock frequency		100		MHz
Reference clock frequency offset	-300		300	ppm
Reference clock cycle-to-cycle jitter[a]			150	ps
Reference clock duty cycle	40		60	%
Common mode input level - Differential inputs	0		PCIE_VP	V
Differential input swing[b]	0.3			V p-p
Single ended input logic low	-0.3		0.3	V
Single-ended input logic high	PCIE_VP – 0.3		PCIE_VP + 0.3	V
Input edge rate	0.6			V/ns
Reference clock skew			200	ps

[a] Deterministic Jitter across all frequencies.

[b] Total input swing should be between -0.3V and PCIE_VP + 0.3V.

3.8.2 PCIe Differential Receiver and Transmitter Specifications

The RWM6050's SerDes logic fully complies to the *PCI Express Base Specification (Rev. 2.1)*. This section provides those specifications for reference purposes only. For complete requirements, see the specification.

3.8.2.1 PCIe Differential Receiver Specifications

Table 38 lists the main electrical characteristics for the PCIe differential receivers in the RWM6050. Parameters are defined separately for 2.5 and 5.0Gbps. For more information, see Section 4.3.3.4/Table 4-12 in the *PCI Express Base Specification (Rev. 2.1)*.

Table 38. PCIe Differential Receiver Specifications

Symbol	Parameter	2.5 Gbps		5.0 Gbps		Unit
		Min.	Max.	Min.	Max.	
UI	Unit interval	399.88	400.12	199.94	200.06	ps
$V_{RX-DIFF-PP-CC}$	Differential Rx peak-peak voltage					
	▪ Common reference clock Rx architecture	0.175	1.2	0.120	1.2	V
	▪ Data clocked Rx architecture	0.175	1.2	0.100	1.2	V
T_{RX-EYE}	Receiver eye time opening	0.40	-	N/A	-	UI
$T_{RX-TJ-CC}$	Maximum Rx inherent timing error					
	▪ Common reference clock Rx architecture	N/A	-	-	0.40	UI
	▪ Data clocked Rx architecture	N/A	-	-	0.34	UI
$T_{RX-DJ-DD-CC}$	Maximum Rx inherent deterministic timing error					
	▪ Common reference clock Rx architecture	N/A	-	-	0.30	UI
	▪ Data clocked Rx architecture	N/A	-	-	0.24	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time delta between median and deviation from median	-	0.3	Not specified		UI
$T_{RX-MIN-PULSE}$	Minimum width pulse at Rx	Not specified		0.6	-	UI
$V_{RX-MAX-MIN-RATIO}$	Minimum/Maximum pulse voltage on consecutive UI	Not specified		-	5	--
$RL_{RX-DIFF}$	Rx package + Si differential return loss					
	▪ 0.05–1.25 GHz	10	-	10	-	dB
	▪ 1.25–2.5 GHz	10	-	8	-	
RL_{RX-CM}	Common mode Rx return loss	6	-	6	-	dB
Z_{RX-DC}	Receiver DC common mode impedance	40	60	40	60	W
$Z_{RX-DIFF-DC}$	DC differential impedance	80	120	Not specified		W
$V_{RX-CM-AC-P}$	Rx AC common mode voltage	-	150	-	150	mV
$Z_{RX-HIGH-IMP-DC-POS}$	DC input common mode input impedance for positive voltage during reset or power down	50k	-	50k	-	W

Table 38. PCIe Differential Receiver Specifications (Cont.)

Symbol	Parameter	2.5 Gbps		5.0 Gbps		Unit
		Min.	Max.	Min.	Max.	
$Z_{RX-HIGH-IMP-DC-NEG}$	DC input common mode input impedance for negative voltage during reset or power down	1.0k	-	1.0k	-	W
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65	175	65	175	mV
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected electrical Idle enter detect threshold integration time	-	10	-	10	ms
$L_{RX-SKEW}$	Lane-to-lane skew	-	20	-	8	ns

3.8.2.2 PCIe Differential Transmitter Specifications

Table 39 lists the main electrical characteristics for the PCIe differential transmitters in the RWM6050. Parameters are defined separately for 2.5 and 5.0Gbps. For more information, see Section 4.3.3.5/Table 4-9 in *PCI Express Base Specification (Rev. 2.1)*.

Table 39. PCIe Differential Transmitter Specifications

Symbol	Parameter	2.5 Gbps		5.0 Gbps		Unit
		Min.	Max.	Min.	Max.	
UI	Unit interval	399.88	400.12	199.94	200.06	ps
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	0.8	1.2	0.8	1.2	V
$V_{TX-DIFF-PP-LOW}$	Low power differential p-p Tx voltage swing	0.4	1.2	0.4	1.2	V
$V_{TX-DE-RATIO-3.5DB}$	Tx de-emphasis level ratio	3.0	4.0	3.0	4.0	dB
$V_{TX-DE-RATIO-6DB}$	Tx de-emphasis level ratio	N/A	N/A	5.5	6.5	dB
$T_{MIN-PULSE}$	Instantaneous lone pulse width	Not specified		0.9	-	UI
T_{TX-EYE}	Transmitter eye including all jitter sources	0.75	-	0.75	-	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	-	0.125	Not specified		UI
$T_{TX-HF-DJ-DD}$	Tx deterministic jitter > 1.5 MHz	Not specified		-	0.15	UI
$T_{TX-LF-RMS}$	TX RMS jitter < 1.5 MHz	Not specified		3.0	-	ps, rms
$T_{TX-RISE-FALL}$	Transmitter rise and fall time	0.125	-	0.15	-	UI
$T_{RF-MISMATCH}$	Tx rise/fall mismatch	Not specified		-	0.1	UI
$RL_{TX-DIFF}$	Tx package + Si differential return loss					
	▪ 0.05–1.25GHz	10	-	10	-	dB
	▪ 1.25–2.5GHz	10	-	8	-	
RL_{TX-CM}	Tx package + Si common mode return loss	6	-	6	-	dB
$Z_{TX-DIFF-DC}$	DC differential Tx impedance	80	120	-	120	W

Table 39. PCIe Differential Transmitter Specifications (Cont.)

Symbol	Parameter	2.5 Gbps		5.0 Gbps		Unit
		Min.	Max.	Min.	Max.	
$V_{TX-CM-AC-PP}$	Tx AC common mode voltage					
	▪ 5.0Gbps	Not specified		-	100	mV
	▪ 2.5Gbps	20	-	Not specified		mV
$I_{TX-SHORT}$	Transmitter short-circuit current limit	-	90	-	90	mA
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	0	3.6	0	3.6	V
$V_{TX-CM-DC-ATIVE-IDLE-DELTA}$	Absolute delta of DC common-mode voltage during L0 and Electrical Idle	0	100	0	100	mV
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common-mode voltage between the differential outputs	0	25	0	25	mV
$V_{TX-IDLE-DIFF\_AC-p}$	Electrical idle differential peak output voltage	0	20	0	20	mV
$V_{TX-IDLE-DIFF\_DC}$	DC electrical idle differential output voltage	Not specified		0	5	mV
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during receiver detection	-	600	-	600	mV
$T_{TX-IDLE-MIN}$	Minimum time spent in electrical idle	20	-	20	-	ns
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an EIOS	-	8	-	8	ns
$T_{TX-IDLE-SET-TO-DIFF-DATA}$	Maximum time to transition to valid differential signaling after leaving electrical idle	-	8	-	8	ns
$T_{CROSSLINK}$	Cross-link random timeout	-	1	-	1	ms
$L_{TX-SKEW}$	Lane-to-lane output skew	-	500 ps + 2 UI	-	500 ps + 2 UI	ps
C_{TX}	AC coupling capacitor	75	200	75	200	nF

4. System Clocking

4.1 System Oscillator

The RWM6050 contains a single 25MHz system XTAL oscillator which provides the reference clock to the two system PLLs.

- When using a resonant crystal, it is connected to SYSOSC_XI and SYSOSC_XO.
- When using a crystal oscillator, it is connected to SYSOSC_XI, and SYSOSC_XO is left unconnected.

4.2 System PLLs

The RWM6050 contains two system PLLs, used to generate all clocks for the system with the exception of the MSFE and PCIe interfaces. The PLL supplies should be separated from the other, noisier, supplies in the board. These supplies should be decoupled close to the respective IC power pins.

4.3 PHY Clocks

The PHY allows considerable flexibility for the RF reference clocks. There must be a single common frequency reference for both the RF device and the RWM6050 PHY. The PHY contains a high-Q crystal oscillator that can generate a frequency reference with low jitter from either a fundamental or third overtone crystal. Alternatively, the PHY may use a frequency reference from an external source or the RF device itself. An external source would be required if fine frequency control is required. The following diagrams show some possible examples.

Figure 17. PHY Clocks – RWM6050 Master, RF Slave

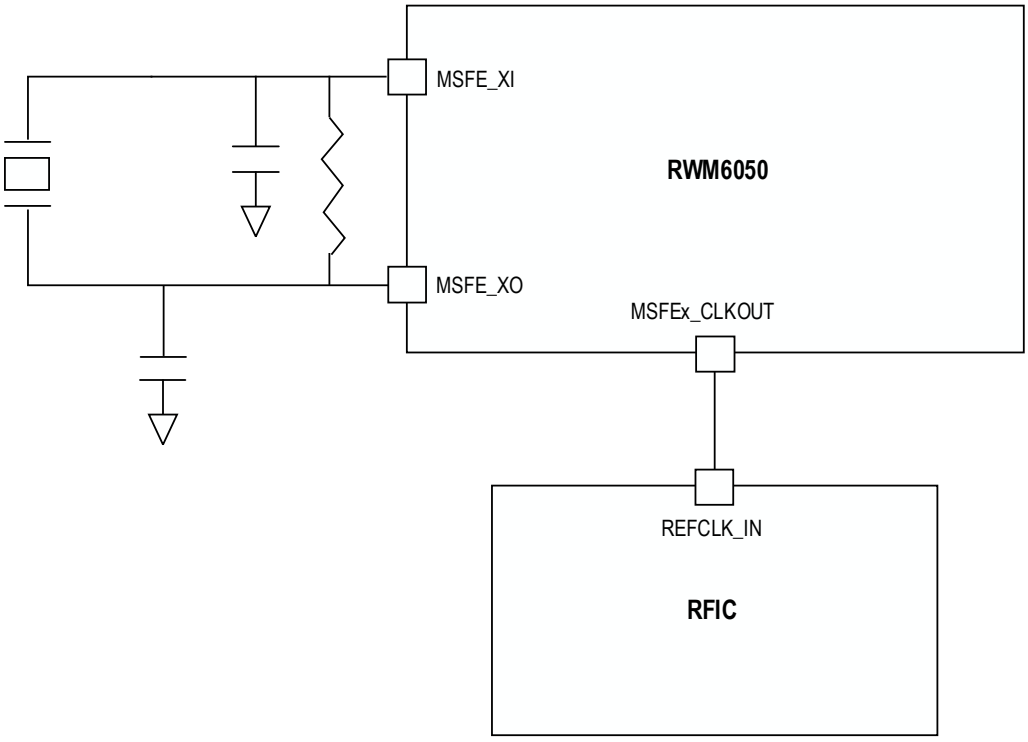


Figure 18. PHY Clocks – RF Master, RWM6050 Slave

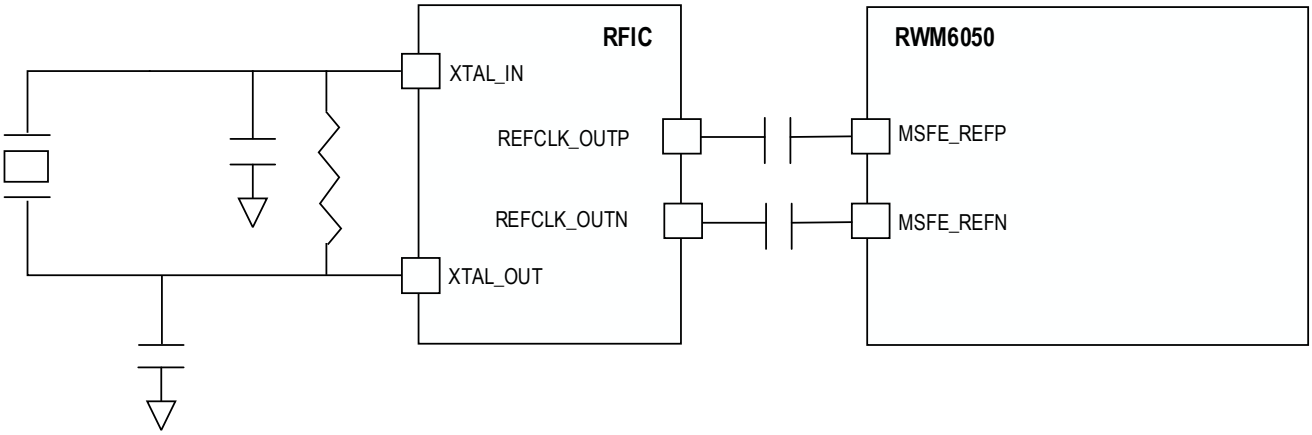
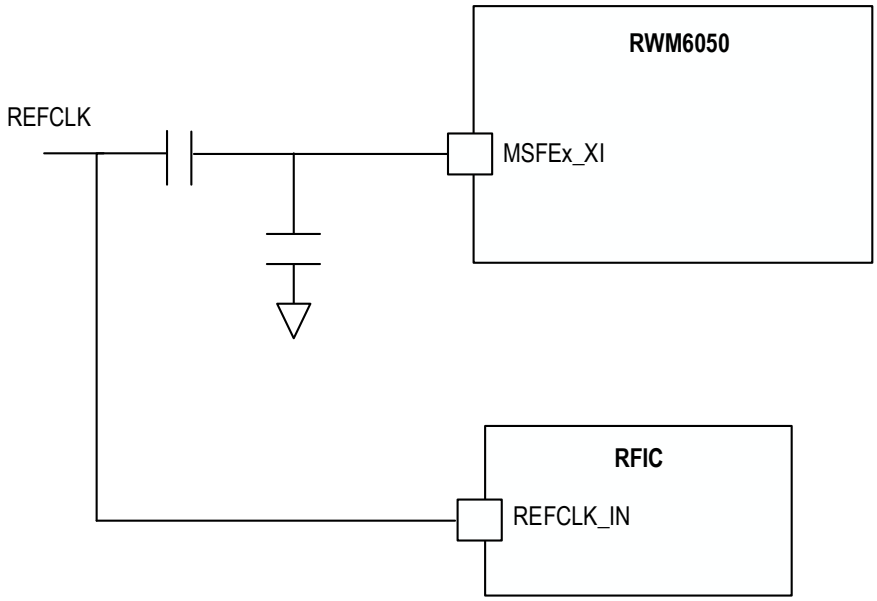


Figure 19. PHY Clocks – RWM6050 and RF Slave



5. Package Specifications

5.1 Package Information

Package information for the RWM6050 is summarized in the following table.

Table 40. Package Information

Specification	Description
Package Code	ALG484
Pb (Lead) Free	Yes - e1 SnAgCu
Package type	FlipChip BGA (FCBGA)
Package Length × Width	19 × 19 mm
Package Thickness - Nominal	2.47mm
Ball pitch	0.8mm
Ball diameter	0.5mm
Ball count	484

5.2 Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

5.3 Thermal Characteristics

Heat generated by the packaged silicon must be removed from the package to ensure the silicon is maintained within its functional and maximum design temperature limits. If heat buildup becomes excessive, the silicon temperature may exceed the temperature limits. A consequence of this is that the silicon may fail to meet the performance specifications and the reliability objectives may be affected.

Failure mechanisms and failure rate of a device has an exponential dependence on the silicon operating temperatures. Therefore, the control of the package, and by extension the junction temperature, is essential to ensure product reliability. The device is specified safe for operation when the junction temperature is within the recommended limits as displayed in Table 14. Table 41 shows the simulated junction to board and case thermal characteristics (Theta JB and Theta JC).

Table 41. Junction to Board/Case Thermal Characteristics (Theta JB/JC)

Interface	Results (^{0}C/Watt)
Theta JB (Junction to Board)	2.74
Theta JC (Junction to Case)	0.466

Table 42 shows the simulated junction to ambient characteristics (Theta JA) of the FCBGA package. The thermal resistance Theta JA characteristics of a package depends on multiple variables other than just the package. In a typical application, designers must consider various system-level and environmental characteristics, such as:

- Package mounting (vertical/horizontal)
- System airflow conditions (laminar/turbulent)
- Heat sink design and thermal characteristics
- Heat sink attachment method
- PWB size, layer count, and conductor thickness
- Influence of the heat dissipating components assembled on the PWB (neighboring effects)

Table 42. Junction to Ambient Thermal Characteristics (Theta JA)

Package	Theta JA Results at Specified Airflow (^{0}C/Watt)		
	0 m/s	1 m/s	2 m/s
FCBGA – No heat sink	13.8	10.34	8.89
FCBGA – With heat sink[a]	9.72	6.7	5.82

[a] Heat sink dimensions: See Table 43.

The simulated results in Table 43 are based on a JEDEC Thermal Test Board configuration (JESD51-9), and do not factor in the system-level characteristics described above. As such, these values are for reference only.

Table 43. With External Heat Sink

Characteristic	Value
Heat sink dimensions	19 × 19 mm
heat sink base thickness	1mm
Fin height	10mm
Thermal grease with conductivity of	25W/m-K

6. Marking Diagram

1. Line 1 is the part number.
2. Line 2:
   - "#" denotes stepping.
   - "YY" is the last two digits of the year, and "WW" is a work week number that the part was assembled.
   - "$" denotes the mark code.

7. Ordering Information

Part Number	Package	Carrier Type	Temperature Range
80RWM6050BALG	19 × 19 mm, 484-FCBGA	Tray	0°C to 70°C
80RWM6050BALGI	19 × 19 mm, 484-FCBGA	Tray	-40°C to 85°C

8. Partner Acknowledgment

HYDRA Technology licensed from BluWireless Technology Ltd.

Revision History

Revision Date	Description of Change
April 14, 2022	▪ Corrected the maximum power numbers for PLLx_VDDH and PLLx_VDDA/PLL_DVDD in Table 15. They were incorrectly swapped in the previous datasheet.
May 25, 2021	▪ Updated the MSFE reference clock to 45MHz from 54MHz.
July 22, 2020	▪ Updated the pin descriptions to match the *RWM6050 BluWireless Reference Design Schematic*, dated June 1, 2020, Rev A01. No electrical functions are affected.
May 22, 2019	▪ Updated “Sampling Clock” in Mixed Signal Front End ▪ Updated the description of RCIx_MOSI[1:3]_S in Table 5 ▪ Updated “Differential input impedance” in Table 31
May 7, 2019	Initial release.