



Tsi RapidIO Switch Device Differences

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1. Tsi RapidIO Switch Device Differences

This document describes the key differences between IDT's third, fourth, and fifth-generation RapidIO switches. The following topics are discussed:

- "Overview" on page 3
- "Hardware Differences" on page 4
- "Register Differences" on page 5
- "Errata Fixes" on page 10

Revision History

80B803A_AN004_02, Formal, August 2009

There have been no technical changes to this document. The formatting was updated to reflect IDT.

80B803A_AN004_01, Formal, January 2009

This was the first version of the *Tsi RapidIO Switch Device Differences Application Note*.

1.1 Overview

IDT continues to increase the features and functionality of its RapidIO switches with each successive generation. IDT's fourth-generation (Tsi620) and fifth-generation (Tsi577) RapidIO switches incorporate a number of improvements over IDT's third-generation switches (see [Table 1](#)). This document describes the key improvements between these generations.

Table 1: IDT's RapidIO Switches

Switch	Switch Generation	RapidIO Interface Capability
Tsi572	Third	Two 4x mode ports or Four 1x mode ports Up to eight 1x mode ports
Tsi574	Third	Four 4x mode ports Up to eight 1x mode ports
Tsi576	Third	Two 4x mode ports + Eight 1x mode ports Up to 12 1x mode ports
Tsi578	Third	Eight 4x mode ports Up to 16 1x mode ports

Table 1: IDT's RapidIO Switches (Continued)

Switch	Switch Generation	RapidIO Interface Capability
Tsi577	Fifth	Four 4x mode ports Up to 16 1x mode ports
Tsi620	Fourth	Three 4x mode ports + FPGA Interface Up to six 1x mode ports

1.2 Hardware Differences

There are four main hardware differences between the third-generation RapidIO switches and the new generations. The first two differences (P_CLK and CLK_SEL) were first implemented in the Tsi620, and then ported to the Tsi577. The other two differences are specific to the Tsi577 and Tsi620.

1.2.1 P_CLK Signal Not Required

All of the third-generation RapidIO switches require a P_CLK signal, which is used to drive the internal register bus, some RapidIO timeout counters, and the low-speed interfaces such as I²C. In some cases, supplying the P_CLK signal required additional board components.

The fourth and fifth generations of RapidIO switches do not require a P_CLK signal. Instead, the frequency of the RapidIO reference clock signal, S_CLK_p/n, is divided down internally to drive the functionality that P_CLK previously offered.

1.2.2 CLK_SEL Signal Added

While the third-generation RapidIO switches make use of a variety of RapidIO reference clock frequencies, including 156.25 MHz and 125 MHz, there is no method for these devices to communicate the reference frequency to software.

The fourth and fifth generations of RapidIO switches have a CLK_SEL signal that indicates whether a 156.25 MHz or 125 MHz reference clock is in use. The CLK_SEL signal is incorporated into the SerDes clocking scheme, which allows the same register values to select a specific lane rate, regardless of reference clock frequency.

The registers affected by the new CLK_SEL signal include:

- Tsi577
 - GLOB_PWRUP_STAT[CLK_SEL]
 - SMACx_DLOOP_CLK_SEL[IO_SPEED]
- Tsi620
 - CG_RIO_PWRUP_STATUS[SP_REF_CLK]
 - SMACx_DLOOP_CLK_SEL[IO_SPEED]

1.2.3 Tsi577 4x/4 1x Ports

In all third-generation RapidIO switches, and the Tsi620, a 4x RapidIO port can be divided into two 1x RapidIO ports. If only one of the 1x ports is needed, it must be the evenly numbered port since powering down the evenly numbered port also disables the odd numbered port.

In contrast, the Tsi577 allows a 4x port to be divided into four 1x RapidIO ports. Any unused 1x ports can be powered down without affecting the operation of other ports. The Tsi577 registers are backward compatible with software designed for third-generation switches.

1.2.4 Tsi620 FPGA Interface

The Tsi620 incorporates an FPGA Interface that is based on the XGMII standard. The FPGA Interface is a parallel interface that supports the RapidIO protocol. In effect, the FPGA Interface implements the RapidIO link without a SerDes, which allows the use of less expensive FPGAs.

1.3 Register Differences

There are a few register differences between the third-generation and the fourth/fifth generations of RapidIO switches. Drivers written for third-generation RapidIO switches, however, will operate correctly on the latest switch generations. The fourth- and fifth-generation switches contain additional registers, and offer some functionality enhancements.



Many of the register enhancements in the Tsi577 (fifth generation) were first implemented in the Tsi620 (fourth generation).

Various registers were added to the fourth- and fifth-generation switches. These registers, however, do not impact the compatibility of the latest generation devices with the third-generation. The new grouping of registers include the following:

- “Per Port Copies of Global Registers” on page 6
- “Global Power-up Status Registers” on page 8

1.3.1 Per Port Copies of Global Registers

In the fourth/fifth generation of MAC interfaces, some global registers also have local copies in each RapidIO port. These registers allow read/write access to the per port copies of the global registers.



Per port copies of global registers are used to check/correct register values after a port is powered down and back up. They are not intended to be the standard method for programming these registers. However, if users prefer to include the local copies of the registers into their programming model, they are not prohibited from doing so.

New registers include the following:

- RapidIO Port x Multicast Write ID 0/1/2/3/4/5/6/7
 - Description: These registers are per port copies of the RapidIO Multicast Write ID x register, where “x” is 0/1/2/3/4/5/6/7. The RapidIO Multicast Write ID x register contains the Multicast ID for which the associated multicast mask registers are applicable. The switch supports eight multicast groups, therefore, the Multicast ID registers for each multicast group must contain unique values. These registers are located in every switch port.
 - RapidIO Port x Multicast Write ID 0 Offsets: 16000, 16100, ...16F00
 - RapidIO Port x Multicast Write ID 1 Offsets: 16004, 16104, ...16F04
 - RapidIO Port x Multicast Write ID 2 Offsets: 16008, 16108, ...16F08
 - RapidIO Port x Multicast Write ID 3 Offsets: 1600C, 1610C, ...16F0C
 - RapidIO Port x Multicast Write ID 4 Offsets: 16010, 16110, ...16F10
 - RapidIO Port x Multicast Write ID 5 Offsets: 16014, 16114, ...16F14
 - RapidIO Port x Multicast Write ID 6 Offsets: 16018, 16118, ...16F18
 - RapidIO Port x Multicast Write ID 7 Offsets: 1601C, 1611C, ...16F1C
- RapidIO Port x Switch Port Link Timeout Control CSR
 - Description: This register is the per port copy of the RapidIO Switch Port Link Time Out Control CSR.
 - Offsets: 16020, 16120, ...16F20
- RapidIO Port x Port Write Target Device ID CSR
 - Description: This register is the per port copy of the RapidIO Port Write Target Device ID CSR.
 - Offsets: 16028, 16128, ...16F28
- RapidIO Port x Packet Time-to Live CSR
 - Description: This register is the per port copy of the RapidIO Packet Time-to Live CSR.
 - Offsets: 1602C, 1612C, ...16F2C
- RapidIO Port x Switch Port General Control CSR

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- Description: This register is the per port copy of the RapidIO Switch Port General Control CSR.
 - Offsets: 1613C, 1623C, ...16F3C
 - RapidIO Port x Component Tag CSR
 - Description: This register is the per port copy of the RapidIO Component Tag CSR
 - Offsets: 1606C, 1616C, ...16F6C
 - RapidIO Port x Route LUT Attributes (Default Port) CSR
 - Description: This register is the per port copy of the RapidIO Route LUT Attributes (Default Port) CSR
 - Offsets: 16078, 16178, ...16F78
 - RapidIO Port x Logical and Transport Layer Error Enable CSR
 - Description: This register is the per port copy of the RapidIO Logical and Transport Layer Error Enable CSR
 - Offsets: 1607C, 1617C, ...16F7C

1.3.2 Global Power-up Status Registers

In many cases it is useful for configuration software to know the power-up status configuration of a switch. This allows communication of the device's location within a system, and customization of the device's initialization based on its location.

1.3.2.1 Tsi620

The Tsi620 incorporates two global power-up status registers (for more information about these registers, see the *Tsi620 User Manual*). This register shows the status of the Tsi620 RapidIO power-up configuration.

Register name: CG_RIO_PWRUP_STATUS Reset value: Undefined	Register offset: 0x034
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Bits	7	6	5	4	3	2	1	0
31:24	SP_MAST_EN	SP_HOST	SP_TX_SWAP	SP_RX_SWAP	SP_REF_CLK		SP_IO_SPEED	
23:16	Reserved				SP6_MODE	SP4_MODE	SP2_MODE	SP0_MODE
15:08	Reserved							
07:00	Reserved	SP6_PWRDN	SP5_PWRDN	SP4_PWRDN	SP3_PWRDN	SP2_PWRDN	SP1_PWRDN	Reserved

Register name: CG_PWRUP_STATUS Reset value: Undefined	Register offset: 0x038
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Bits	7	6	5	4	3	2	1	0
31:24	Reserved						VARIANT	
23:16	Reserved			PCI_HOLD_BOOT	PCI_ARBEN	PCI_RSTDIR	PCI_M66EN	PCI_PLL_BYPASS
15:08	Reserved				I2C_SEL	I2C_DISABLE	I2C_SLAVE	I2C_MA
07:00	Reserved	I2C_SA[6:0]						

1.3.2.2 Tsi577

The Tsi577 has one register that contains the power-up configuration of the switch (for more information about this register, see the *Tsi577 User Manual*).

Register name: GLOB_PWRUP_STAT Reset value: Undefined	Register offset: 1AC10
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Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved							CLK_SEL

Bits	Name	Description	Type	Reset Value
0:30	Reserved	N/A	R	0
31	CLK_SEL	Clock Select. 1 = 125-MHz Reference clock 0 = 156.25-MHz Reference clock The reset value of this field is dependent upon the SP_CLK_SEL signal.	R	undefined

1.3.2.3 Congestion Detection Enhancement (Tsi577 only)

In the Tsi577, the receiver and transmitter queue threshold control registers are enhanced to allow the detection of continuous congestion events that occur over a longer period than what third-generation switches can detect.

Third-generation switches can detect continuous congestion for up to 210 microseconds. The Tsi577 can detect continuous congestion for up to 107 milliseconds, which allows detection and diagnosis of system failures.

1.4 Errata Fixes

The Tsi577 and Tsi620 incorporate fixes for a subset of errata that are applicable to IDT's third-generation switches.

Table 2: Errata Fixed in Fourth- and Fifth-generation Switches

Errata	Fixed in Tsi620	Fixed in Tsi577
Host Base Device ID Register Locks with 0xFFFF	-	Yes
Multicast Control Symbol Loss	Yes	Yes
Exceeding Error Threshold Limit	-	Yes
Performance Statistics Counter Outbound Measurement	-	Yes
Error Rate Counter Limitation	-	Yes
4x Port in 1x Mode Transmission on Lane 0 and Lane 2 Issue	-	Yes
Lookup Table Parity Data Not Logged	-	Yes
Port N Logical Errors Not Captured when PW_DIS = 1	-	Yes