Tsi578 Ballmap (Document number 80B803A_PN003_04)

Note: This is the ballmap when looking through the top of the package. This ballmap represents the PCB footprint for the Tsi578.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	NO_BALL	VSS	VSS	VSS	VSS	VSS	SP14_TD_P	VSS	SP14_TC_N	VSS	SP14_TB_P	VSS	SP14_TA_N	VSS	SP6_TD_P	VSS	SP6_TC_N	VSS	SP6_TB_P	VSS	SP6_TA_N	VSS	VSS	VSS	VSS	VSS
B	VSS	SP_VDD	VSS	VSS	VSS	VSS	SP14_TD_N	VSS	SP14_TC_P	SP_VDD	SP14_TB_N	VSS	SP14_TA_P	SP_VDD	SP6_TD_N	VSS	SP6_TC_P	SP_VDD	SP6_TB_N	VSS	SP6_TA_P	SP_VDD	VSS	S_CLK_P	S_CLK_N	VSS
C	SP0_TA_N	SP0_TA_P	SP_VDD	SP0_RA_P	SP0_RA_N	SP_VDD	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	VSS	REF_AVDD	VSS	REF_AVDD
D	VSS	VSS	VSS	VSS	SP_VDD	VSS	SP14_RD_N	VSS	SP14_RC_P	SP14_REXT	SP14_RB_N	VSS	SP14_RA_P	VSS	SP6_RD_N	VSS	SP6_RC_P	SP6_REXT	SP6_RB_N	VSS	SP6_RA_P	VSS	VSS	VSS	VSS	VSS
E	SP0_TB_P	SP0_TB_N	SP_VDD	SP0_RB_N	SP0_RB_P	SP_VDD	SP14_RD_P	SP14_AVDD	SP14_RC_N	SP14_AVDD	SP14_RB_P	SP_VDD	SP14_RA_N	VSS	SP6_RD_P	SP6_AVDD	SP6_RC_N	SP6_AVDD	SP6_RB_P	SP_VDD	SP6_RA_N	VSS	VSS	VSS	VSS	VSS
F	VSS	SP_VDD	VSS	SP0_REXT	SP0_AVDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	VSS	VSS	VSS	VSS
G	SP0_TC_N	SP0_TC_P	SP_VDD	SP0_RC_P	SP0_RC_N	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	SP_VDD	SP12_RD_P	SP12_RD_N	SP_VDD	SP12_TD_N	SP12_TD_P
H	VSS	VSS	VSS	VSS	SP0_AVDD	VSS	SP_VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SP_VDD	VSS	SP12_AVDD	VSS	VSS	VSS	VSS
J	SP0_TD_P	SP0_TD_N	SP_VDD	SP0_RD_N	SP0_RD_P	SP_VDD	VSS	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	SP_VDD	SP12_RC_N	SP12_RC_P	SP_VDD	SP12_TC_P	SP12_TC_N
K	VSS	SP_VDD	VSS	VSS	VSS	VSS	SP_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	SP_VDD	VSS	SP12_AVDD	SP12_REXT	VSS	SP_VDD	VSS
L	SP8_TA_N	SP8_TA_P	SP_VDD	SP8_RA_P	SP8_RA_N	SP_VDD	VSS	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	SP_VDD	SP12_RB_P	SP12_RB_N	SP_VDD	SP12_TB_N	SP12_TB_P
M	VSS	VSS	VSS	VSS	SP_VDD	VSS	SP_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	SP_VDD	VSS	SP_VDD	VSS	VSS	VSS	VSS
N	SP8_TB_P	SP8_TB_N	SP_VDD	SP8_RB_N	SP8_RB_P	SP_VDD	VSS	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	SP_VDD	SP12_RA_N	SP12_RA_P	SP_VDD	SP12_TA_P	SP12_TA_N
P	VSS	SP_VDD	VSS	SP8_REXT	SP8_AVDD	VSS	SP_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	SP_VDD	VSS	VSS	VSS	VSS	SP_VDD	VSS
R	SP8_TC_N	SP8_TC_P	SP_VDD	SP8_RC_P	SP8_RC_N	SP_VDD	VSS	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	SP_VDD	SP4_RD_P	SP4_RD_N	SP_VDD	SP4_TD_N	SP4_TD_P
T	VSS	VSS	VSS	VSS	SP8_AVDD	VSS	SP_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	I2C_SA[0]	SP_VDD	VSS	SP4_AVDD	VSS	VSS	VSS	VSS
U	SP8_TD_P	SP8_TD_N	SP_VDD	SP8_RD_N	SP8_RD_P	SP_VDD	VSS	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	I2C_SA[1]	VSS	SP_VDD	SP4_RC_N	SP4_RC_P	SP_VDD	SP4_TC_P	SP4_TC_N
V	VSS	VDD_IO	VSS_IO	VSS	VSS_IO	VDD_IO	SP_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	BCE	SP_VDD	VSS	SP4_AVDD	SP4_REXT	VSS	SP_VDD	VSS
W	VSS_IO	SP4_PWRDN	SP5_PWRDN	VDD_IO	SP6_PWRDN	SP7_PWRDN	SP14_PWRDN	VSS_IO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS_IO	I2C_SEL	SP_VDD	SP4_RB_P	SP4_RB_N	SP_VDD	SP4_TB_N	SP4_TB_P
Y	SP8_PWRDN	VDD_IO	SP9_PWRDN	SP10_PWRDN	VSS_IO	SP11_PWRDN	VDD_IO	SP15_PWRDN	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS_IO	SP_RX_SWAP	SP_TX_SWAP	VSS	SP_VDD	VSS	VSS	VSS	VSS
AA	VSS_IO	SP12_PWRDN	SP13_PWRDN	VDD_IO	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	SP_VDD	SP4_RA_N	SP4_RA_P	SP_VDD	SP4_TA_P	SP4_TA_N
AB	SP4_MODESEL	VDD_IO	SP8_MODESEL	SP8_MODESEL	VSS_IO	SP2_RA_N	SP_VDD	SP2_RB_P	SP2_AVDD	SP2_RC_N	SP2_AVDD	SP2_RD_P	VSS	SP10_RA_N	SP_VDD	SP10_RB_P	SP10_AVDD	SP10_RC_N	SP10_AVDD	SP10_RD_P	VSS	VSS	VSS	VSS	SP_VDD	VSS
AC	VSS_IO	INT_B	SP10_MODESEL	VDD_IO	VSS	SP2_RA_P	VSS	SP2_RB_N	SP2_REXT	SP2_RC_P	VSS	SP2_RD_N	VSS	SP10_RA_P	VSS	SP10_RB_N	SP10_REXT	SP10_RC_P	VSS	SP10_RD_N	VSS	SP_IO_SPEED[0]	SP_IO_SPEED[1]	I2C_DISABLE	VDD_IO	TMS
AD	N/C	VDD_IO	SW_RST_B	N/C	VSS_IO	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS_IO	SP0_MODESEL	SP2_MODESEL	MCES	TDO	TDI
AE	VSS_IO	N/C	VSS	VDD_IO	SP_VDD	SP2_TA_P	VSS	SP2_TB_N	SP_VDD	SP2_TC_P	VSS	SP2_TD_N	SP_VDD	SP10_TA_P	VSS	SP10_TB_N	SP_VDD	SP10_TC_P	VSS	SP10_TD_N	VSS	I2C_MA	SP2_PWRDN	I2C_SD	VDD_IO	TRST_B
AF	P_CLK	HARD_RST_B	SP12_MODESEL	SP14_MODESEL	VSS	SP2_TA_N	VSS	SP2_TB_P	VSS	SP2_TC_N	VSS	SP2_TD_P	VSS	SP10_TA_N	VSS	SP10_TB_P	VSS	SP10_TC_N	VSS	SP10_TD_P	VSS_IO	SP1_PWRDN	SP3_PWRDN	VSS_IO	I2C_SCLK	TCK

Legend

- VSS and VSS_IO
- VDD and VDD_IO
- Miscellaneous
- No Ball and No Connect
- JTAG
- SP_VDD and SPx_AVDD
- S_CLK_x
- Serial RapidIO Interface 0
- Serial RapidIO Interface 2
- Serial RapidIO Interface 4
- Serial RapidIO Interface 6
- Serial RapidIO Interface 8
- Serial RapidIO Interface 10
- Serial RapidIO Interface 12
- Serial RapidIO Interface 14

Copyright © August 2009 Integrate Device Technology (IDT). All rights reserved. Published in Canada.

Disclaimer: IDT assumes no responsibility for the accuracy or completeness of the information presented, which is subject to change without notice. In no event will IDT be liable for any direct, indirect, special, incidental or consequential damages, including lost profits, lost business or lost data, resulting from the use of or reliance upon the information, whether or not IDT has been advised of the possibility of such damages. Mention of non-IDT products or services is for information purposes only and constitutes neither an endorsement nor a recommendation.

Revision History

August 2009, 80B803A_PN003_04 -- No technical changes. Formatting was changed to reflect IDT