Title Page

PCIe2 to S-RIO2 Bridging + Switching Evaluation Platform

TITLE : TITLE PAGE			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
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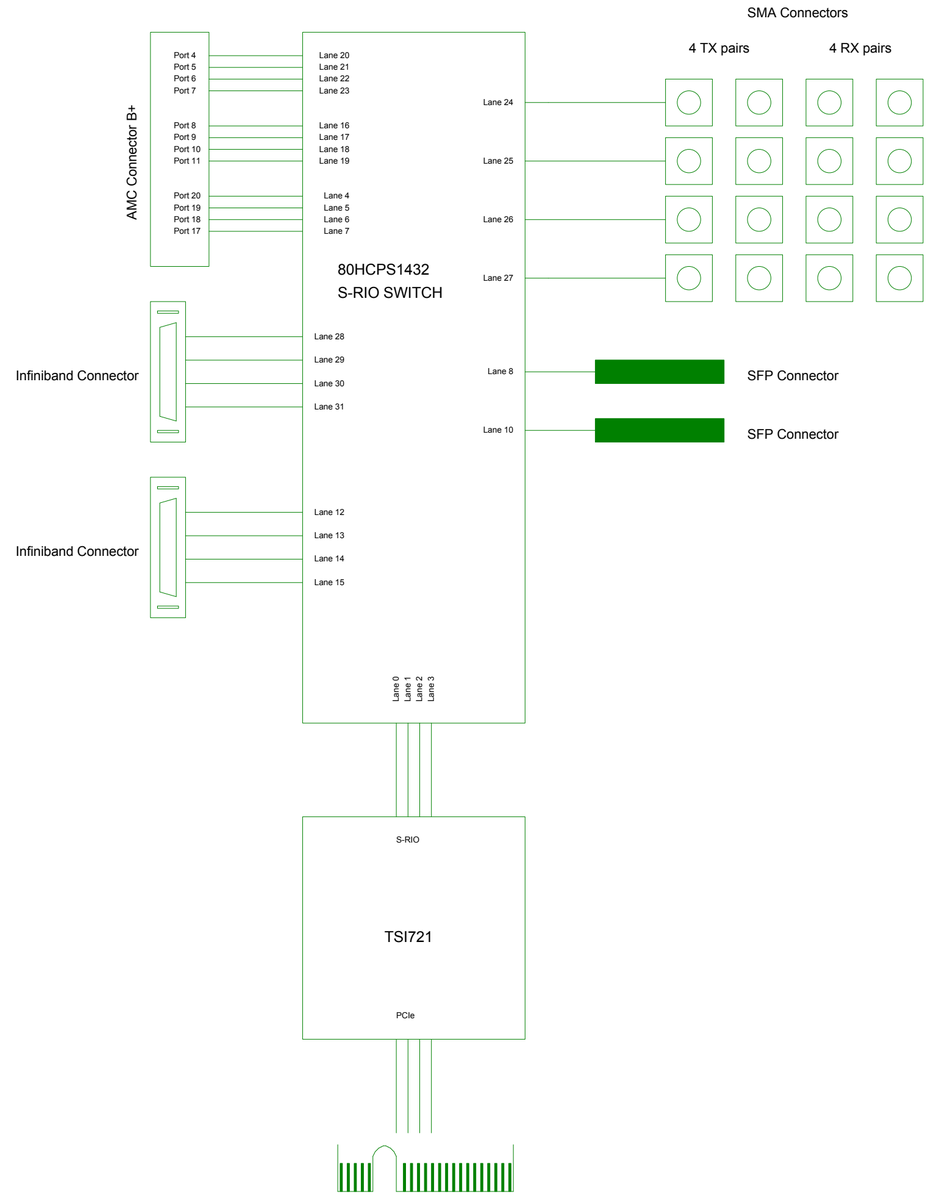
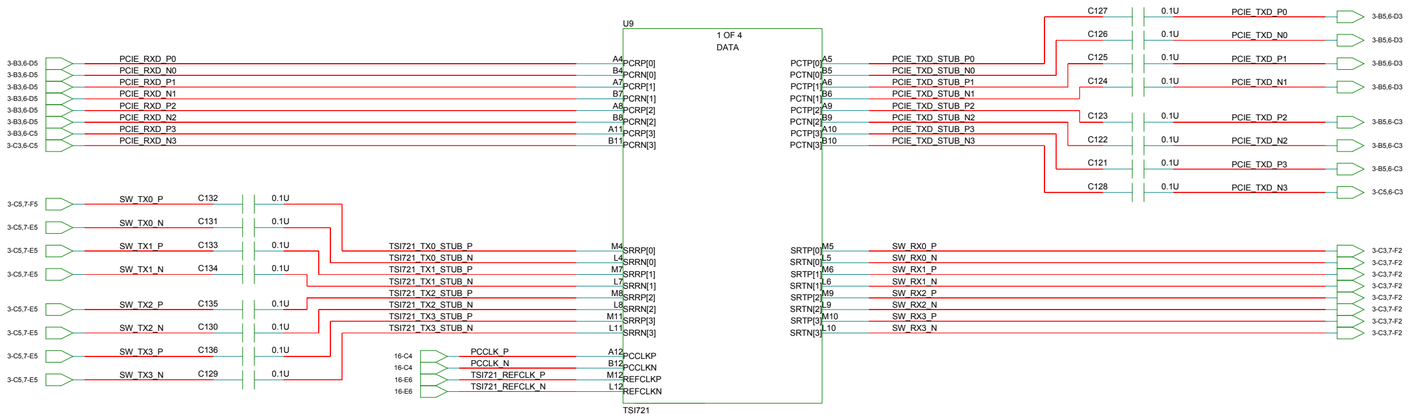
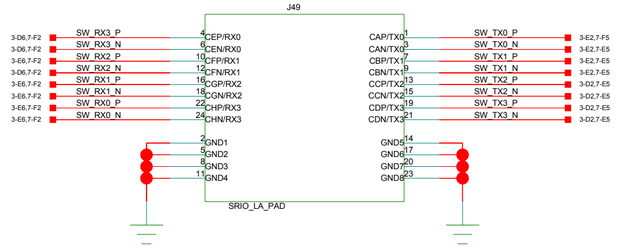
Block Diagram

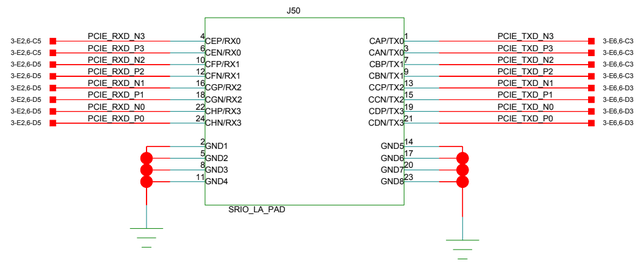


TITLE : BLOCK DIAGRAM			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 30-08-2011_13:30	SHEET 2 OF 21		

Tsi721 Serial Links







TITLE : TSI721 SERIAL LINKS

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C			

LAST MODIFIED DATE : 18-06-2012_15:03

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Tsi721 Configs

GPIO (User) LED
Interrupt Pending LED
PCIE link active LED
ERROR LED
3.3V
R26 300
R25 300
R24 300
R23 300
D2
D19
D1
D8
HSMG-C150
HSMY-C150
HSMG-C150
HSMH-C150

TSI721_I2C_A0

FET Switches

S4.1: I2C_SA0
S4.2: I2C_SA1
S4.3: I2C_SA2
S4.4: I2C_SA3

S1.1: I2C_Disable loading
S1.2: I2C_Address Select
S1.3: I2C_boot mode
S1.4: SRIO Host/Slave mode

R93 10K
R92 10K
R91 10K
R90 10K
S4
97C04ST

R97 10K
R96 10K
R95 10K
R94 10K
S1
97C04ST

U18
U19
SN74CBTLV3257
VCC 16
GND 8
1A 4
2A 7
3A 9
4A 12
1B1 2
1B2 3
2B1 5
2B2 6
3B1 11
3B2 10
4B1 14
4B2 13
S 1
OE# 15

C330 0.1U
C331 0.1U

TP7
TP9
TP8
TP10
TP12
TP11

R9 100
R10 100
R11 100
R12 100
R13 100
R14 100
R15 100
R16 100
R1 100
R2 100
R3 100

R41 10K
R42 10K
R40 10K

U9
4 OF 4
MISC
GPIO[0]-I2C_SA[0]
GPIO[1]-I2C_SA[1]
GPIO[2]-I2C_SA[2]
GPIO[3]-I2C_SA[3]
GPIO[4]-I2C_DISABLE
GPIO[5]-I2C_SEL
GPIO[6]-I2C_MA
GPIO[7]-SP_SWAP_RX
GPIO[8]-SP_SWAP_TX
GPIO[9]-SP_HOST
GPIO[10]-SP_DEVID
GPIO[11]-CLKSEL[0]
GPIO[12]-CLKSEL[1]
GPIO[13]
GPIO[14]
GPIO[15]
SR_BOOT
STRAP_RATE[0]
STRAP_RATE[1]
STRAP_RATE[2]
CLKMOD
RSTN
TSI721

I2C_SDA
I2C_SCL
M1
L1

TSI721_I2C_A1
U16
AT24C64B-10TU-18
A2
A1
A0
SDA
SCL
WP
VCC 8
GND 4
C137 0.1U

R51 10K
R52 10K
8-E6,11-B3,16-A2,17-D7
8-E6,11-B3,16-A2,17-D7

TDO D11
TCK E11
TDI F11
TMS H11
TRSTN J11
TSI721_TDO
JTAG_TCK
JTAG_TDI
JTAG_TMS
TSI721_TRST
8-A2,17-A2
8-A2,17-A3,17-E6
17-A3,17-E6
8-A2,17-A3,17-E6

U31
NC7SZ08
VCC5
GND 3
JTAG_TRST
BOARD_RESET
8-A2,17-A3,17-E6
4-C1,8-D3,11-E1,21-C6

TEST_BCE E12
TEST_BIDIR_CTL G12
TEST_ON F12
R20 DNP 0
R21 DNP 0
J26
69190-102H
DNP

MECS M2
TP13
SRRSTON J12
PCRSTON D12
D9
D10
HSMH-C150
R27 300
R28 300

4-C7,8-D3,11-E1,21-C6
BOARD_RESET
Sense threshold 0.5V
U26
TL7700
SENSE 2
CT 1
GND 4
VCC 5
RESET 6
NC1 3
NC2 7
NC3 8
NC
C329 0.1U
C45 0.1U
R98 10K
DELAYED_BOARD_RESET

Delay set to 1ms

S3.1: S-RIO Device ID control
S3.2: Clock Frequency select 0
S3.3: Clock Frequency select 1
S3.4: S-RIO Link training mode

S2.1: S-RIO Link Rate[0]
S2.2: S-RIO Link Rate[1]
S2.3: S-RIO Link Rate[2]
S2.4: PCI Express Clocking Mode

S3
S2
97C04ST
R8 10K

3.3VSB
U10 DNP
74LVC1G125
VCC 5
OE#1
A2
GND3
Y 4
6-E5
PCIE_WAKE
R99 10K
R100 10K

IDT

TITLE : TSI721 CONFIGS			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
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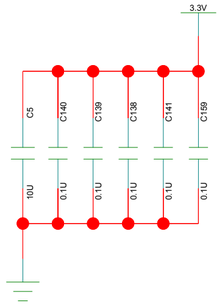
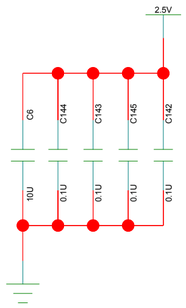
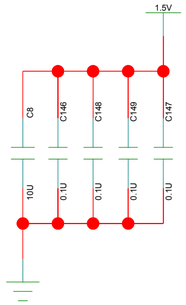
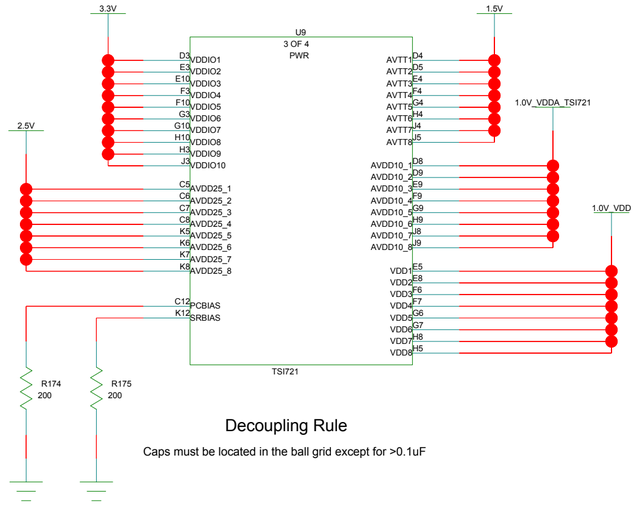
Tsi721 Power



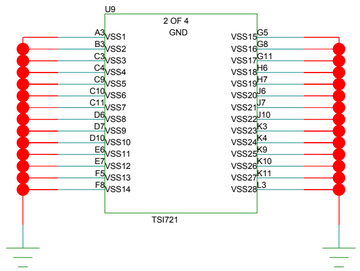




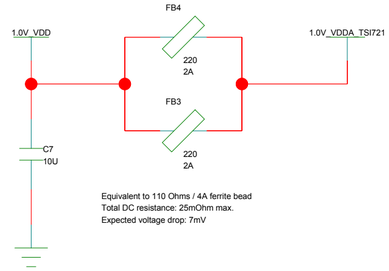


Decoupling Rule

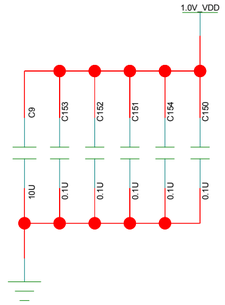
Caps must be located in the ball grid except for >0.1uF

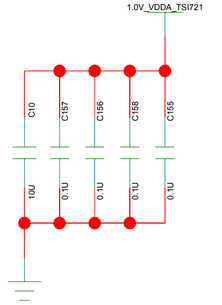


Make two seperate power planes: 1.0V_VDD and 1.0V_VDDA_Tsi721



Equivalent to 110 Ohms / 4A ferrite bead
Total DC resistance: 25mOhm max.
Expected voltage drop: 7mV





TITLE : TSI721 POWER			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
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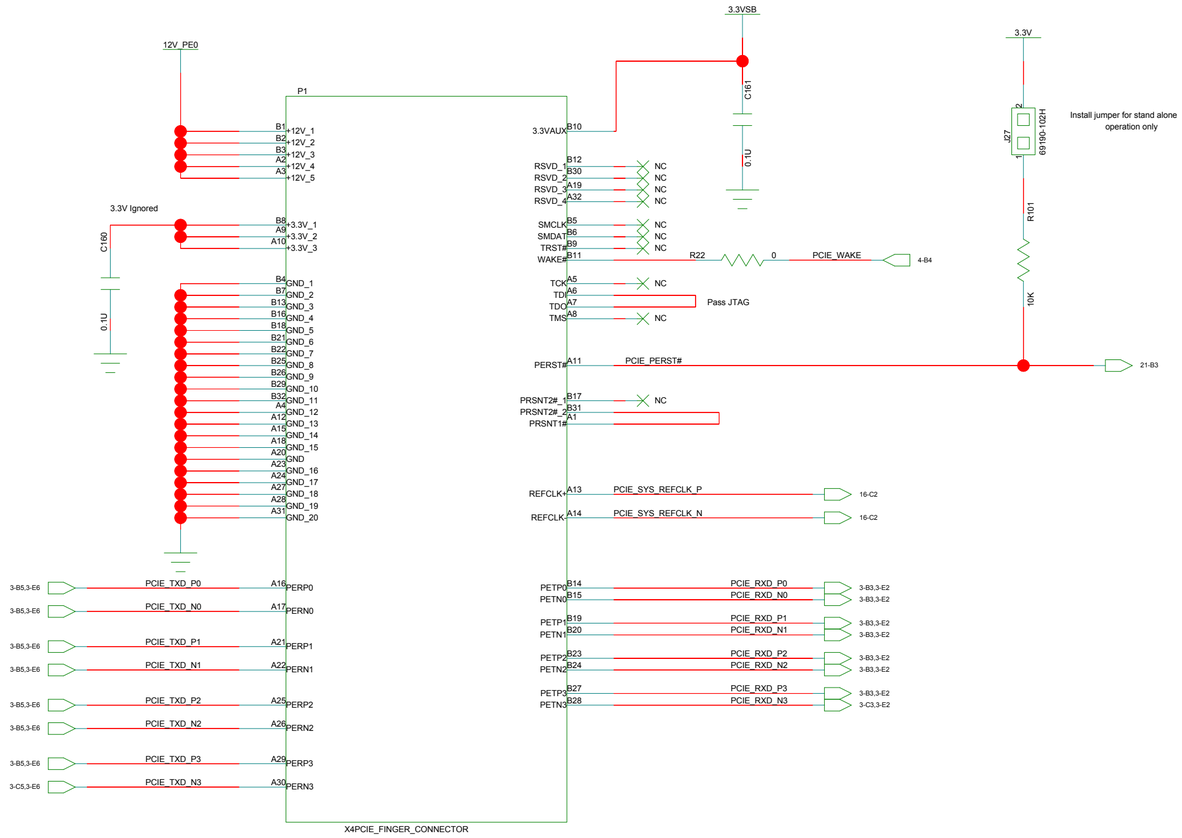
PCI Express Connector



IDT

TITLE : PCI EXPRESS CONNECTOR

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C			

LAST MODIFIED DATE : 07-09-2011_13:17

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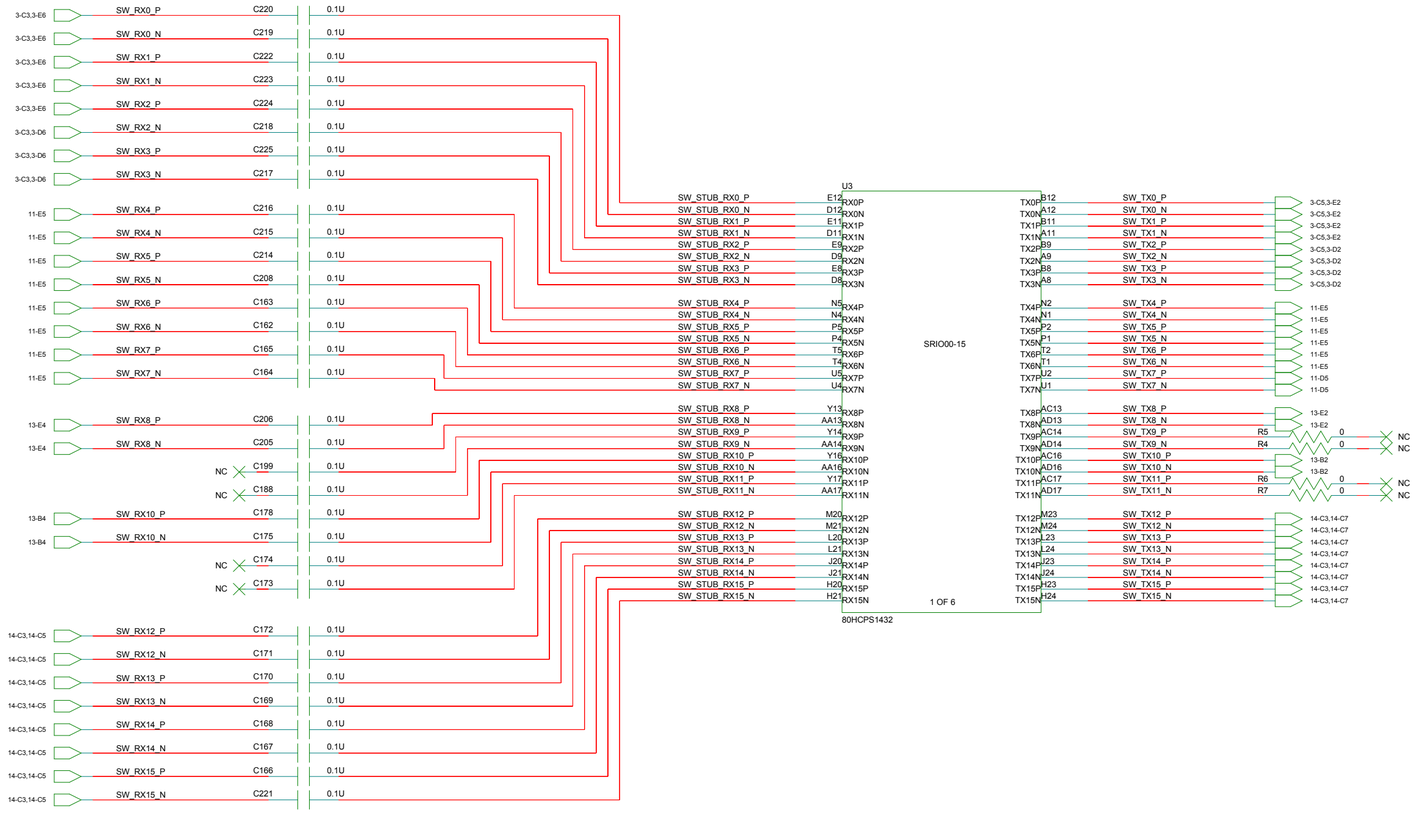
CPS1432 Serial Links



TITLE : CPS1432 SERIAL LINKS

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C			

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CPS1432 Configs

I2C address 0x60

3.3V

R65 DNP 10K
R62 DNP 10K
R64 DNP 10K
R70 DNP 10K
R71 10K
R69 10K
R66 DNP 10K
R68 10K
R61 10K
R67 10K
R63 10K

U17
A2 3
A1 2
A0 1
SDA 5
SCL 6
WP 7
VCC 8
GND 4
AT24C64B-10TU-18
C226
0.1U

R55 10K
R54 10K

SDA B20
SCL A21
SW_SDA
SW_SCL

J28 69190-102H
I2C_SDA
4-D7,11-B3,16-A2,17-D7

J29 69190-102H
I2C_SCL
4-C7,11-B3,16-A2,17-D7

U3

S7 97C04ST OPEN

R134 0
R136 DNP 0
R135 DNP 0
R137 0
R131 0
R130 0
R132 0

A20 ID0
B23 ID1
A23 ID2
B22 ID3
A22 ID4
B21 ID5
E24 ID6
D24 ID7
B24 ID8
C23 ID9
C24 ADS
D23 MM#

J31 69190-102H

QCFG have internal pull ups

S5 97C04ST OPEN
S6 97C04ST OPEN

QCFG0 AA2
QCFG1 AB1
QCFG2 AB2
QCFG3 AC1
QCFG4 AC2
QCFG5 AD2
QCFG6 AC3
QCFG7 AD3

MISC

R60 10K
R59 10K
R58 10K

AC24 SPD0
AD23 SPD1
AD22 SPD2
Y1 FSEL0
Y2 FSEL1
AD4 MCAST

S8 97C04ST OPEN
R133 DNP 0

16-B5 SW_REFCLK_P
16-B5 SW_REFCLK_N
AA24 REF_CLKP
Y24 REF_CLKN

4-C1,4-C7,11-E1,21-C6 BOARD_RESET
AA1 RST#

D1 TCK
C2 TDI
A2 TMS
B2 TRST#

REXTP AB21
REXTN AA21
R186 9.1K

IRQ# C1
TDO B1

DNC_AC4 AC4 NC
DNC_AD5 AD5 NC
DNC_AA22 AA22 NC
DNC_AB22 AB22 NC

3 OF 6
80HCPS1432

U32
VCC 5
GND 3
NC7SZ08

R53 10K

J24 54101-T06-01 DNP

U11
VCC 5
1OE# 1
2A 2
3GND 3
Y4 4
74LVC1G125

R29 300
D17 LTST-C190EKT
Orange LED

MCAST is rising edge triggered

D13 S1B

U5
VCC 5
1OE# 1
2A 2
3GND 3
Y4 4
74LVC1G125

J30 69190-102H

This header is for an external pulse generator

2K R41
2K R40
2K R39
2K R42

8-A3 SW_TRST
8-A3 SW_TDI
8-A3 SW_TDO
8-A3 SW_TMS
8-A3 SW_TCK

R164 33.2

J46 N2510-6002-RB

4-C6,17-A2 TSI721_TDO R126 DNP 0 SW_TDI 8-B3
17-A2 CPS1432_TDO R129 0 SW_TDO 8-B3

4-C6,17-A3,17-E6 JTAG_TMS R127 DNP 0 SW_TMS 8-B3
4-C7,17-A3,17-E6 JTAG_TRST R128 DNP 0 SW_TRST 8-B3
4-C6,17-A3,17-E6 JTAG_TCK R125 DNP 0 SW_TCK 8-B3

IDT

TITLE : CPS1432 CONFIGS			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
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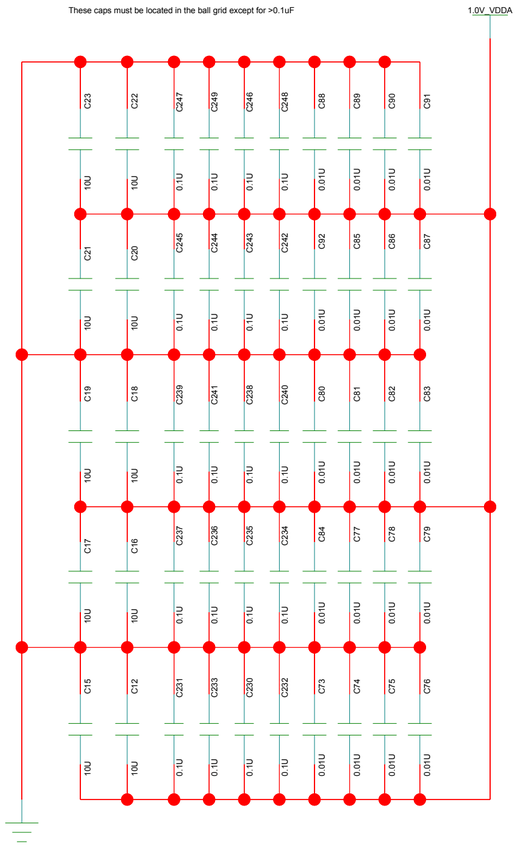
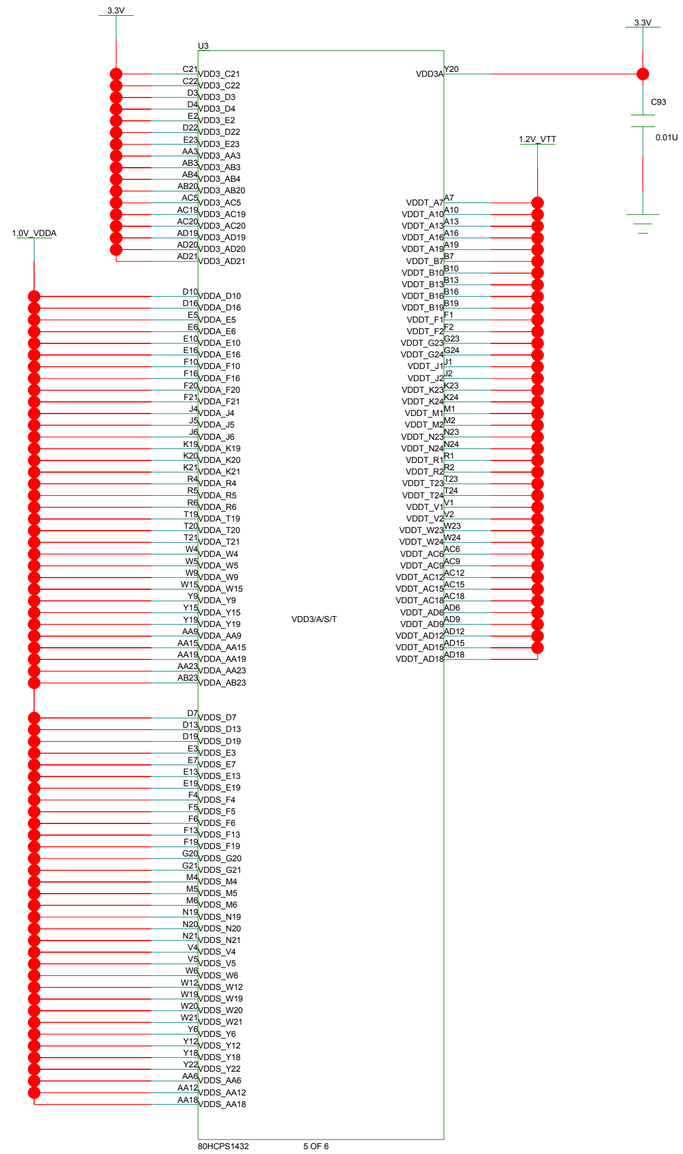
CPS1432 Power

Decoupling 1.0V_VDDA

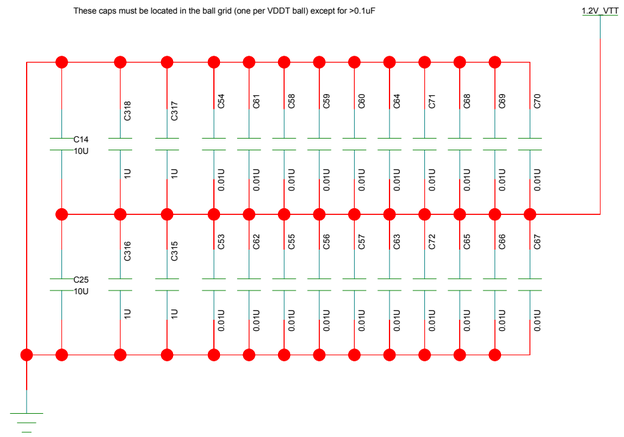
These caps must be located in the ball grid except for >0.1uF





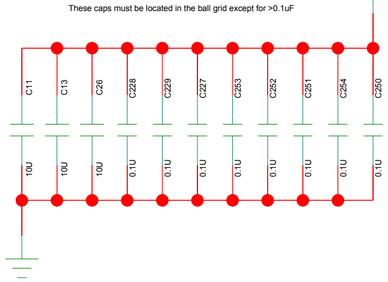
Decoupling 1.2V_VDDT

These caps must be located in the ball grid (one per VDDT ball) except for >0.1uF



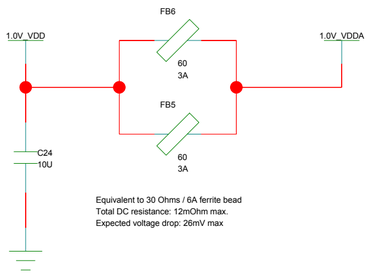
Decoupling 3.3V

These caps must be located in the ball grid except for >0.1uF



Board layout note:

Make two seperate power planes: 1.0V_VDD and 1.0V_VDDA



Equivalent to 30 Ohms / 6A ferrite bead
Total DC resistance: 12mOhm max.
Expected voltage drop: 26mV max

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TITLE :

CPS1432 POWER

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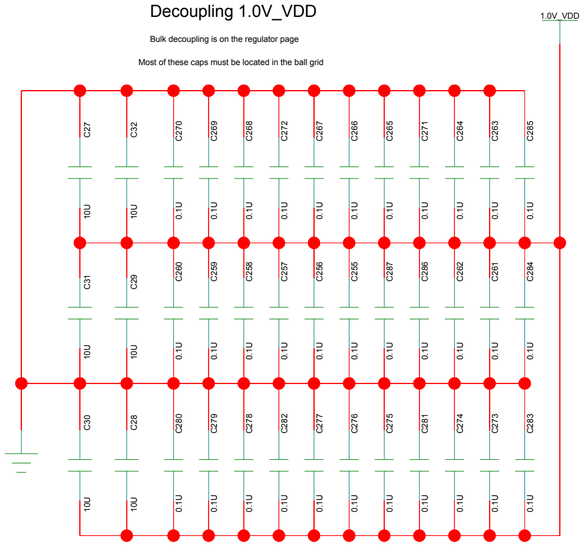
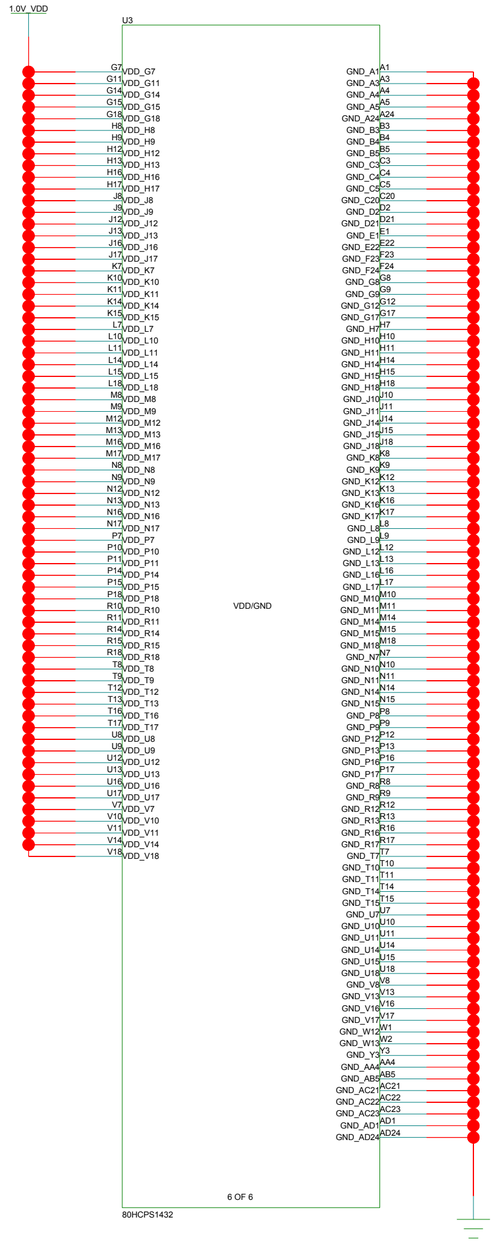
CPS1432 Core Power & Ground

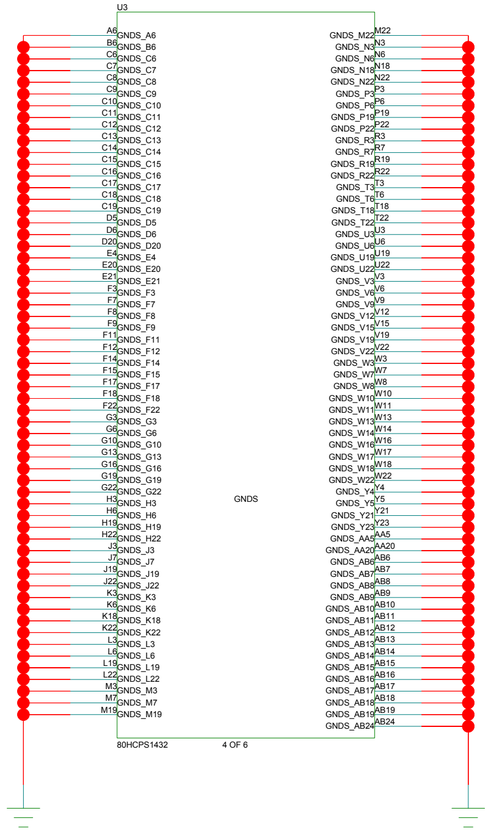
Decoupling 1.0V_VDD

Bulk decoupling is on the regulator page

Most of these caps must be located in the ball grid







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TITLE :	CPS1432 CORE POWER & GROUND
SIZE: C	DRAWING NUMBER :
Version:	DESIGNER :
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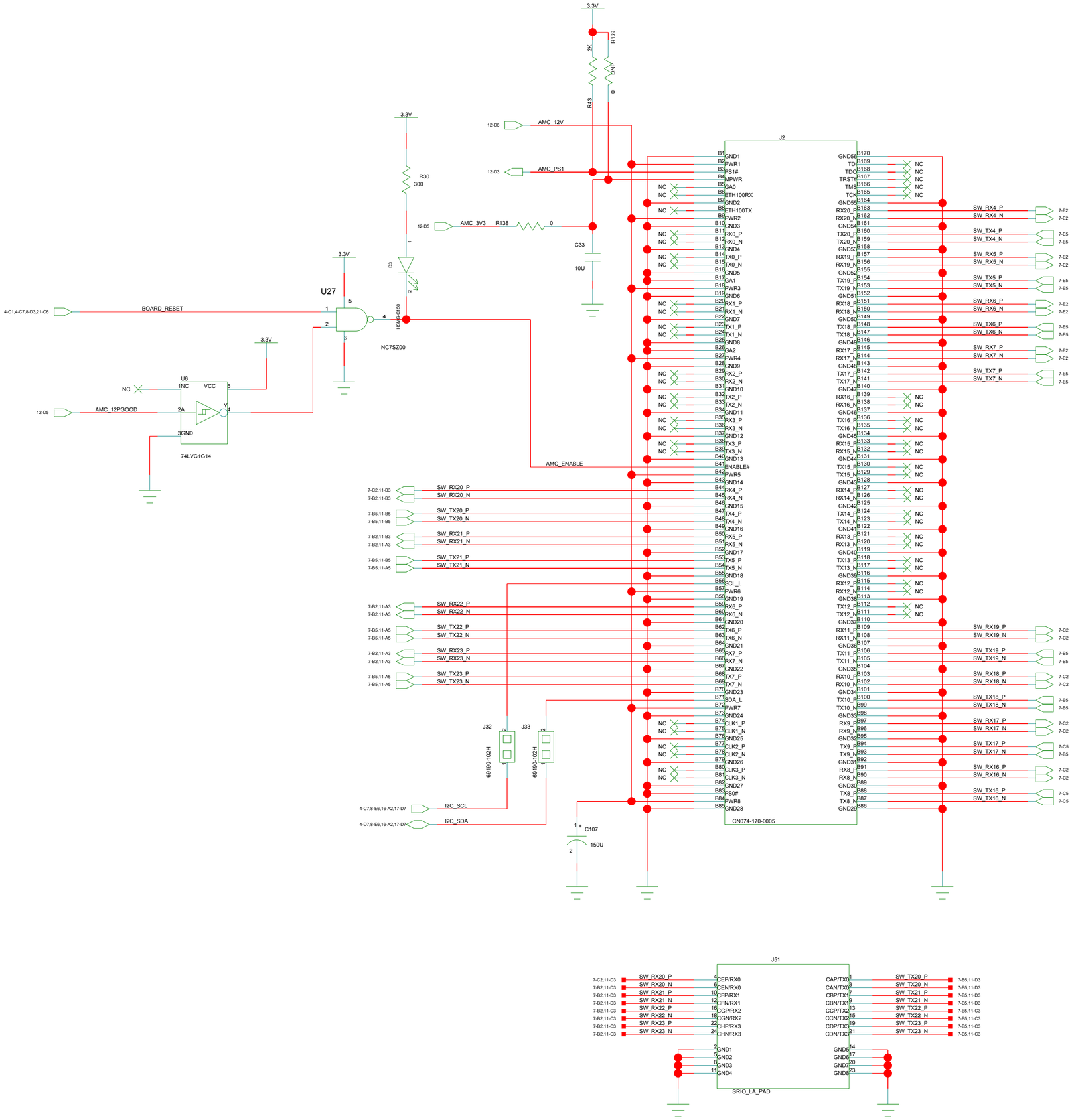
AMC Connector



TITLE :	AMC CONNECTOR		
SIZE: C	DRAWING NUMBER :	Version:	DESIGNER :
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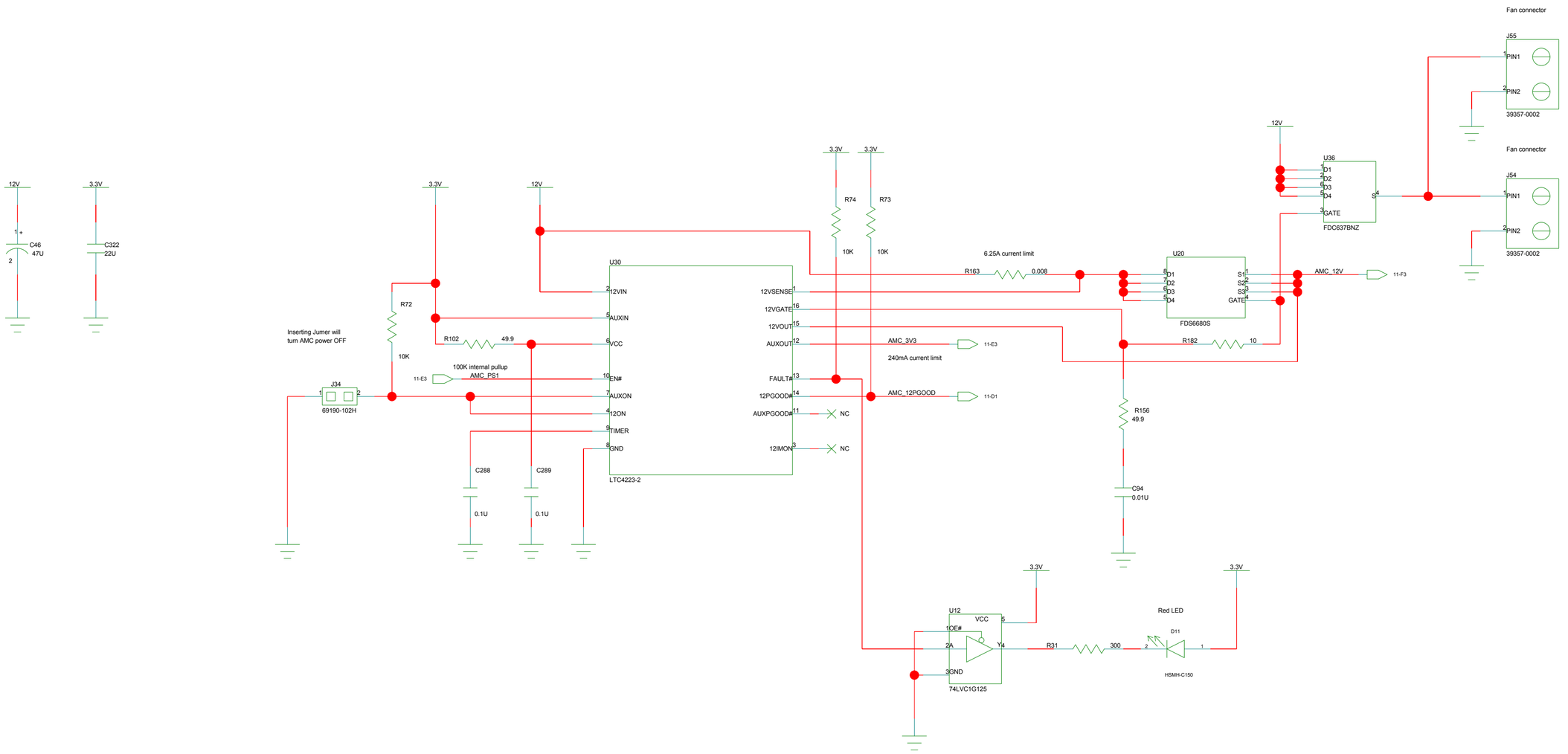
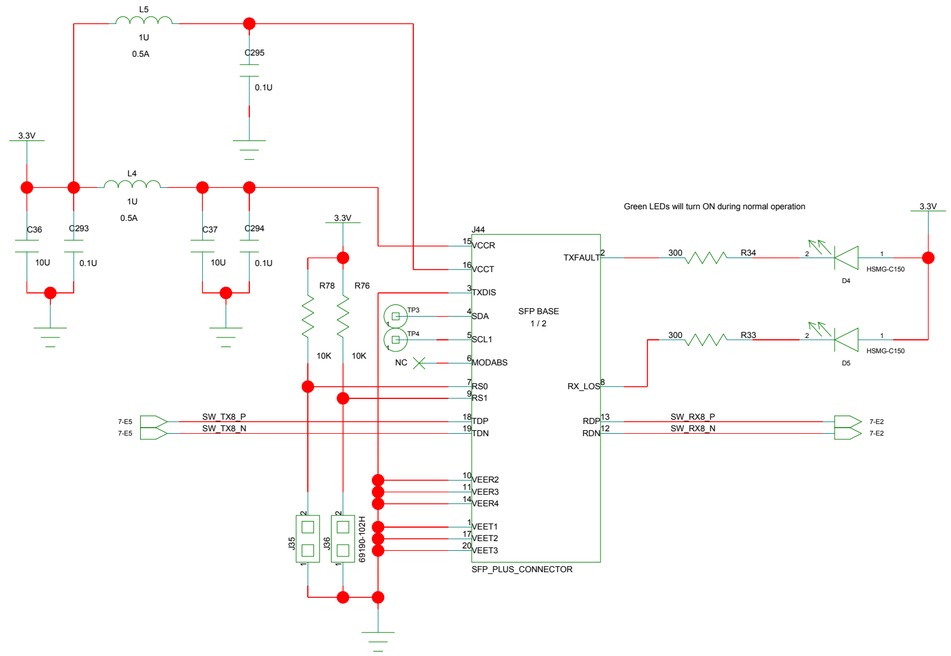
AMC Hot plug / Power Controller

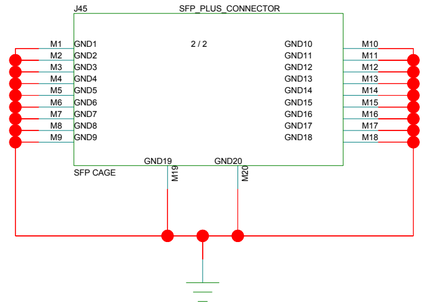


TITLE : AMC HOT PLUG / POWER CONTROLLER			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 07-09-2011_13:17	SHEET 12 OF 21		

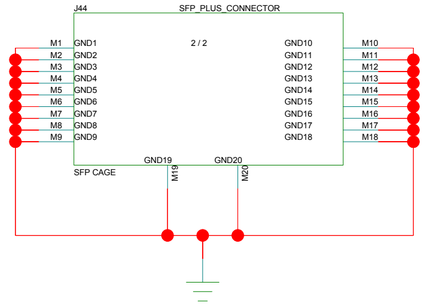
SFP+ Connectors



PRESS FIT CAGE



PRESS FIT CAGE



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TITLE :

SFP+ CONNECTORS

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
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07-09-2011_13:17

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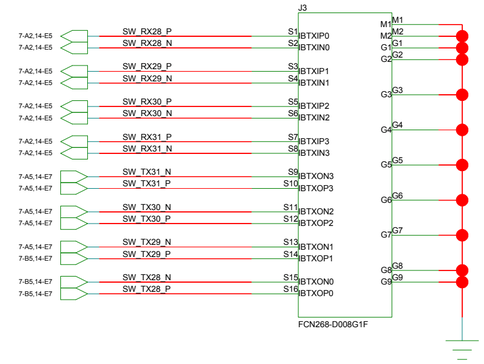
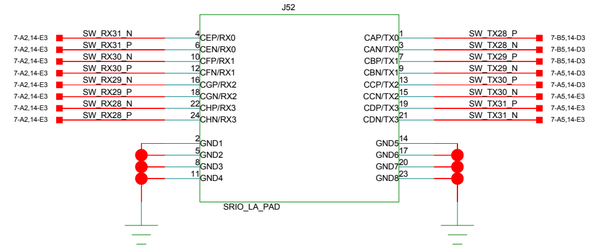
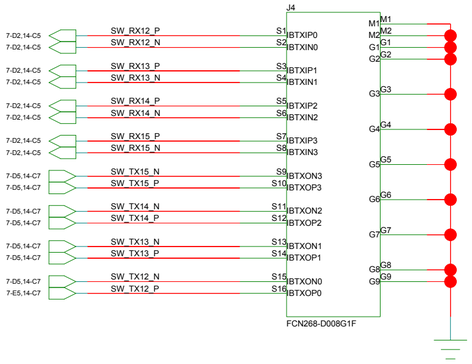
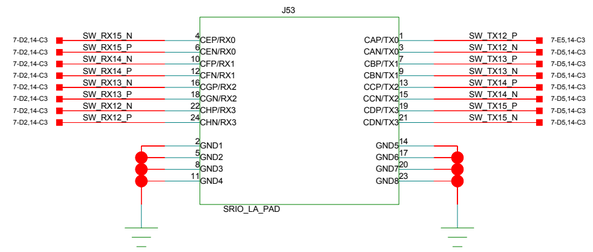
Infiniband Connectors









IDT

TITLE :

INFINIBAND CONNECTORS

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C			

LAST MODIFIED DATE :

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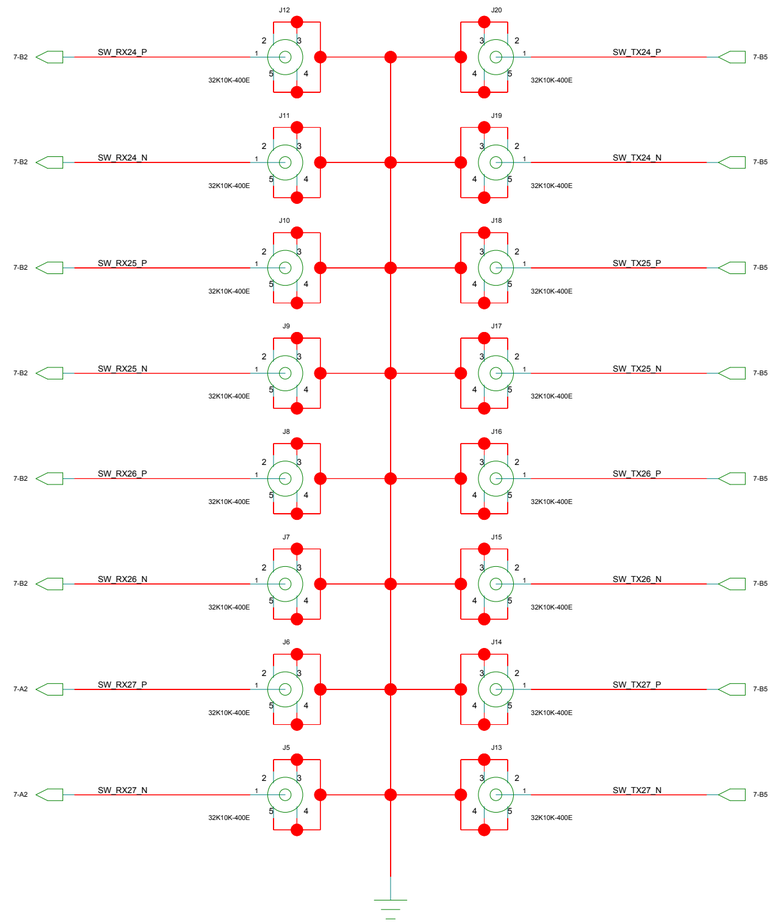
SMA Connectors

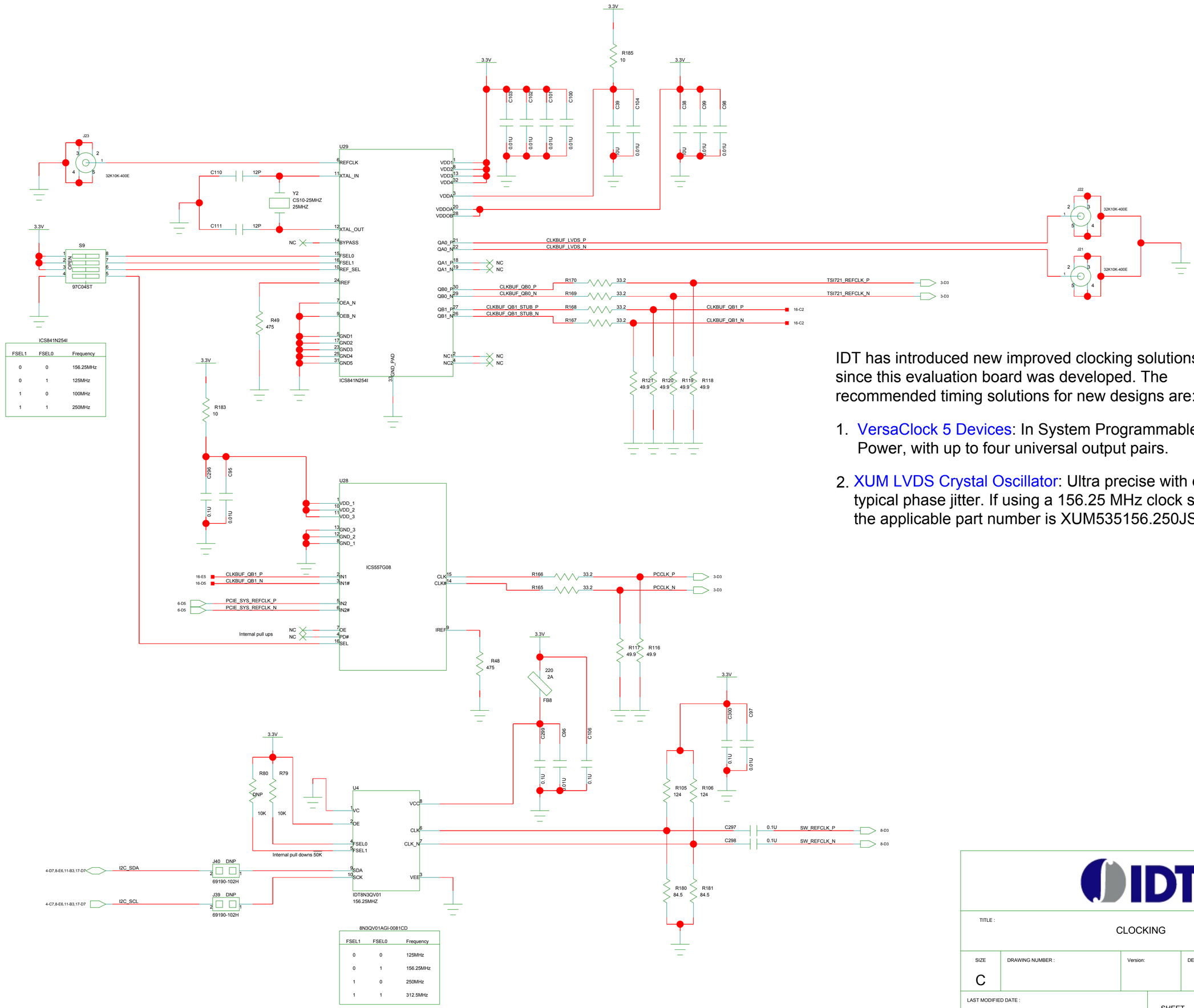


TITLE : SMA CONNECTORS

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C			

LAST MODIFIED DATE : 07-09-2011_13:17

Clocking



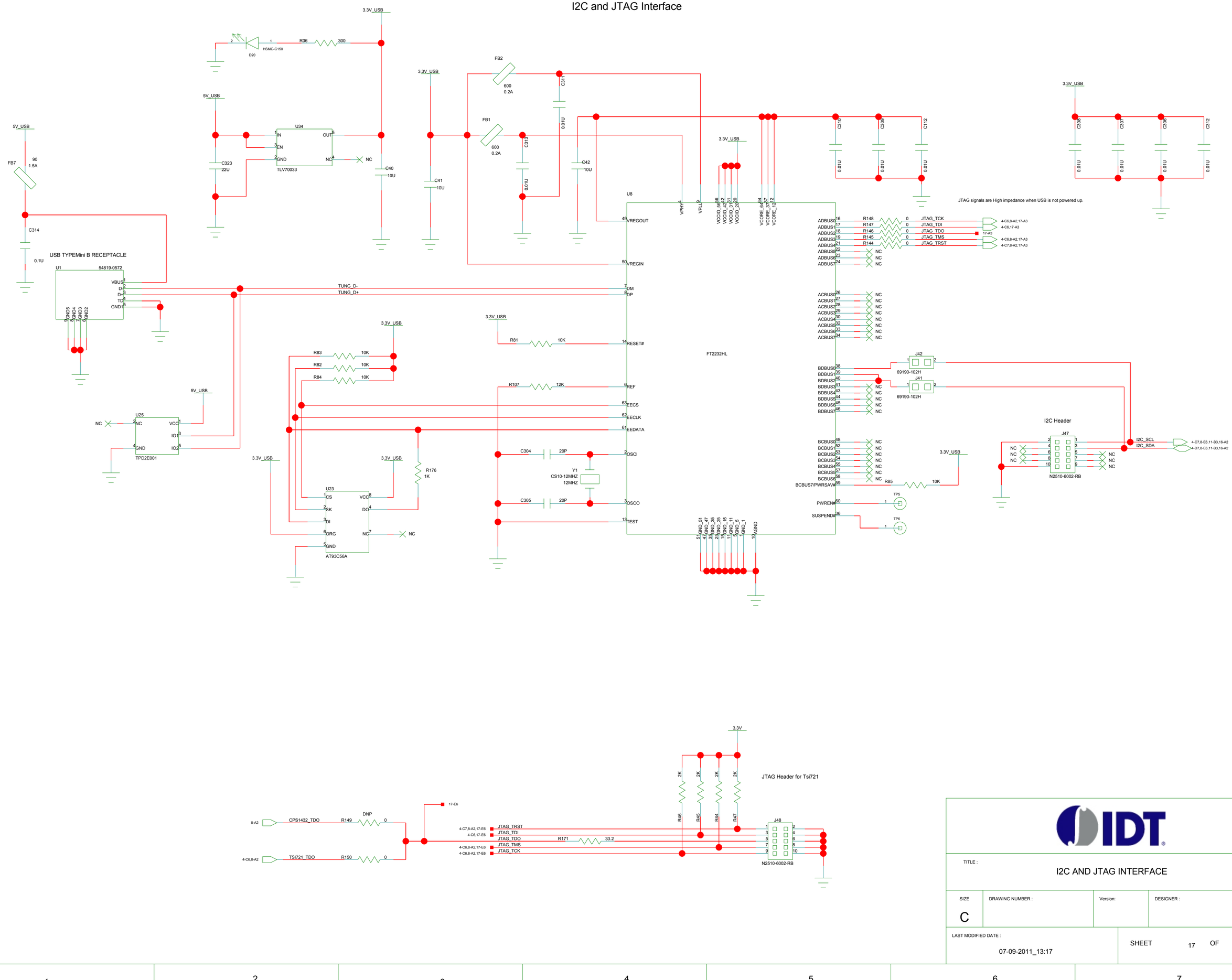
IDT has introduced new improved clocking solutions since this evaluation board was developed. The recommended timing solutions for new designs are:

1. VersaClock 5 Devices: In System Programmable, Very Low Power, with up to four universal output pairs.

2. XUM LVDS Crystal Oscillator: Ultra precise with only 300fs typical phase jitter. If using a 156.25 MHz clock source then the applicable part number is XUM535156.250JS6I8.

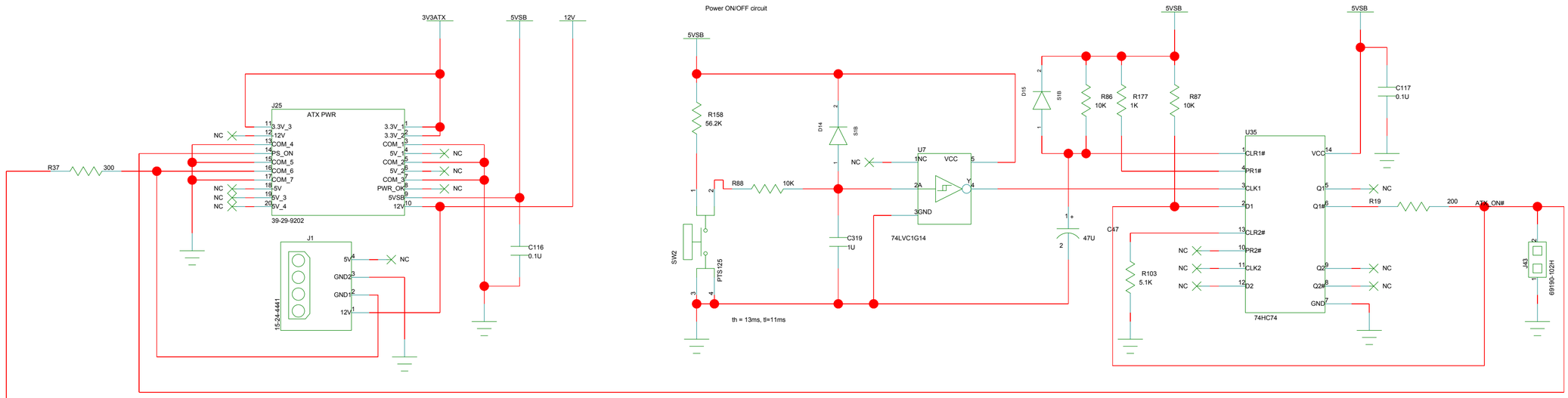
TITLE : CLOCKING			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 07-09-2011_13:17	SHEET 16 OF 21		

I2C and JTAG Interface

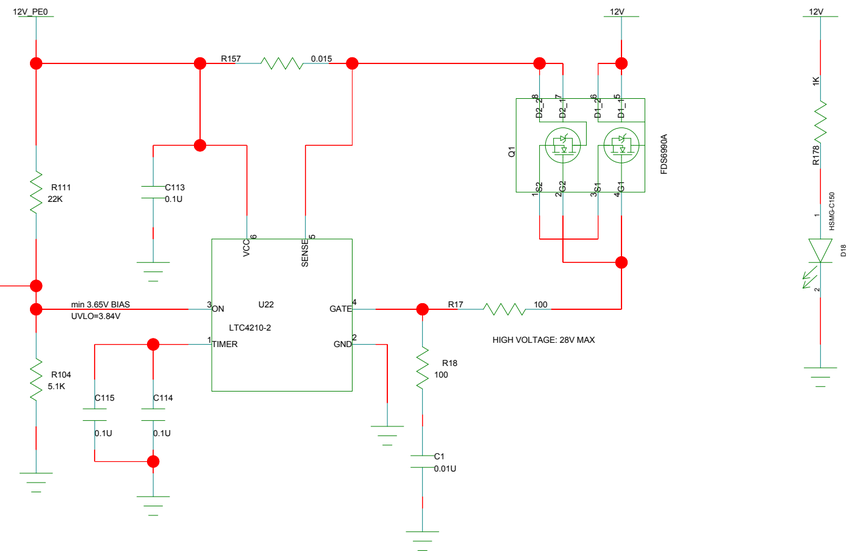


TITLE : I2C AND JTAG INTERFACE			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 07-09-2011_13:17	SHEET 17 OF 21		

ATX Power

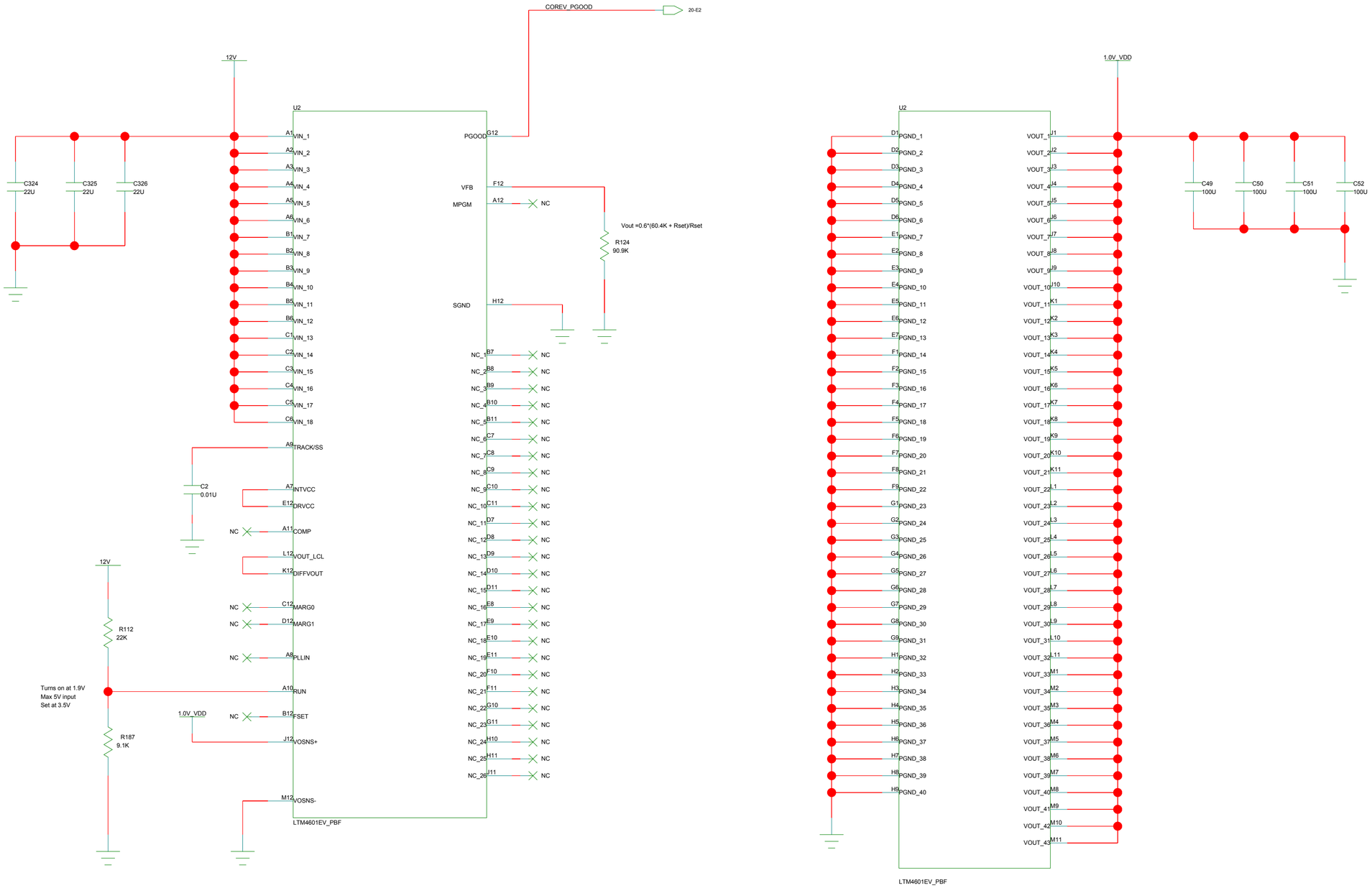


SYS SUPPLY SWITCH



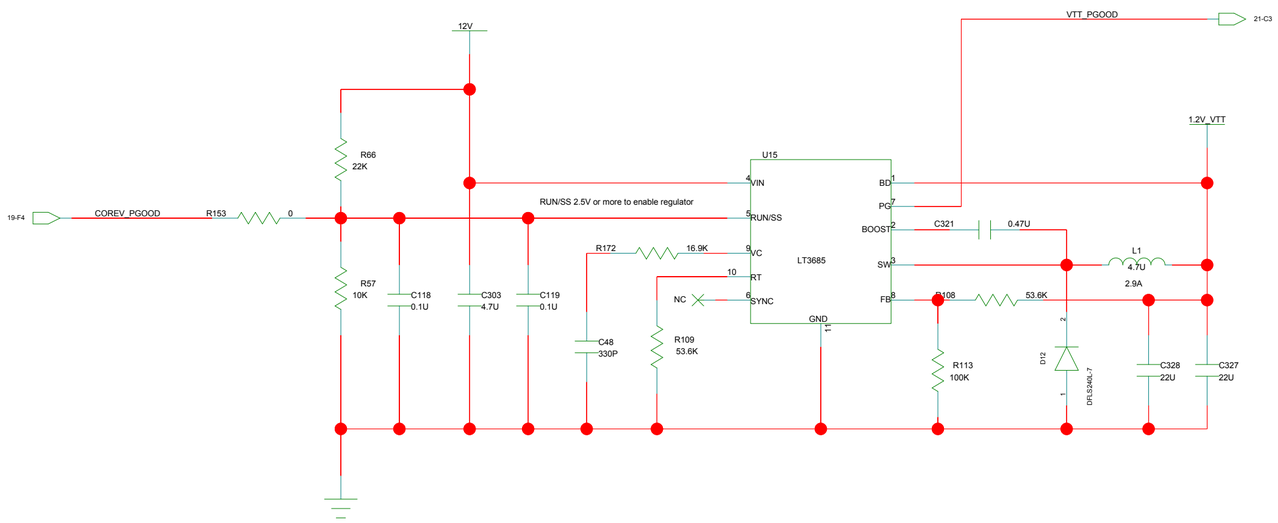
TITLE : ATX POWER			
SIZE: C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 13-09-2011_16:07	SHEET 18 OF 21		

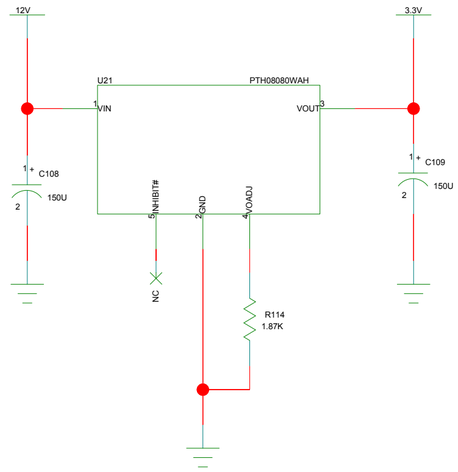
Core Voltage Regulator

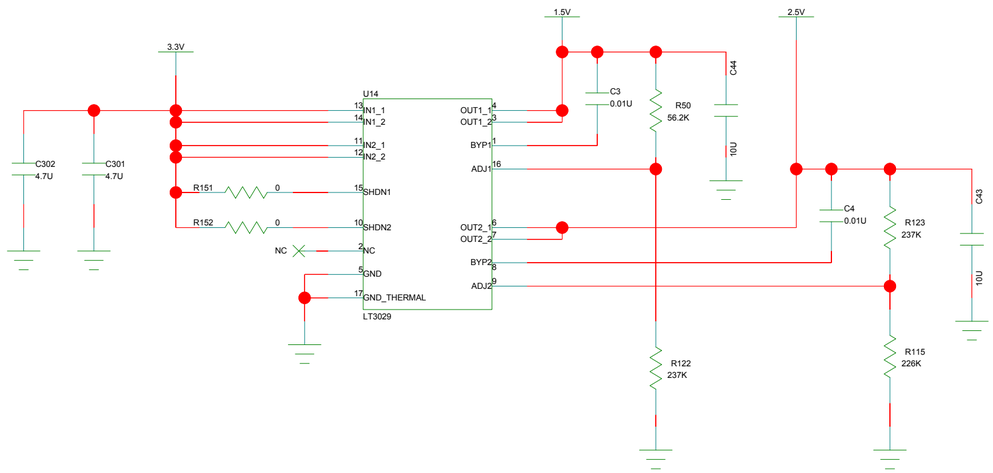


TITLE : CORE VOLTAGE REGULATOR			
SIZE: C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 07-09-2011_13:17	SHEET 19 OF 21		

Voltage Regulators



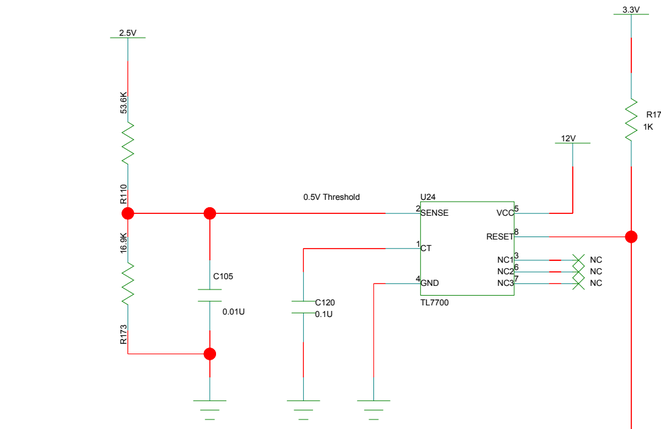




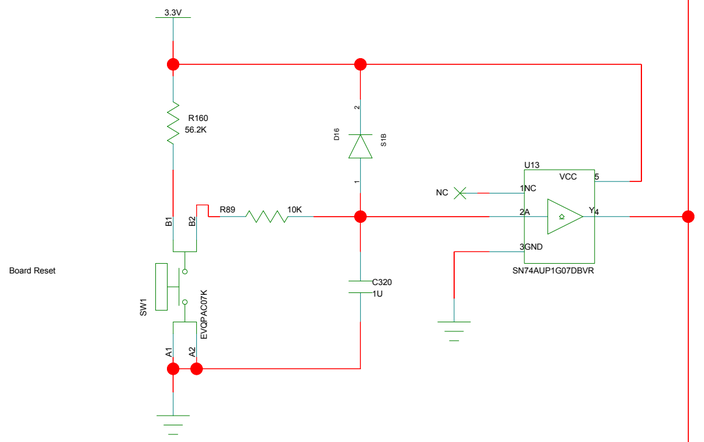
TITLE : VOLTAGE REGULATORS			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 07-09-2011_13:17	SHEET 20 OF 21		

Voltage Monitors

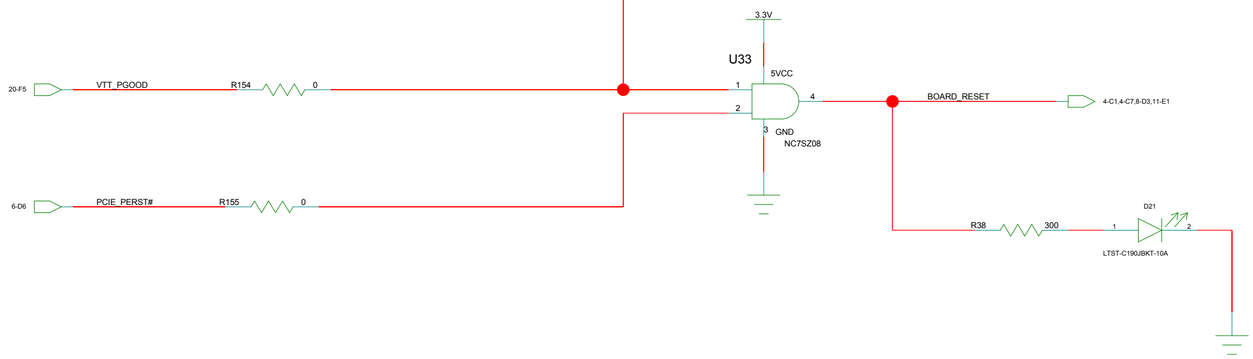
Board Reset



POR delay 10ms



Board Reset



TITLE : VOLTAGE MONITORS & BOARD RESET			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 07-09-2011_13:17		SHEET 21 OF 21	

Revision History

April 7, 2015 -- Added a note on page 16 on improving clocking solutions for S-RIO components.

June 28, 2011 -- The following changes were made:

* Sheet 4 - Added connections to ground on SP_SWAP_TX and SP_SWAP_RX
* Sheet 4 - Added 10K pull up resistors to 3.3V on SP_DEVID, CLKSEL[0] and CLKSEL[1]
* Sheet 4 - Added DNP attribute on U10
* Sheet 21 - Changed U13 to SN74AUP1G07
* Sheet 21 - Changed C320 to 0.1uF

April 11, 2011 -- First release of document.

TITLE : Revision History				
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :	
LAST MODIFIED DATE :		SHEET		