

F1441

1350MHz to 2800MHz Configurable 50Ω or 100Ω DIFF-In to 50Ω SE-Out Variable Gain Amplifier

The F1441 is a high-linearity variable gain RF amplifier with an integrated digital step attenuator (DSA) designed to operate within the 1350MHz to 2800MHz frequency range. Using a single 5V power supply, the F1441 typically provides 40dB of gain, 2.5dB of noise figure, 41dBm of OIP3, and 27dBm OP1dB at its maximum gain setting.

The F1441 is packaged in a 5 × 5 mm, 32-VFQFPN package, with an external input BOM configurable differential 50Ω or 100Ω input and single-ended 50Ω output impedances for ease of integration into the signal path.

Competitive Advantage

- High level of integration in a compact 5 × 5 mm 32-VFQFPN package
- Uses patented *Glitch-Free™* technologies, providing superior performance and PA damage protection over the entire RF gain range

Applications

- FDD or TDD 5G sub-6GHz wireless infrastructure
- Repeaters and DAS
- General-purpose RF

Features

- Frequency range: 1350MHz to 2800MHz
- 40dB typical gain at 2000MHz
- 2.5dB typical NF at 2000MHz
- 41dBm typical OIP3 at 2000MHz
- 27dBm typical OP1dB at 2000MHz
- Configurable 50Ω or 100Ω differential input impedance through external input BOM change
- 31.5dB DSA range with 0.5dB step size
- 5V power supply
- 350mA typical quiescent current consumption
- 1.8V and 3.3V SPI SDI logic compatible
- 1.8V SPI SDO logic compatible
- SPI control for DSA attenuation
- Disable mode for power savings
- Operating temperature (T_{EPAD}) range: -40°C to +105°C
- 5 × 5 mm 32-VFQFPN package

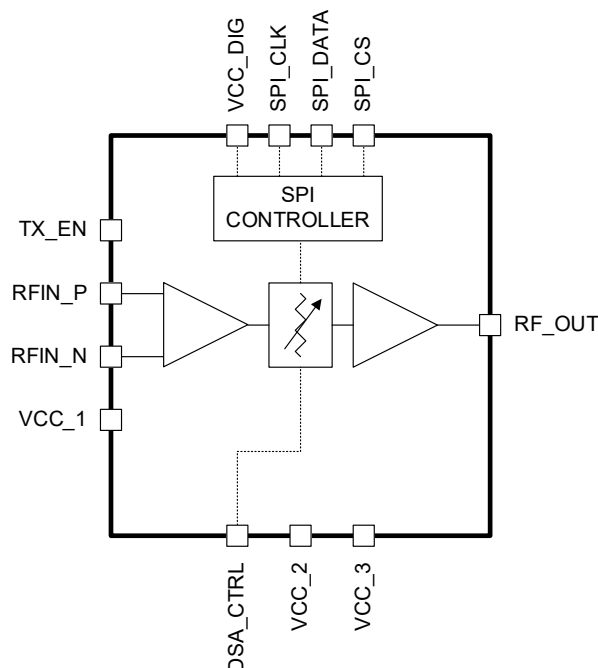


Figure 1. Block Diagram

Contents

1. Pin Information	4
1.1 Pin Assignments	4
1.2 Pin Descriptions	4
2. Specifications	6
2.1 Absolute Maximum Ratings	6
2.2 Recommended Operating Conditions	6
2.3 Electrical Specifications	7
2.3.1 General Electrical Specifications	7
2.3.2 1750MHz to 2250MHz Electrical Specifications	8
2.3.3 1350MHz to 2800MHz Electrical Specifications	9
2.4 Thermal Characteristics	11
2.4.1 Elevated Operating Temperature Considerations	11
3. Typical Operating Conditions	12
3.1 Typical Performance Curves	12
3.2 1350MHz to 2800MHz Performance	12
4. Functional Description	16
4.1 TX Enable	16
4.2 Serial Programming	16
4.2.1 SPI Protocol	16
4.2.2 Device Register Map	16
4.2.3 DSA Truth Tables	19
4.2.4 Timing Diagrams	21
4.2.5 DSA Mode Control	22
5. Evaluation Board (EVB) Information	23
5.1 Evaluation Board Schematic	24
5.2 Evaluation Kit (EVK) Information	25
5.3 Bill of Materials	25
6. Package Outline Drawings	28
7. Marking Diagram	28
8. Ordering Information	28
9. Revision History	29

Figures

Figure 1. Block Diagram	1
Figure 2. Pin Assignments – Top View.....	4
Figure 3. Gain	12
Figure 4. Gain vs. Attenuation State, 5V, 25°C	12
Figure 5. Input Return Loss	12
Figure 6. Output Return Loss	12
Figure 7. Reverse Isolation	13
Figure 8. CMRR.....	13
Figure 9. Gain Imbalance	13
Figure 10. Phase Imbalance	13
Figure 11. Disable Mode Gain	13
Figure 12. OIP3, DSA = 0dB, 10MHz Tone Spacing.....	13
Figure 13. OIP3, DSA = 16dB, 10MHz Tone Spacing.....	14
Figure 14. OIP3, DSA = 31.5dB, 10MHz Tone Spacing.....	14
Figure 15. OP1dB, DSA = 0dB	14
Figure 16. OP1dB, DSA = 16dB	14
Figure 17. OP1dB, DSA = 31.5dB	14
Figure 18. ACLR, DSA = 0, at 2GHz	14
Figure 19. Noise Figure, DSA = 0dB	15
Figure 20. Noise Figure, DSA = 16dB	15
Figure 21. DSA Step Size at 2GHz	15
Figure 22. K-Factor.....	15
Figure 23. Write Mode Timing Diagram.....	21
Figure 24. Read Mode Timing Diagram	21
Figure 25. SPI Timing Information	22
Figure 26. Evaluation Board – Front.....	23
Figure 27. Evaluation Board – Back	23
Figure 28. Evaluation Board Circuit Schematic – Image 1	24
Figure 29. Evaluation Board Circuit Schematic – Image 2.....	25

Tables

Table 1. TX Enable Truth Table	16
Table 2. Digital Specification	22
Table 3. DSA_CTRL Truth Table.....	22
Table 4. Evaluation Board Bill of Material (BOM) – 100Ω	25
Table 5. Evaluation Board Bill of Material (BOM) – 50Ω	27
Table 6. Pin 1 Orientation in Tray and Reel Packaging	29

1. Pin Information

1.1 Pin Assignments

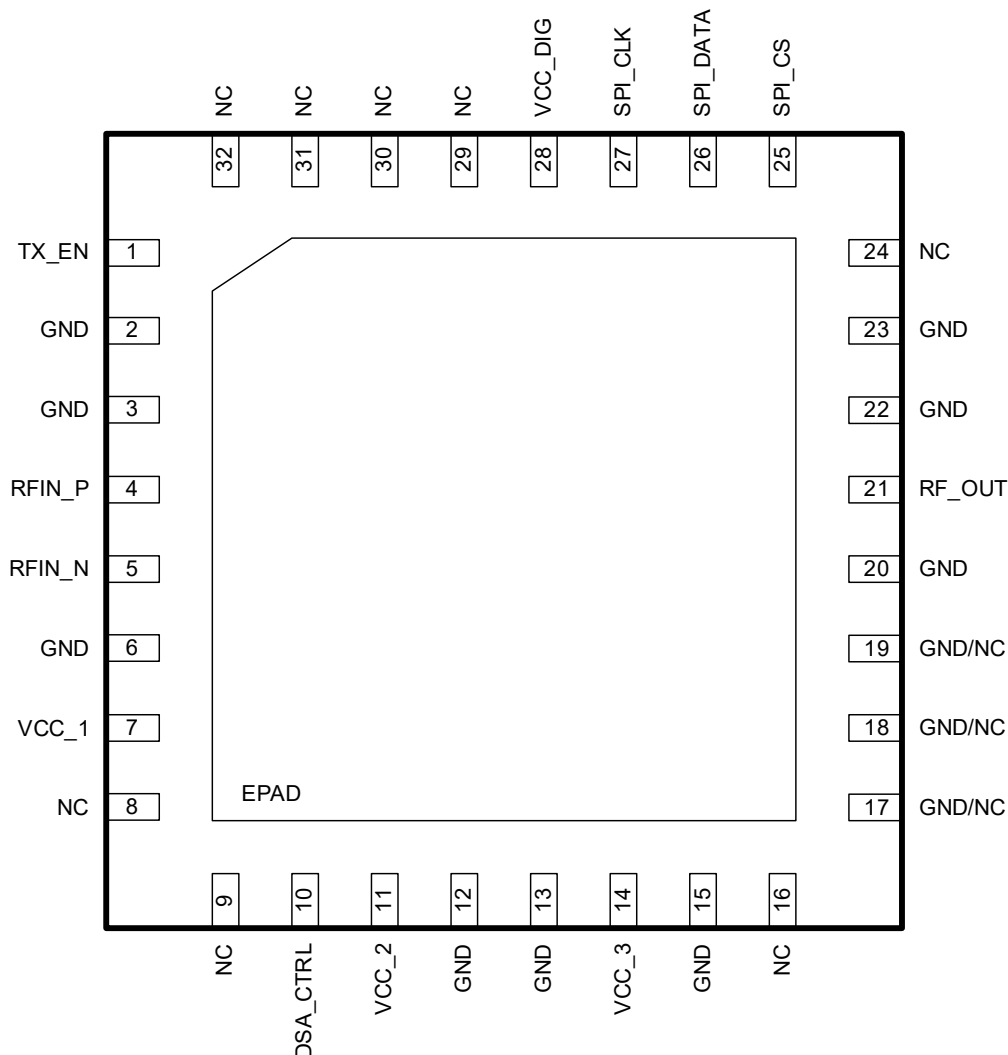


Figure 2. Pin Assignments – Top View

1.2 Pin Descriptions

Number	Name	Description
1	TX_EN	Power-down pin. With Logic LOW applied to this pin, the device is powered off. With Logic HIGH applied to this pin (or if the pin is left unconnected), the device is in full operation mode. Pin is 1.8V, and 3.3V logic compatible.
2, 3, 6, 12, 13, 15, 20, 22, 23,	GND	Internally grounded. This pin must be grounded with a via as close to the pin as possible.
4	RFIN_P	RF input. Must use an external DC block.
5	RFIN_N	RF input. Must use an external DC block.
7	VCC_1	5V power supply. Use bypass capacitors as close to the pin as possible.

Number	Name	Description
8, 9, 16, 24, 29, 30, 31, 32	NC	No internal connection. Can be left floating or connected to VCC or GND.
10	DSA_CTRL	DSA configuration control pin.
11	VCC_2	5V power supply. Use bypass capacitors as close to the pin as possible.
17, 18, 19	GND/NC	Ground or no connection. These pins can be left unconnected or connected to ground (recommended). If grounded, use a via as close to the pin as possible.
14	VCC_3	5V power supply. Use bypass capacitors as close to the pin as possible.
21	RF_OUT	RF output. Must use an external DC block.
25	SPI_CS	SPI chip-select pin.
26	SPI_DATA	SPI data pin for read and write operations.
27	SPI_CLK	SPI clock pin.
28	VCC_DIG	5V digital power supply. Use bypass capacitors as close to the pin as possible.
-	EPAD	Exposed Pad. Internally connected to ground. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the noted RF performance.

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Stresses above those listed below can cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Parameter	Symbol	Minimum	Maximum	Unit
V _{CC} to GND	V _{CC}	-0.3	+5.5	V
SPI_CLK, SPI_DATA, SPI_CS	V _{SPI}	-0.3	V _{CC} + 0.25	V
TX_EN, DSA_CTRL	V _{CTL}	-0.3	V _{CC} + 0.25	V
RFIN Externally Applied DC Current	V _{RFIN}	-1	+1	mA
Maximum CW Input Power applied for 24 hours. V _{CC} = 5V, T _{EPAD} = 105°C. 50Ω system. TX_EN = logic HIGH: ON state ^[1]	P _{MAX_IN_ON}	-	+6	dBm
Maximum CW Input Power applied for 24 hours. V _{CC} = 5V, T _{EPAD} = 105°C. 50Ω system. TX_EN = logic LOW: OFF state ^[1]	P _{MAX_IN_OFF}	-	+6	dBm
Storage Temperature Range	T _{st}	-65	150	°C
Lead Temperature (soldering, 10s)		-	260	°C
SiGe device Maximum Junction Temperature	T _{J_MAX_SiGe}	-	+140	°C
GaAs device Maximum Junction Temperature	T _{J_MAX_GaAs}	-	+160	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V _{ESDHBM}	-	1000	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)	V _{ESDCDM}	-	500	V

1. Exposure to these maximum RF levels can result in significantly higher I_{CC} current draw because of overdriving the amplifier stages.

2.2 Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power Supply Voltage	V _{CC}	-	4.75	5	5.25	V
Full Functionality Operating Temperature Range	T _{EPAD1}	Exposed paddle	-40	-	+105	°C
Full Performance Operating Temperature Range	T _{EPAD1}	Exposed paddle	-20	-	+105	°C
Junction Temperature	T _J	SiGe device	-	-	+125	°C
		GaAs device	-	-	+150	°C
RF Frequency Range	f _{RF}	-	1350	-	2800	MHz
RFIN Port Impedance	Z _{RFI}	Differential	-	50 or 100	-	Ω
RFOUT Port Impedance	Z _{RFO}	Single-ended	-	50	-	Ω

2.3 Electrical Specifications

2.3.1 General Electrical Specifications

Specifications apply when operated as a TX amplifier with internal tuning optimized for desired band of interest (see Register settings in section Device Register Map), $V_{CC} = +5.0V$, $T_{EPAD} = +25^{\circ}C$, $TX_EN = HIGH$, $Z_S = 100\Omega$ differential, $Z_L = 50\Omega$ single-ended, and maximum gain setting. Evaluation Board trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Logic Input High	V_{IH}	-	1.17 ^[1]	-	3.3	V
Logic Input Low	V_{IL}	-	-0.3	-	0.63	V
SPI Logic Current ^[2]	I_{SPI}	1.8V	-100	-	100	μA
		3.3V	-100	-	100	μA
TX_EN, DSA_CTRL Logic Current	I_{CTL}	1.8V	-150	-	150	μA
		3.3V	-150	-	150	μA
Quiescent Current ^[3]	I_{CC}	-	-	350	390	mA
Standby Current	I_{DD_STBY}	TX_EN pin = LOW	-	5	-	mA
Enable Settling Time ^[4]	t_{SETTLE_ON}	50% TX_EN control to RF output within 0.25dB and 1° of the on-state final value. $T_{EPAD} = -20^{\circ}C$ to $105^{\circ}C$, $V_{CC} = 4.75V$ to $5.25V$	-	-	1	μs
Disable Settling Time ^[4]	t_{SETTLE_OFF}	50% TX_EN control to Maximum gain – 40dB. $T_{EPAD} = -20^{\circ}C$ to $105^{\circ}C$, $V_{CC} = 4.75V$ to $5.25V$	-	-	1	μs
Serial Clock Speed	f_{CLK}	-	-	-	25	MHz
CS to First Serial Clock Rising Edge	t_{LS}	SPI 3-wire bus. 50% of CS falling edge to 50% of CLK rising edge.	10	-	-	ns
Serial Data Hold Time	t_H	SPI 3-wire bus. 50% of CLK rising edge to 50% of DATA falling edge.	10	-	-	ns
Final Serial Clock Rising Edge to CS	t_{CLS}	SPI 3-wire bus. 50% of CLK rising edge to 50% of CS rising edge.	10	-	-	ns

1. Specifications in the minimum/maximum columns that are shown in **bold italics** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.
2. Voltage condition refers to SDI logic.
3. I_{CC} refers to the nominal small signal bias current.
4. Speeds are measured after SPI programming is completed (data latched with SPI_CS = HIGH).

2.3.2 1750MHz to 2250MHz Electrical Specifications

Typical specifications apply when operated as a TX amplifier with internal tuning optimized for desired band of interest (see Register settings in section Device Register Map), $V_{CC} = +5.0V$, $T_{EPAD} = +25^{\circ}C$, $f_{RF} = 2000MHz$, $TX_EN = HIGH$, $Z_S = 100\Omega$ differential, $Z_L = 50\Omega$ single-ended, and maximum gain setting (DSA = 0dB). Minimum and maximum specifications apply across process, recommended operating voltage, and full performance temperature unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	-	35	40	45	dB
		+105°C	35	-	42	
Gain Slope Relative to Center Frequency	G_{SLOPE}	Across any $\pm 100MHz$ BW.	-	-	-0.3 / +0.5	dB
		Across any $\pm 250MHz$ BW.	-	-	-0.5 / +1.1	dB
CMRR	CMR	-	25	-	-	dB
Gain Imbalance	G_{IMB}	-	-	0.2	-	dB
Phase Imbalance	PH_{IMB}	-	-	1	-	deg
RF Input Return Loss	RL_{RFIN}	-	11	-	-	dB
RF Output Return Loss	RL_{RFOUT}	-	9	-	-	dB
Reverse Isolation	ISO_{REV}	-	-	59	-	dB
Disable Mode Gain	G_{STBY}	STBY = logic LOW, $P_{IN} \leq -15dBm$	-	-55	-	dB
DSA Dynamic Range	DSA_{RANGE}	-	30.5	-	-	dB
DSA Step Size	DSA_{STEP}	-	0.25	0.5	0.6	dB
DSA Phase Delta	DSA_{PHASE}	Phase change A_{MIN} vs. A_{MAX} .	-	10	-	deg
DSA Settling Time	DSA_{SETTLE}	From rising edge of SPI_CS to within 0.1dB of final gain setting, excluding SPI communication.	-	-	1	μs
DSA Transient Slew Rate	DSA_{SLEW}	For every 0.5 and 1dB attenuation state change combination only.	-	-	75	dB/ μs
Noise Figure	NF	DSA = 0dB	-	2.5	4.5	dB
		DSA = 16dB	-	5	7	dB
Output 3rd Order Intercept Point [1]	OIP3	DSA = 0dB	37	41	-	dBm
		DSA = 16dB	32.5	38.5	-	dBm
		DSA = 31.5dB	18	24	-	dBm

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Output 1dB Compression Point	OP1dB	DSA = 0dB.	24	27	-	dBm
		DSA = 16dB.	19	22	-	dBm
		DSA = 31.5dB.	4	9	-	dBm
ACLR	ACP	E-TM1.1 at Pout = 10dBm DSA = 0dB.	-	-63	-	dBc
Stability K-Factor	K	10MHz to 13.5GHz.	1	-	-	

1. Pout = (OP1dB - 10dB) total power, Δf = 1MHz to 100MHz.

2.3.3 1350MHz to 2800MHz Electrical Specifications

Typical specifications apply when operated as a TX amplifier with internal tuning optimized for desired band of interest (see Register settings in section Device Register Map), $V_{CC} = +5.0V$, $T_{EPAD} = +25^{\circ}C$, $f_{RF} = 2000MHz$, $TX_EN = HIGH$, $Z_S = 100\Omega$ differential, $Z_L = 50\Omega$ single-ended, and maximum gain setting (DSA = 0dB).

Minimum and maximum specifications apply across process, recommended operating voltage, and full performance temperature unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	-	34	40	45	dB
		+105°C	34	-	42	
Gain Slope Relative to Center Frequency	G _{SLOPE}	Across any $\pm 100MHz$ BW.	-	-	-0.3/+0.5	dB
		Across any $\pm 250MHz$ BW.	-	-	-0.5/+1.1	dB
		Across any $\pm 500MHz$ BW.	-	-	-0.9/+2.0	dB
CMRR	CMR	-	23	-	-	dB
Gain Imbalance	G _{IMB}	-	-	0.2	-	dB
Phase Imbalance	PH _{IMB}	-	-	1	-	deg
RF Input Return Loss	RL _{RFIN}	1350MHz – 1750MHz.	7	-	-	dB
		1750MHz – 2250MHz	11			dB
		2250MHz – 2800MHz	11	-	-	dB
RF Output Return Loss	RL _{RFOUT}	-	9	-	-	dB
Reverse Isolation	ISO _{REV}	-	-	59	-	dB
Disable Mode Gain	G _{STBY}	STBY = logic LOW, P _{IN} $\leq$ -15dBm	-	-55	-	dB
DSA Dynamic Range	DSA _{RANGE}	1350MHz – 1750MHz	30	-	-	dB
		1750MHz – 2250MHz	30.5	-	-	dB
		2250MHz – 2800MHz	31	-	-	dB

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
DSA Step Size	DSA _{STEP}	1750MHz – 2250MHz	0.25	0.5	0.6	dB
DSA Phase Delta	DSA _{PHASE}	Phase change A _{MIN} vs. A _{MAX} .	-	10	-	deg
DSA Settling Time	DSA _{SETTLE}	From rising edge of SPI_CS to within 0.1dB of final gain setting, excluding SPI communication.	-	-	1	μs
DSA Transient Slew Rate	DSA _{SLEW}	For every 0.5 and 1dB attenuation state change combination only.	-	-	75	dB/μs
Noise Figure	NF	DSA = 0dB.	-	2.5	6	dB
		DSA = 16dB.	-	5	9.2	dB
Output 3rd Order Intercept Point [1]	OIP3	DSA = 0dB.	37	41	-	dBm
		DSA = 16dB.	31.5	38.5	-	dBm
		DSA = 31.5dB.	17	24	-	dBm
Output 1dB Compression Point	OP1dB	DSA = 0dB.	24	27	-	dBm
		DSA = 16dB.	18	22	-	dBm
		DSA = 31.5dB.	2.5	9	-	dBm
ACLR	ACP	E-TM1.1 at P _{out} = 10dBm DSA = 0dB.	-	-63	-	dBc
Stability K-Factor	K	10MHz to 13.5GHz.	1	-	-	-

1. P_{out} = (OP1dB - 10dB) total power, Δf = 1MHz to 100MHz.

2.4 Thermal Characteristics

Parameter	Symbol	Value	Unit
Junction to Ambient Thermal Resistance	θ_{JA}	31.45	°C/W
Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	$\theta_{JC_BOT_SIGE}$	5.8	°C/W
	$\theta_{JC_BOT_GAAS}$	11.8	°C/W
Moisture Sensitivity Rating (Per J-STD-020)	-	MSL1	-

2.4.1 Elevated Operating Temperature Considerations

This F1441 supports applications in a natural convection environment that does not have any thermal conductivity through ambient air. The printed circuit board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (EPAD) with enhanced thermal parameters, which is soldered to the PCB where most of the heat escapes from the bottom of the exposed pad. For this type of application, it is recommended that the maximum recommended junction temperature is not exceeded when operating above the maximum recommended full functional operating temperature of 105°C to maintain long-term reliability. The junction temperature can be calculated using the following equation:

$$T_J = T_{EPAD} + (\theta_{JC_BOT} \times P_D), \text{ where}$$

- T_J = Junction temperature at steady state condition in °C.
- T_{EPAD} = Exposed pad temperature at steady state condition in °C.
- θ_{JC_BOT} = Junction to case thermal resistance (case is defined as the exposed paddle) in °C/W.
- P_D = Device power dissipation in W at the desired operating configuration.

The following is an example calculation given an EPAD temperature of 108°C.

Variable	Value
T_{EPAD}	108°C
$\theta_{JC_BOT_SIGE}$	5.8°C/W
$\theta_{JC_BOT_GAAS}$	11.8°C/W
P_D	2.1W

- $T_{J_SIGE} = 108^\circ\text{C} + (5.8^\circ\text{C/W} \times 2.1\text{W}) = 120.2^\circ\text{C}$
- $T_{J_GAAS} = 108^\circ\text{C} + (11.8^\circ\text{C/W} \times 2.1\text{W}) = 132.8^\circ\text{C}$

For the variables above, the junction temperature is equal to 120.2°C for the SiGe IC and 132.8°C for the GaAs IC. Since this is below the maximum recommended junction temperature of 125°C for the SiGe IC and 150°C for the GaAs IC, there are no long-term reliability concerns.

3. Typical Operating Conditions

Unless otherwise stated, the typical operating graphs were measured under the following conditions:

- $V_{CC} = 5.0V$
- $TX_EN = HIGH$
- $T_{EPAD} = +25^{\circ}C$
- $f_{RF} = 2000MHz$
- $Z_S = 100\Omega$ differential, $Z_L = 50\Omega$ single-ended
- $P_{out} = 0dBm/tone$ and 10MHz tone spacing for OIP3

3.1 Typical Performance Curves

Note: 100 Ω BOM (maximum gain condition unless otherwise stated)

3.2 1350MHz to 2800MHz Performance

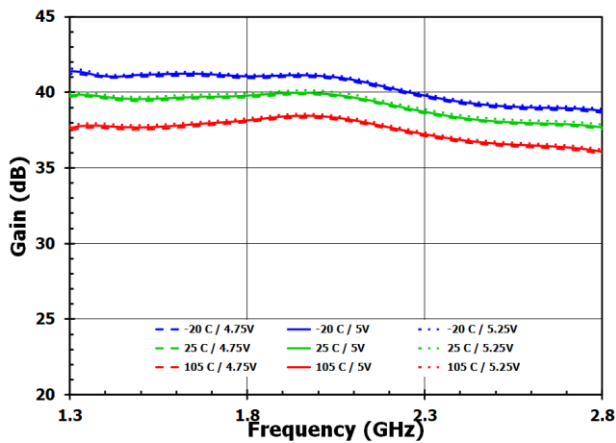


Figure 3. Gain

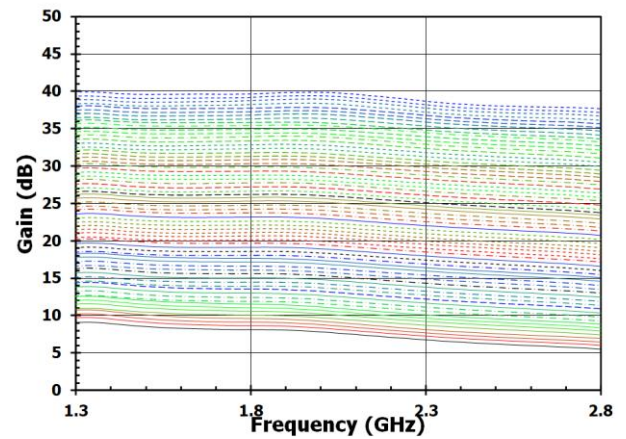


Figure 4. Gain vs. Attenuation State, 5V, 25°C

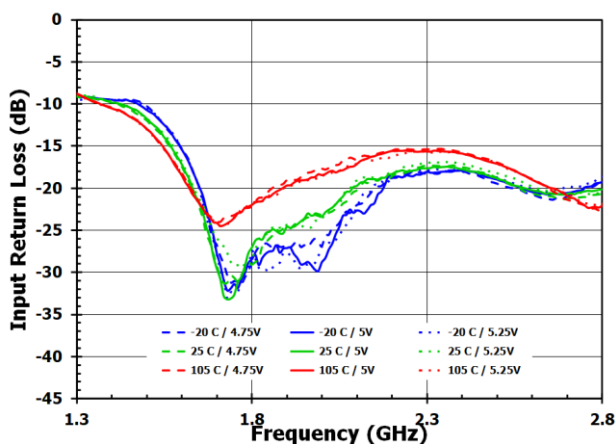


Figure 5. Input Return Loss

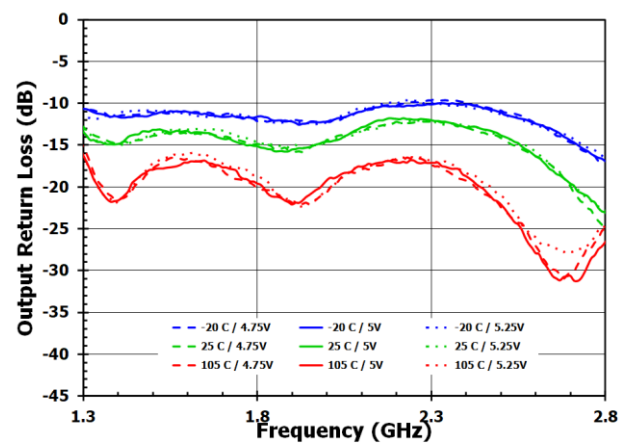


Figure 6. Output Return Loss

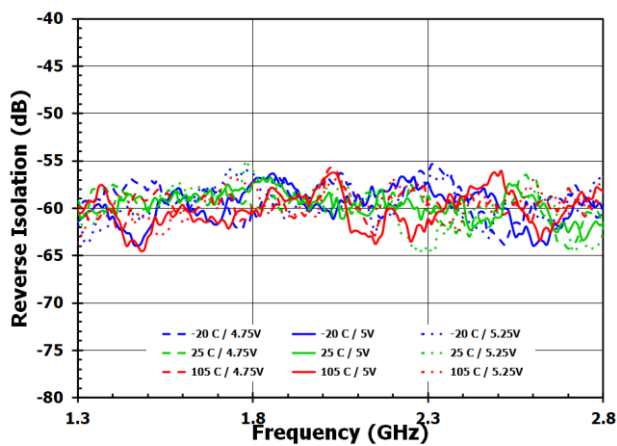


Figure 7. Reverse Isolation

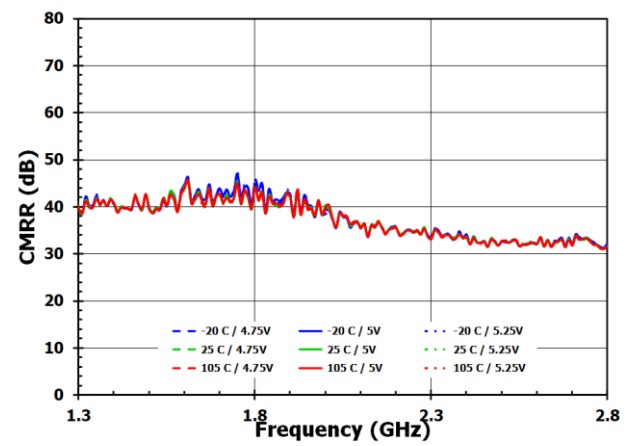


Figure 8. CMRR

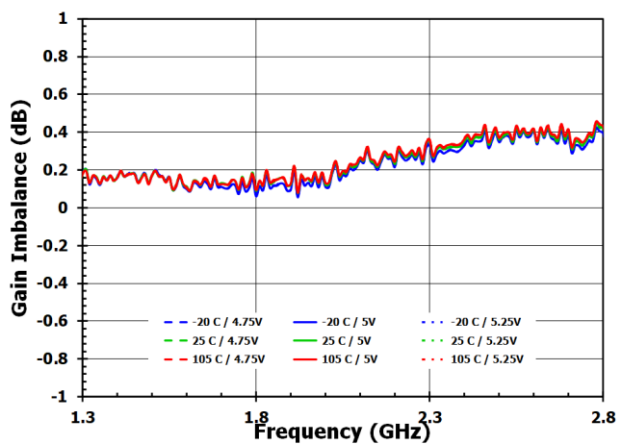


Figure 9. Gain Imbalance

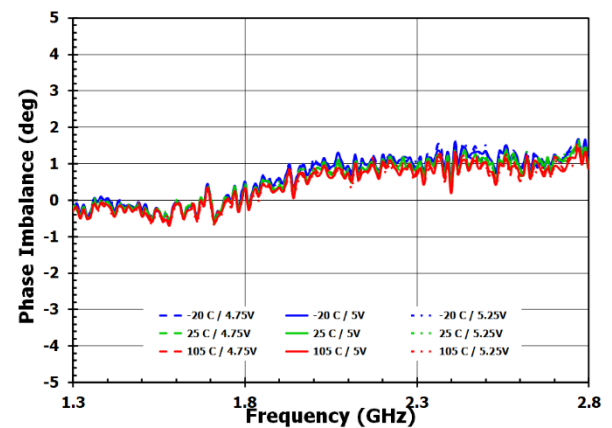


Figure 10. Phase Imbalance

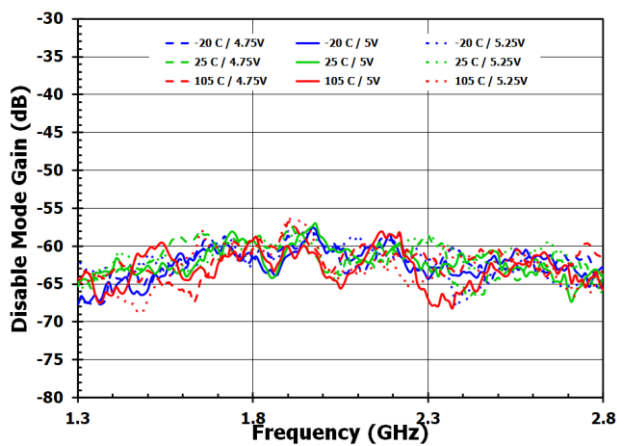


Figure 11. Disable Mode Gain

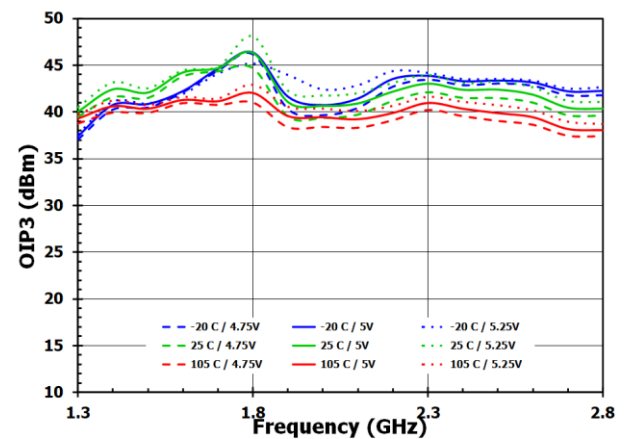


Figure 12. OIP3, DSA = 0dB, 10MHz Tone Spacing

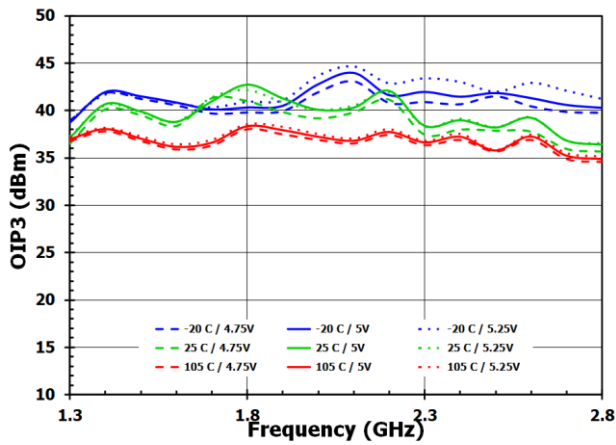


Figure 13. OIP3, DSA = 16dB, 10MHz Tone Spacing

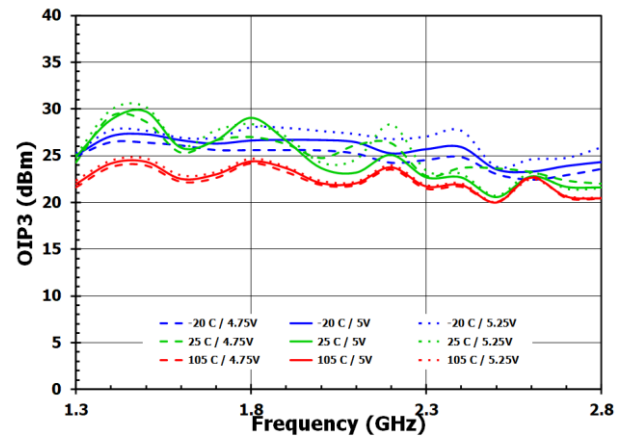


Figure 14. OIP3, DSA = 31.5dB, 10MHz Tone Spacing

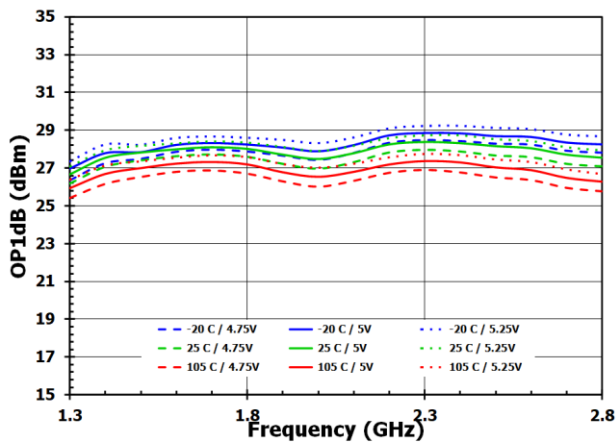


Figure 15. OP1dB, DSA = 0dB

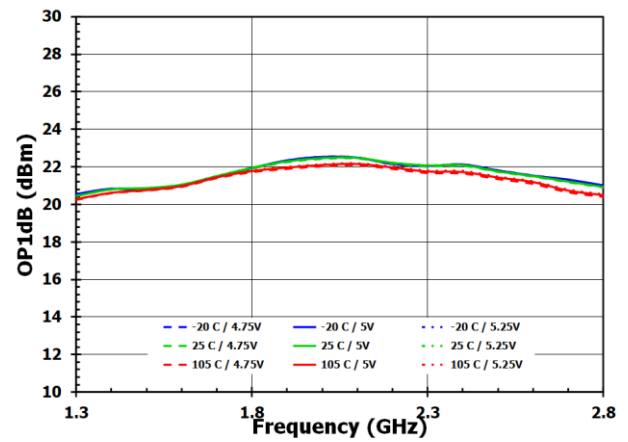


Figure 16. OP1dB, DSA = 16dB

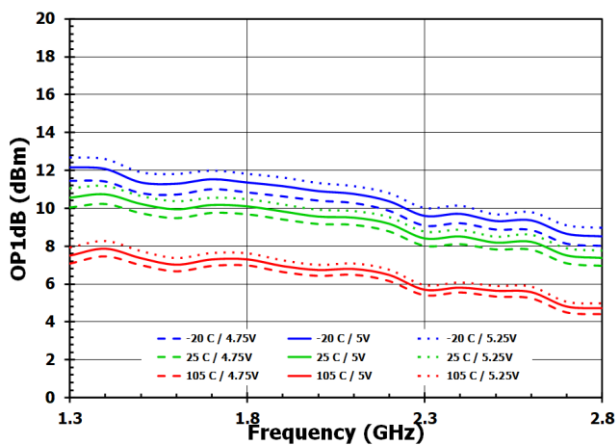


Figure 17. OP1dB, DSA = 31.5dB

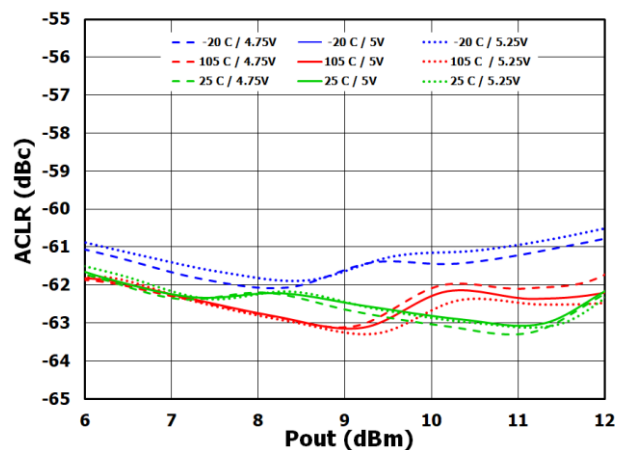


Figure 18. ACLR, DSA = 0, at 2GHz

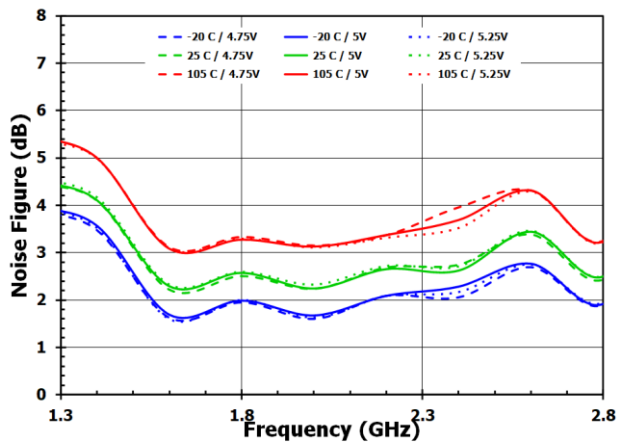


Figure 19. Noise Figure, DSA = 0dB

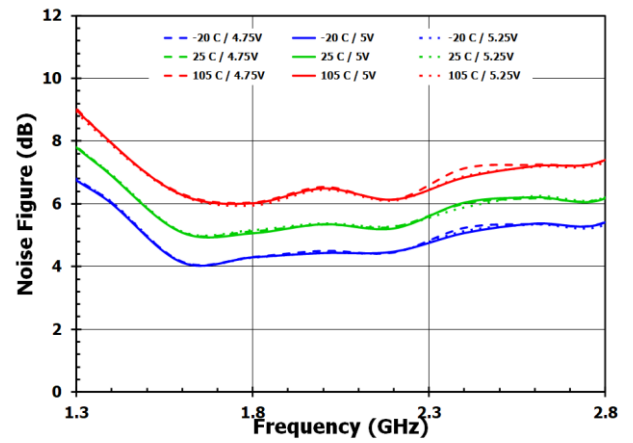


Figure 20. Noise Figure, DSA = 16dB

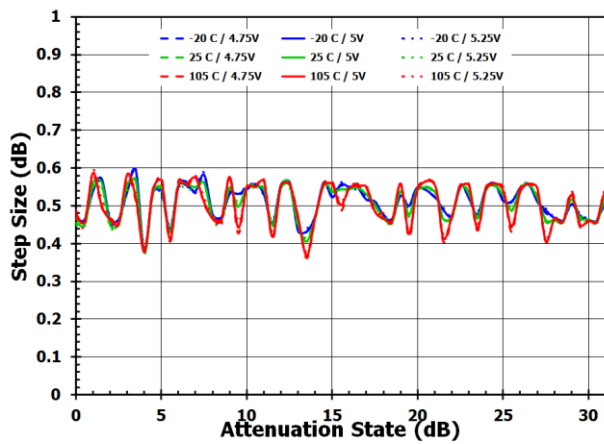


Figure 21. DSA Step Size at 2GHz

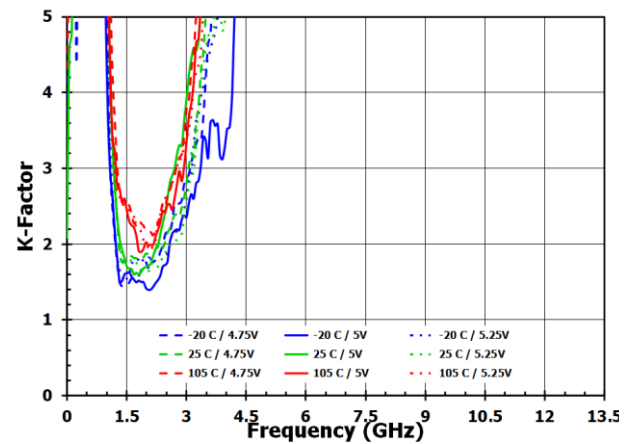


Figure 22. K-Factor

4. Functional Description

4.1 TX Enable

The F1441 can be disabled for low current consumption by applying a logic voltage to the TX_EN (pin 1) using Table 1.

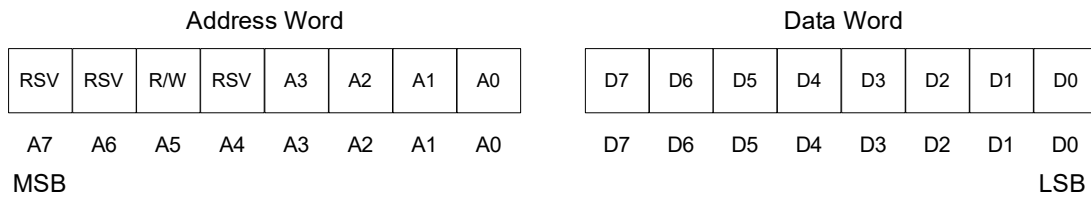
Table 1. TX Enable Truth Table

TX_EN	Condition
Logic HIGH / NC	Full operation, Amplifiers ON
Logic LOW	Amplifiers OFF, DSA set to maximum attenuation

4.2 Serial Programming

4.2.1 SPI Protocol

The F1441 includes an SPI interface that is used primarily to program the device's on-chip digital step attenuator and bias tuning functions. The SPI protocol uses an 8-bit address word followed by an 8-bit data word. The SPI bus consists of three wire signals: Serial Clock (SPI_CLK), Chip Select Bit (SPI_CS), and Serial Data (SPI_DATA). The SPI_DATA line is bi-directional mode and is used for READ and WRITE operations as defined by bit A5 in the Address word.



4.2.2 Device Register Map

4.2.2.1 Address Word Bit Definition

Bits	Name	Description
7:6	RSV	RESERVED bits. Do not care values.
5	R/W	Defines Read or Write mode. Read = 0 Write = 1
4	RSV	RESERVED bits. Do not care values.
3:0	REG_ADD	Register Address to Read or Write.

4.2.2.2 Attenuation Setting Register (DSA_SET)

The DSA_SET register sets the device attenuation setting when the DSA_CTRL pin is logic LOW.

Address: 0

Bits	Name	Type	Default	Description
7:0	ATT1	R/W	0x0	8-bit attenuation setting (MSB is bit 7).

4.2.2.3 DSA_CTRL Enabled Attenuation Setting Register (DSA_CTRL_SET)

The DSA_CTRL_SET register sets the device attenuation setting when the DSA_CTRL pin is logic HIGH.

Address: 1

Bits	Name	Type	Default	Description
7:0	ATT2	R/W	0x0	8-bit attenuation setting (MSB is bit 7).

4.2.2.4 Bias Control Register (BIAS_CTRL_SET)

Address: 2

Bits	Name	Type	Default	Description
7:0	RSV	R/W	0x0	Reserved for factory use only.

4.2.2.5 Common Controls Register (COM_CTRL_SET)

Address: 3

Bits	Name	Type	Default	Description
7:6	RSV	R/W	0x0	Reserved for factory use only.
5:3	BG_SET	R/W	0x0	Bandgap current reference setting.
2:0	PTAT_SET	R/W	0x0	PTAT current reference setting.

4.2.2.6 Driver Register - 1 (DRV1_SET)

Address: 4

Bits	Name	Type	Default	Description
7	RSV	R/W	0x0	Reserved for factory use only.
6	DRV_PTBG	R/W	0x0	Driver bias profile selection: 0 = Bandgap 1 = PTAT
5:3	RSV	R/W	0x0	Reserved for factory use only.
2:0	DRV_BIAS	R/W	0x0	Driver bias control.

4.2.2.7 Driver Register - 2 (DRV2_SET)

Address: 5

Bits	Name	Type	Default	Description
7:0	RSV	R/W	0x0	Reserved for factory use only.

4.2.2.8 Driver Register – 3 (DRV3_SET)

Address: 6

Bits	Name	Type	Default	Description
7	RSV	R/W	0x0	Reserved for factory use only.
6:5	DRV_FEED_CAP	R/W	0x0	Driver feedback cap control.
4:0	RSV	R/W	0x0	Reserved for factory use only.

4.2.2.9 Stage-1 Register (STG1_SET)

Address: 7

Bits	Name	Type	Default	Description
7:0	RSV	R/W	0x0	Reserved for factory use only.

4.2.2.10 Chip ID Register (CHIPID_SET)

Address: 8

Bits	Name	Type	Default	Description
7:6	MFR_ID	R	0x2	Axiro manufacturer ID code.
5:4	PRO_ID	R	0x1	Axiro product ID code.
3:0	DEVICE_ID	R	0x2	Axiro device ID code.

4.2.2.11 Control and Configuration Registers

Register Addresses 2 to 7 are used for device configuration as determined through factory test. The default values listed should be used and loaded after device start-up to ensure performance as shown in the datasheet.

Bits	Register Address	Type	Default	Description
7:0	2	R/W	0x80	Control Register.
7:0	3	R/W	0x24	Common Controls Register.
7:0	4	R/W	0x9C	Driver Register 1.
7:0	5	R/W	0xFA	Driver Register 2.
7:0	6	R/W	0x1F	Driver Register 3.
7:0	7	R/W	0x0	Stage 1 Register.
7:0	8	R	0x92	Chip ID Register.

4.2.3 DSA Truth Tables

For optimized DSA step size performance, a unique set of DSA settings are recommended for specific frequency ranges of operation.

Att (dB)	1.75 – 2.25GHz		1.35 – 1.75GHz		2.25 – 2.8GHz		1.75 – 2.74GHz	
	DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0 (Max Gain)	255	11111111	255	11111111	255	11111111	255	11111111
0.5	254	11111110	254	11111110	254	11111110	254	11111110
1	253	11111101	253	11111101	253	11111101	253	11111101
1.5	252	11111100	252	11111100	252	11111100	252	11111100
2	123	01111011	251	11111011	123	01111011	123	01111011
2.5	250	11111010	250	11111010	122	01111010	122	01111010
3	249	11111001	249	11111001	121	01111001	121	01111001
3.5	248	11111000	248	11111000	120	01111000	120	01111000
4	247	11110111	247	11110111	119	01110111	119	01110111
4.5	246	11110110	246	11110110	182	10110110	182	10110110
5	245	11110101	245	11110101	117	01110101	117	01110101
5.5	244	11110100	244	11110100	116	01110100	116	01110100
6	243	11110011	115	01110011	115	01110011	179	10110011
6.5	242	11110010	242	11110010	114	01110010	114	01110010
7	241	11110001	241	11110001	241	11110001	241	11110001
7.5	240	11110000	240	11110000	240	11110000	240	11110000
8	111	01101111	111	01101111	111	01101111	111	01101111
8.5	238	11101110	238	11101110	110	01101110	110	01101110
9	237	11101101	237	11101101	109	01101101	109	01101101
9.5	236	11101100	236	11101100	108	01101100	108	01101100
10	107	01101011	235	11101011	107	01101011	171	10101011
10.5	234	11101010	234	11101010	106	01101010	106	01101010
11	233	11101001	233	11101001	233	11101001	233	11101001
11.5	232	11101000	232	11101000	232	11101000	232	11101000
12	103	01100111	167	10100111	103	01100111	167	10100111
12.5	230	11100110	166	10100110	102	01100110	102	01100110
13	229	11100101	165	10100101	229	11100101	229	11100101
13.5	228	11100100	164	10100100	228	11100100	100	01100100
14	99	01100011	35	00100011	227	11100011	35	00100011
14.5	226	11100010	162	10100010	226	11100010	34	00100010

Att (dB)	1.75 – 2.25GHz		1.35 – 1.75GHz		2.25 – 2.8GHz		1.75 – 2.74GHz	
	DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
15	225	11100001	97	01100001	225	11100001	161	10100001
15.5	224	11100000	96	01100000	224	11100000	160	10100000
16	223	11011111	223	11011111	223	11011111	159	10011111
16.5	222	11011110	222	11011110	222	11011110	94	01011110
17	221	11011101	221	11011101	221	11011101	221	11011101
17.5	220	11011100	220	11011100	220	11011100	220	11011100
18	219	11011011	219	11011011	219	11011011	219	11011011
18.5	218	11011010	218	11011010	218	11011010	218	11011010
19	217	11011001	217	11011001	217	11011001	217	11011001
19.5	216	11011000	216	11011000	216	11011000	216	11011000
20	87	01010111	215	11010111	151	10010111	151	10010111
20.5	214	11010110	214	11010110	86	01010110	86	01010110
21	213	11010101	213	11010101	213	11010101	213	11010101
21.5	212	11010100	84	01010100	212	11010100	212	11010100
22	83	01010011	211	11010011	211	11010011	83	01010011
22.5	210	11010010	210	11010010	210	11010010	82	01010010
23	209	11010001	209	11010001	209	11010001	209	11010001
23.5	208	11010000	208	11010000	208	11010000	208	11010000
24	143	10001111	79	01001111	143	10001111	143	10001111
24.5	78	01001110	206	11001110	78	01001110	78	01001110
25	77	01001101	205	11001101	205	11001101	205	11001101
25.5	76	01001100	76	01001100	204	11001100	204	11001100
26	11	00001011	75	01001011	139	10001011	139	10001011
26.5	10	00001010	202	11001010	74	01001010	74	01001010
27	137	10001001	201	11001001	201	11001001	201	11001001
27.5	136	10001000	136	10001000	200	11001000	200	11001000
28	7	00000111	199	11000111	71	01000111	71	01000111
28.5	134	10000110	198	11000110	70	01000110	70	01000110
29	69	01000101	197	11000101	69	01000101	69	01000101
29.5	68	01000100	132	10000100	68	01000100	68	01000100
30	3	00000011	3	00000011	3	00000011	3	00000011
30.5	2	00000010	130	10000010	2	00000010	2	00000010
31	1	00000001	65	01000001	1	00000001	1	00000001

Att (dB)	1.75 – 2.25GHz		1.35 – 1.75GHz		2.25 – 2.8GHz		1.75 – 2.74GHz	
	DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
31.5	0	00000000	0	00000000	0	00000000	0	00000000

4.2.4 Timing Diagrams

4.2.4.1 Register Write

A register write sequence is started by asserting the SPI_CS pin to logic 0 and ends by de-asserting the SPI_CS pin to logic 1. A register write is recognized by setting the Address word bit 5 to a logic 1. Data should be clocked in MSB first.

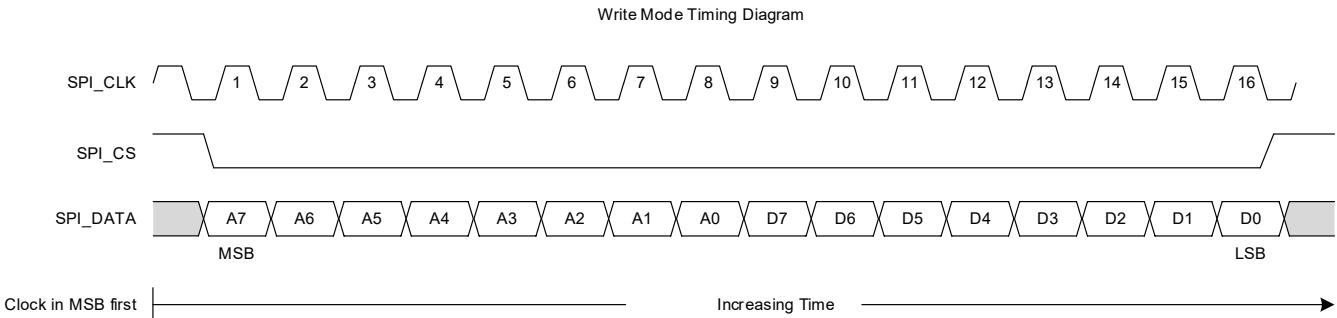


Figure 23. Write Mode Timing Diagram

4.2.4.2 Register Read

A register read sequence is started by asserting the SPI_CS pin to logic 0 and ends by de-asserting the SPI_CS pin to logic 1. A register read is recognized by setting the Address word bit 5 to a logic 0. Data should be clocked in MSB first. On a read access, data is clocked out on the next clock cycle after the last Address bit is clocked in. Note that the data output can be delayed as long as there is no SPI_CLK signal while SPI_CS is a logic 0. Data output will resume on the next active clock cycle.

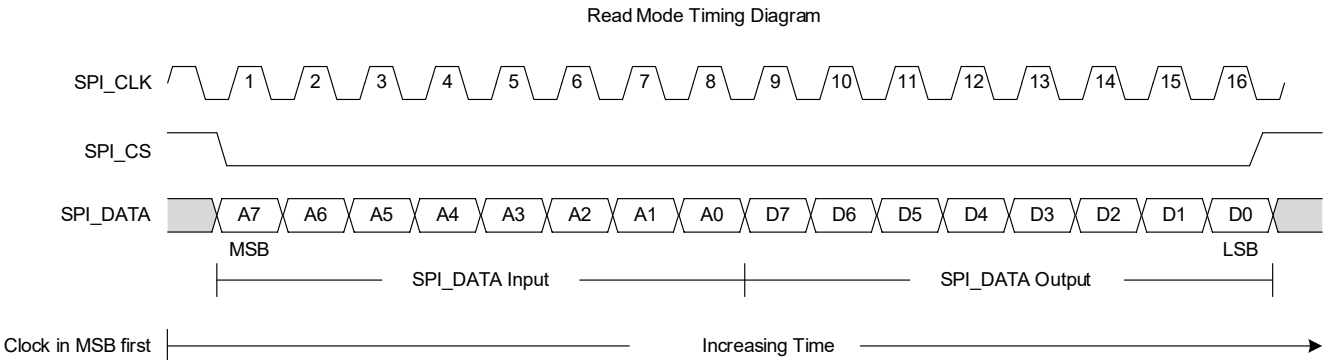


Figure 24. Read Mode Timing Diagram

4.2.4.3 SPI Timing Information

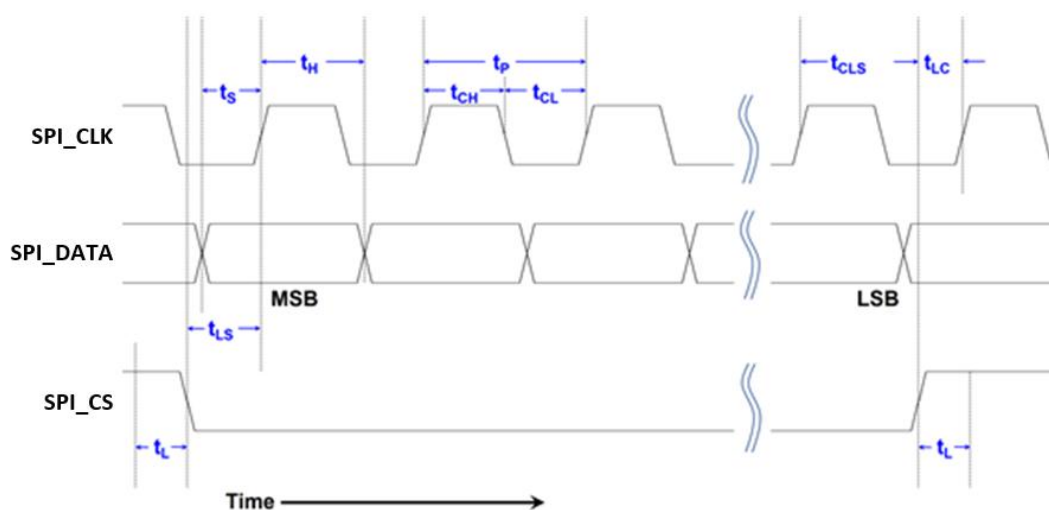


Figure 25. SPI Timing Information

Table 2. Digital Specification

Parameter	Symbol	Minimum	Maximum	Unit
CLK Frequency	f_c	-	25	MHz
CLK High Duration Time	t_{CH}	20	-	ns
CLK Low Duration Time	t_{CL}	20	-	ns
CLK Period ^[1]	t_p	40	-	ns
DATA to CLK Setup Time	t_s	10	-	ns
CLK to DATA Hold Time	t_H	10	-	ns
Final CLK Rising Edge to SPI_CS Rising Edge	t_{CLS}	10	-	ns
SPI_CS to CLK Setup Time	t_{LS}	10	-	ns
SPI_CS Trigger Pulse Width	t_L	10	-	ns
SPI_CS Trigger to CLK Setup Time ^[2]	t_{LC}	10	-	ns

1. $(t_{CH} + t_{CL}) \geq 1/f_c$.

2. Once all desired DATA is clocked in, t_{LC} represents the time SPI_CS high needs to occur before any subsequent CLK signals.

4.2.5 DSA Mode Control

The DSA_CTRL pin sets the DSA setting to a pre-programmed value by applying a logic voltage to pin 10 as defined by Table 3. The default programmed attenuation setting is 31.5dB and can be updated through an SPI command. The programmed attenuation setting is reset back to the default value when power to the device is reset.

Table 3. DSA_CTRL Truth Table

DSA_CTRL	Condition
Logic HIGH	DSA set to pre-programmed value

Logic LOW / NC	DSA setting controlled by SPI command
----------------	---------------------------------------

5. Evaluation Board (EVB) Information

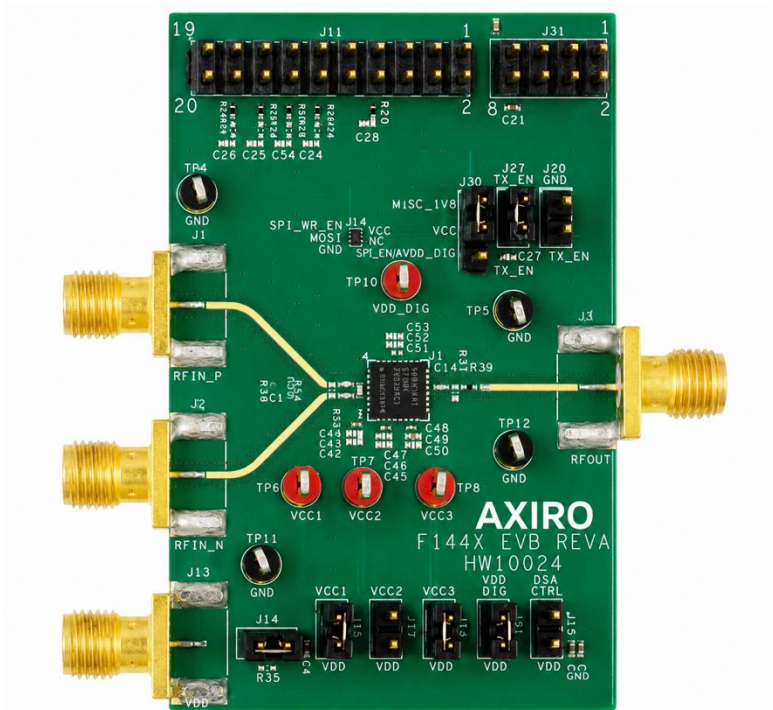


Figure 26. Evaluation Board – Front

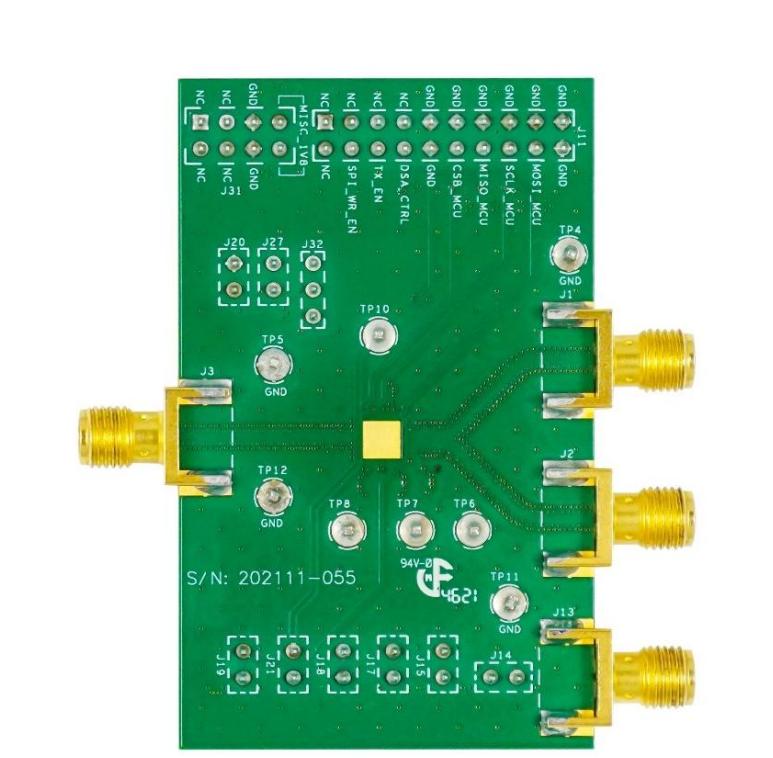


Figure 27. Evaluation Board – Back

5.1 Evaluation Board Schematic

TX_EN Operation

1. Manual Ctrl: Place J20 and Remove J27
2. FDTI Ctrl: Remove J20 and Place J27

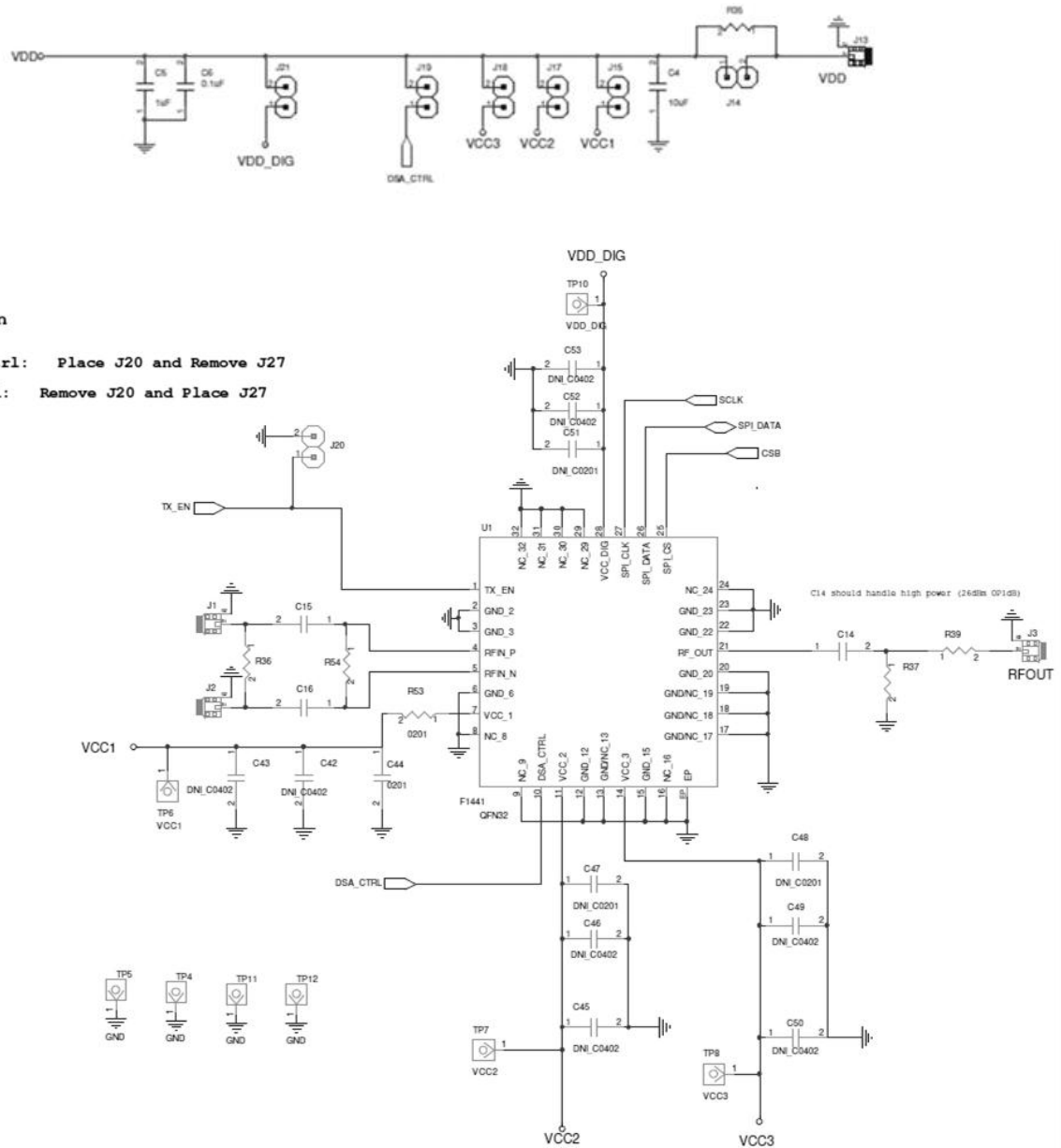
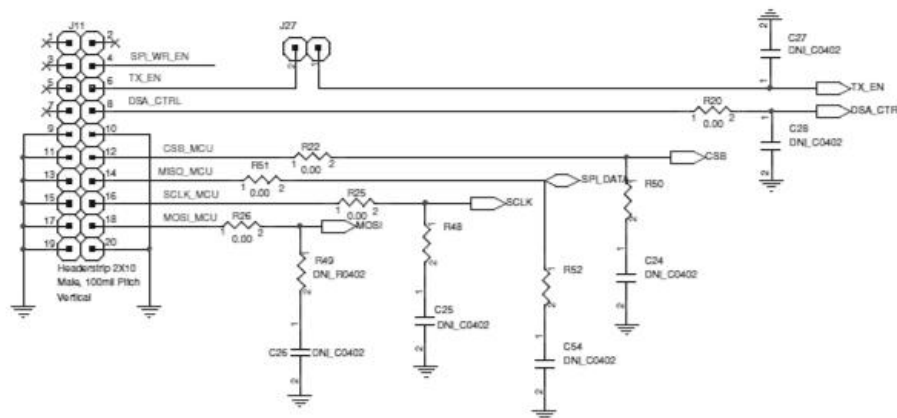


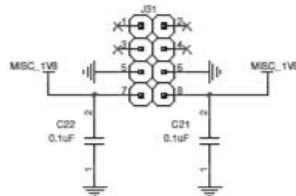
Figure 28. Evaluation Board Circuit Schematic – Image 1

Digital Control

F2232H SPI MODULE (REVC) CONNECTOR 1 (2x10)



F2232H SPI MODULE (REVC) CONNECTOR 2 (2x4)



J32 - Default Position is 1-2 (MISC_1V8)

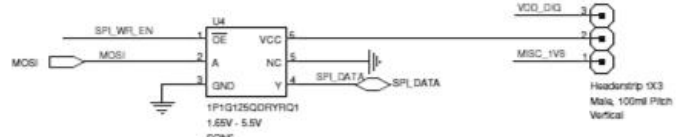


Figure 29. Evaluation Board Circuit Schematic – Image 2

5.2 Evaluation Kit (EVK) Information

For instructions on how to use the EVB and graphical user interface software, see the *F1441 EVK Manual*.

5.3 Bill of Materials

Table 4. Evaluation Board Bill of Material (BOM) – 100Ω

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C4	1	10uF ± 20%, 6.3V, X5R Surface Mount Capacitor (0402)	GRM155R60J106M	Murata Electronics
C5	1	1uF ± 10%, 25V, X5R Surface Mount Capacitor (0402)	GRM155R61A105KE15D	Murata Electronics
C6,C21,C22	3	0.1uF ± 10%, 50V, X5R Surface Mount Capacitor (0402)	GRM155R61H104K	Murata Electronics
C14	1	68pF ± 5%, 50V, X5R Surface Mount Capacitor (0402)	GRM1555C1H1680J	Murata Electronics
C15,C16	2	3pF ± 0.05%, 25V, X5R Surface Mount Capacitor (0402)	GRM1555C1H3R0WA01D	Murata Electronics
C48	1	10nF ± 10%, 50V, X5R Surface Mount Capacitor (0201)	GRM033R71E103KE14D	Murata Electronics
C49	1	100pF ± 5%, 50V, X5R Surface Mount Capacitor (0402)	GRM1555C1H101JA01D	Murata Electronics
C44	1	1uF ± 20%, 10V, X5R Surface Mount Capacitor (0201)	GRM033C81A105ME05D	Murata Electronics
C47	1	100pF ± 5%, 50V, X5R Surface Mount Capacitor (0201)	GRM0335C1H101JA01J	Murata Electronics

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C24,C25,C26,C27, C28,C42,C43,C45, C46,C50,C52,C53, C54	13	DNI_C0402	-	-
C51	1	DNI_0201	-	-
J1,J2,J3,J13	4	Cinch: SMA JACK STR 50 OHM EDGE MNT, Fits 0.062" board	142-0701-851	Cinch
J11	1	Molex: Header Dual, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240 inch contact mating length	10-89-7200	Molex
J14,J15,J17,J18,J1 9,J20,J21,J27	8	Molex: Header, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240 inch contact mating length	22-28-4023	Molex
J31	1	Molex: C-Grid Header Dual, Gold, Unshrouded, Breakaway, 100mil pitch	10-89-7080	Molex
J32	1	Molex: Header, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240 inch contact mating length	22-28-4033	Molex
R20,R22,R25,R26, R39,R51	6	0Ω 1/10W Surface Mount Resistor (0402)	ERJ-2GE0R00	Panasonic
R54	1	0.6pF ± 0.1pF, 50V, Surface Mount Capacitor (0402)	GRM1555C1HR60BA01D	Murata Electronics
R35,R36,R37,R48, R49,R50,R52	7	DNI_R0402	-	-
R53	1	2nH ±0.1nH, 600mA, Surface Mount Inductor (0201)	LQP03TN2N0B02D	Murata Electronics
TP4,TP5,TP11,TP1 2	4	Keystone Electronics: Phosphor Bronze Wire Loop, heat resistant nylon base	5006	Keystone
TP6	1	Keystone Electronics: Phosphor Bronze Wire Loop, heat resistant nylon base	5010	Keystone
TP7	1	Keystone Electronics: Phosphor Bronze Wire Loop, heat resistant nylon base	5010	Keystone
TP8	1	Keystone Electronics: Phosphor Bronze Wire Loop, heat resistant nylon base	5010	Keystone
TP10	1	Keystone Electronics: Phosphor Bronze Wire Loop, heat resistant nylon base	5010	Keystone
U1	1	Axiro:1350MHz – 2800MHz Selectable 50Ω or 100Ω DIFF-In to 50Ω SE-Out Variable Gain Amplifier 5 × 5 mm 32-VFQFPN package	F1441	Axiro
U4	1	TI: Buffer, Non-Inverting 1 Element 1 Bit per Element 3-State Output 6-SON (1.45x1)	1P1G125QDRYRQ1	Texas Instruments

Table 5. Evaluation Board Bill of Material (BOM) – 50Ω

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C4	1	10uF ± 20%, 6.3V, X5R Surface Mount Capacitor (0402)	GRM155R60J106M	Murata Electronics
C5	1	1uF ± 10%, 25V, X5R Surface Mount Capacitor (0402)	GRM155R61A105KE15D	Murata Electronics
C6,C21,C22	3	0.1uF ± 10%, 50V, X5R Surface Mount Capacitor (0402)	GRM155R61H104K	Murata Electronics
C14	1	68pF ± 5%, 50V, X5R Surface Mount Capacitor (0402)	GRM1555C1H1680J	Murata Electronics
C15,C16	2	2.4pF ± 0.05pF 50V, X5R Surface Mount Capacitor (0402)	GRM1555C1H2R4WA01D	Murata Electronics
C48	1	10nF ± 10%, 50V, X5R Surface Mount Capacitor (0201)	GRM033R71E103KE14D	Murata Electronics
C49	1	100pF ± 5%, 50V, X5R Surface Mount Capacitor (0402)	GRM1555C1H101JA01D	Murata Electronics
C44	1	1uF ± 20%, 10V, X5R Surface Mount Capacitor (0201)	GRM033C81A105ME05D	Murata Electronics
C47	1	100pF ± 5%, 50V, X5R Surface Mount Capacitor (0201)	GRM0335C1H101JA01J	Murata Electronics
C24,C25,C26,C27, C28,C42,C43,C45, C46,C50,C52,C53, C54	13	DNI_C0402	-	-
C51	1	DNI_0201	-	-
J1,J2,J3,J13	4	Cinch: SMA JACK STR 50 OHM EDGE MNT, Fits 0.062" board	142-0701-851	Cinch
J11	1	Molex: Header Dual, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240 inch contact mating length	10-89-7200	Molex
J14,J15,J17,J18,J1 9,J20,J21,J27	8	Molex: Header, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240 inch contact mating length	22-28-4023	Molex
J31	1	Molex: C-Grid Header Dual, Gold, Unshrouded, Breakaway, 100mil pitch	10-89-7080	Molex
J32	1	Molex: Header, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240 inch contact mating length	22-28-4033	Molex
R20,R22,R25,R26, R39,R51	6	0Ω 1/10W Surface Mount Resistor	ERJ-2GE0R00	Panasonic
R54	1	0.2pF ± 0.1pF, 50V, Surface Mount Capacitor (0402)	GRM1555C1HR20BA01D	Murata Electronics
R35,R37,R48,R49, R50,R52	6	DNI_R0402	-	-
R36	1	0.4pF ± 0.1pF, 50V, Surface Mount Capacitor (0402)	GRM1555C1HR40WA01D	Murata Electronics
R53	1	2nH ±0.1nH, 600mA, Surface Mount Inductor (0201)	LQP03TN2N0B02D	Murata Electronics
TP4,TP5,TP11,TP 12	4	Keystone Electronics: Phosphor Bronze Wire Loop, heat resistant nylon base	5006	Keystone
TP6	1	Keystone Electronics: Phosphor Bronze Wire Loop, heat resistant nylon base	5010	Keystone
TP7	1	Keystone Electronics: Phosphor Bronze Wire Loop, heat resistant nylon base	5010	Keystone

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
TP8	1	Keystone Electronics: Phosphor Bronze Wire Loop, heat resistant nylon base	5010	Keystone
TP10	1	Keystone Electronics: Phosphor Bronze Wire Loop, heat resistant nylon base	5010	Keystone
U1	1	Axiro:1350MHz – 2800MHz Selectable 50Ω or 100Ω DIFF-In to 50Ω SE-Out Variable Gain Amplifier 5 × 5 mm 32-VFQFPN package	F1441	Axiro
U4	1	TI: Buffer, Non-Inverting 1 Element 1 Bit per Element 3-State Output 6-SON (1.45x1)	1P1G125QDRYRQ1	Texas Instruments

6. Package Outline Drawings

The package outline drawings are accessible from the Axiro website (see package links in Ordering Information). The package information is the most current data available and is subject to change without revision of this document.

7. Marking Diagram

Top Marking Illustration	Marking	Representation
	RA81F1441STGNH	Manufacturer Part Number
	#	Die Version
	YYWW	Date code, two digits for the year and two digits for the work week
	\$	Assembly Site
	*****	Assembly Lot Number

8. Ordering Information

Part Number	Package	MSL Rating	Carrier Type	Temperature Range
RA81F1441STGNH#BB0	5.0 × 5.0 mm 32-VFQFPN	MSL1	Tray	-40°C to +105°C
RA81F1441STGNH#KB0	5.0 × 5.0mm 32-VFQFPN	MSL1	Reel	-40°C to +105°C
RTKA81F1441ST000RU	Evaluation Kit (EVK)			

Table 6. Pin 1 Orientation in Tray and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
BBO (Tray)	See illustration	
KBO (Reel)	Quadrant 2 (EIA-481-E)	

9. Revision History

Revision	Date	Description
2.00	Aug 3, 2026	Updated document branding and layout to Axiro Semiconductor standard. No changes to device functionality or specifications.