F1475

High-Linearity RF Driver Amplifier 700MHz to 2800MHz

The F1475 is a high-linearity RF Driver Amplifier designed to operate within the 700MHz to 2800MHz frequency range. Using a single 5V power supply, the F1475 provides 18.5dB typical gain and 30dBm typical OP1dB with a quiescent current consumption of 225mA at 2000MHz.

The F1475 is offered in a 4 × 4 mm, 20-VFQFPN package, with matched 50Ω input and output impedances for ease of integration into the signal path.

Competitive Advantage

- Exceptional OP1dB and linearity performance
- Compact 4 × 4 mm, 20-VFQFPN package
- Wide bandwidth with flexible tuning
- Robust ESD performance
  - 1.5kV HBM ESD rating
  - 1.5kV CDM ESD rating

Features

- Frequency range: 700MHz to 2800MHz
- 18.5dB typical gain at 2000MHz
- 30dBm typical OP1dB at 2000MHz
- 5V power supply
- 225mA typical quiescent supply current
- 1.8V logic compatible standby mode for power savings
- Operating temperature (T_{EPAD}) range: -40°C to +115°C
- 4 × 4 mm 20-VFQFPN package

Applications

- 5G Sub-6GHz Macro/AAS/Massive MIMO
- FDD or TDD systems
- General-purpose RF

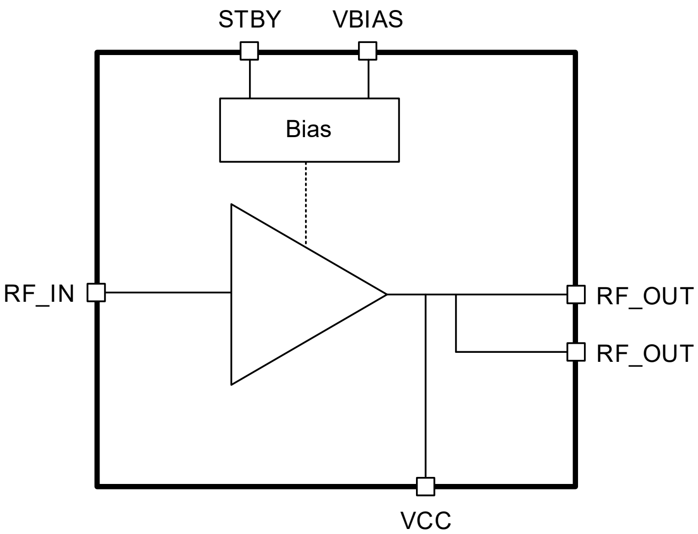

Figure 1. Block Diagram

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1. Pin Information

1.1 Pin Assignments

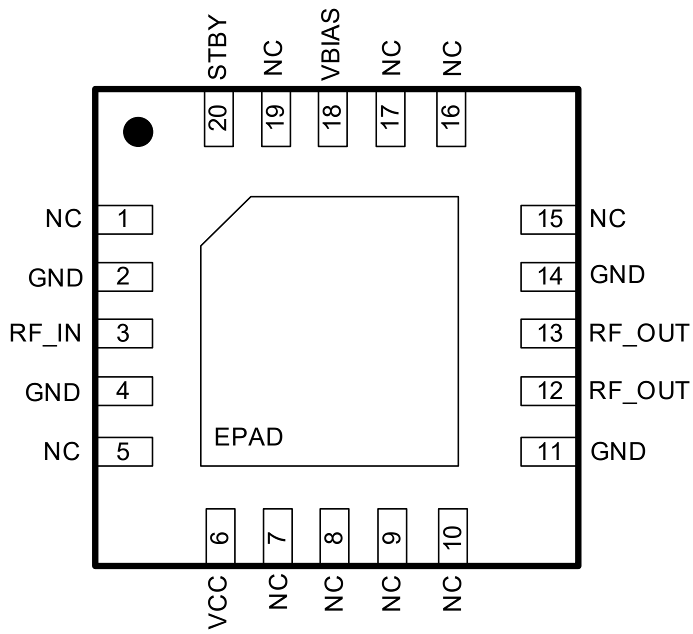


Figure 2. Pin Assignments – Top View

1.2 Pin Descriptions

Number	Name	Description
1, 5, 7, 8, 9, 10, 15, 16, 17, 19	NC	No internal connection. These pins can remain unconnected or be connected to ground (recommended). Use a via as close to the pin as possible if grounded.
2, 4, 11, 14	GND	Internally grounded. This pin must be grounded with vias as close to the pin as possible.
3	RF_IN	RF input internally matched to 50Ω. Must use an external DC block.
6	VCC	Connect pin directly to V_{CC}. Axiro recommends placing a decoupling capacitor as close to this pin as possible.
12, 13	RF_OUT	RF output. Pull up to V_{CC} through inductor. Must use an external DC block.
18	VBIAS	Connect pin via resistor to a common V_{CC}. Axiro recommends placing a decoupling capacitor as shown in the Evaluation Board Schematic in section 6.2. Place the network as close to this pin as possible.
20	STBY	Standby pin. With Logic LOW applied to this pin the amplifier is powered off. With Logic HIGH applied to this pin (or if the pin is left unconnected), the part is in full operation mode.
-	EPAD	Exposed Pad. Internally connected to ground. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the noted RF performance.

2. Specifications

2.1 Absolute Maximum Ratings

Stresses above those listed can cause permanent damage to /the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Parameter	Symbol	Minimum	Maximum	Unit
V_{CC} to GND	V_{CC}	-0.3	6.0	V
V_{BIAS} to GND	V_{BIAS}	-0.3	6.0	V
STBY	V_{STBY}	-0.3	5.0	V
RFIN Externally Applied DC Voltage	V_{RFIN}	-	2.5	V
RFOUT Externally Applied DC Voltage	V_{RFOUT}	-	6.0	V
Maximum CW Input Power applied for 24 hours. V_{CC} = 5V, T_{EPAD} = 115˚C, 50Ω system. Standby = logic HIGH: ON state. [1]	$P_{MAX\_IN\_ON}$	-	15	dBm
Maximum CW Input Power applied for 24 hours. V_{CC} = 5V, T_{EPAD} = 115˚C, 50Ω system. Standby = logic LOW: OFF state. [1]	$P_{MAX\_IN\_OFF}$	-	15	dBm
Junction Temperature	T_{JMAX}	-	175	°C
Storage Temperature Range	T_{st}	-65	150	°C
Lead Temperature (soldering, 10s)	-	-	260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2017)	V_{ESDHBM}	-	1500	V
Electrostatic Discharge – CDM (JEDEC JS-002-2022)	V_{ESDCDM}	-	1500	V

1. Exposure to these maximum RF levels can result in significantly higher ICC current draw because of overdriving the amplifier stages.

2.2 Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power Supply Voltage	V_{CC}	-	4.75	5	5.25	V
	V_{BIAS}	-	4.75	5	5.25	V
Operating Temperature Range[1]	T_{EPAD_OP}	Exposed paddle	-40	-	+115	°C
RF Frequency Range	f_{RF}	-	700	-	2800	MHz
RFIN Port Impedance	Z_{RFI}	Single-ended	-	50	-	Ω
RFOUT Port Impedance	Z_{RFO}	Single-ended	-	50	-	Ω

1. Electrical specifications are confirmed within this temperature range unless otherwise specified.

2.3 Thermal Specifications

Parameter	Symbol	Value	Unit
Junction to Ambient Thermal Resistance.	θ_{JA}	51.4	°C/W
Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	$\theta_{JC\text{-}BOT}$	27	°C/W
Moisture Sensitivity Rating (Per J-STD-020)	-	MSL1	-

2.4 Electrical Specifications

2.4.1. General Specifications

Specifications apply when operated as a TX amplifier with V_{CC} = +5.0V, V_{BIAS} = +5.0V, T_{EPAD} = +25°C, STBY = HIGH, Z_S = Z_L = 50Ω, Evaluation Board trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Logic Input High	V_{IH}	-	***1.07*** [1]	-	V_{CC}	V
Logic Input Low	V_{IL}	-	-0.3	-	***0.67***	V
Logic Current	I_{IH}, I_{IL}	STBY pin. V_{STBY} = 1.8V	***-150***	-	***150***	µA
Quiescent Current [2]	I_{CCQ}	-	-	225	***270***	mA
Standby Current	I_{CC_STBY}	STBY = LOW	-	7	-	mA
Standby Enable/Disable Settling Time	t_{SETTLE}	Settling time for disable to enable. 50% TX_EN control to RF output within 0.25dB and 1° of the on-state final value. T_{EPAD} = -40°C to +115°C, V_{CC} = +4.75V to +5.25V	-	-	1	µs
		Settling time for enable to disable. Gain shall be <5% of the Gain in enable state. T_{EPAD} = -40°C to +115°C, V_{CC} = +4.75V to +5.25V	-	-	1	µs

1. Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test.
2. I_{CCQ} refers to the nominal small signal bias current.

2.4.2. 700MHz to 900MHz Specifications

Typical specifications apply when operated as an amplifier with tuning optimized for 700MHz to 900MHz band, V_{CC} = +5.0V, V_{BIAS} = +5.0V, f_{RF} = 800MHz, T_{EPAD} = +25°C, STBY = HIGH, Z_S = Z_L = 50Ω. Minimum and maximum specifications apply across process, recommended operating voltage, full performance temperature, and tuned frequency range unless otherwise stated. Evaluation Board trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	-	-	18	-	dB
			14	-	-	dB
Gain Variation Over Process	G_{PROC}	-	-	-	±1.5	dB
Gain Variation Over Temperature	G_{TEMP}	-	-	-	+1.0/-1.5	dB
Gain Flatness	G_{FLAT}	±100MHz BW	-	-	±0.5	dB
STBY Mode Gain	G_{STBY}	STBY = logic LOW, PIN ≤ -10dBm f_{RF} = 800MHz	-	-18	-	dB
RF Input Return Loss	RL_{RFIN}	-	-	11	-	dB
RF Output Return Loss	RL_{RFOUT}	-	-	14	-	dB
Reverse Isolation	ISO_{REV}	-	-	36	-	dB
Noise Figure	NF	-	-	7.2	9.8	dB
Output Third Order Intercept Point	OIP3	Pout = +5dBm/tone up to 15dBm/tone Δf = 1MHz to 20MHz	32	38	-	dBm
		Pout = +5dBm/tone up to 15dBm/tone Δf = 100MHz	30	35	-	dBm
Output 1dB Compression Point	OP1dB	-	28	30	-	dBm
ACLR	ACLR	LTE 20MHz signal, Pout = 18dBm, 9dB PAR, CCDF = 0.01%.	-	-53	-	dBc
Stability K-Factor	K_{FACT}	f_{RF} = Up to 20GHz	1	-	-	-

2.4.3. 1350MHz to 1750MHz Specifications

Typical specifications apply when operated as an amplifier with tuning optimized for 1350MHz to 1750MHz band, V_{CC} = +5.0V, V_{BIAS} = +5.0V, f_{RF} = 1550MHz, T_{EPAD} = +25°C, STBY = HIGH, Z_S = Z_L = 50Ω. Minimum and maximum specifications apply across process, recommended operating voltage, full performance temperature, and tuned frequency range unless otherwise stated. Evaluation Board trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	-	-	18.5	-	dB
			14.5	-	-	dB
Gain Variation Over Process	G_{PROC}	-	-	-	±1.5	dB
Gain Variation Over Temperature	G_{TEMP}	-	-	-	+1.1 / -1.75	dB
Gain Flatness	G_{FLAT}	±100MHz BW	-	-	±0.4	dB
		±200MHz BW	-	-	±0.8	dB
STBY Mode Gain	G_{STBY}	STBY = logic LOW, PIN ≤ -10dBm f_{RF} = 1550MHz	-	-20	-	dB
RF Input Return Loss	RL_{RFIN}	-	-	10	-	dB
RF Output Return Loss	RL_{RFOUT}	-	-	13	-	dB
Reverse Isolation	ISO_{REV}	-	-	33	-	dB
Noise Figure	NF	-	-	4.8	7	dB
Output Third Order Intercept Point	OIP3	Pout = +5dBm/tone up to 15dBm/tone Δf = 1MHz to 20MHz	36	42	-	dBm
		Pout = +5dBm/tone up to 15dBm/tone Δf = 100MHz	33	36	-	dBm
Output 1dB Compression Point	OP1dB	-	28	30	-	dBm
ACLR	ACLR	LTE 20MHz signal, Pout = 18dBm, 9dB PAR, CCDF = 0.01%.	-	-53	-	dBc
Stability K-Factor	K_{FACT}	f_{RF} = Up to 20GHz	1	-	-	-

2.4.4. 1750MHz to 2250MHz Specifications

Typical specifications apply when operated as an amplifier with tuning optimized for 1750MHz to 2250MHz band, V_{CC} = +5.0V, V_{BIAS} = +5.0V, f_{RF} = 2000MHz, T_{EPAD} = +25°C, STBY = HIGH, Z_S = Z_L = 50Ω. Minimum and maximum specifications apply across process, recommended operating voltage, full performance temperature, and tuned frequency range unless otherwise stated. Evaluation Board trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	-	-	18.5	-	dB
			15	-	-	dB
Gain Variation Over Process	G_{PROC}	-	-	-	±1.5	dB
Gain Variation Over Temperature	G_{TEMP}	-	-	-	+1.1 / -1.75	dB
Gain Flatness	G_{FLAT}	±100MHz BW	-	-	±0.35	dB
		±200MHz BW	-	-	±0.45	dB
STBY Mode Gain	G_{STBY}	STBY = logic LOW, PIN ≤ -10dBm f_{RF} = 2000MHz	-	-18	-	dB
RF Input Return Loss	RL_{RFIN}	-	-	13	-	dB
RF Output Return Loss	RL_{RFOUT}	-	-	13	-	dB
Reverse Isolation	ISO_{REV}	-	-	32	-	dB
Noise Figure	NF	-	-	4.6	7.2	dB
Output Third Order Intercept Point	OIP3	Pout = +5dBm/tone up to 15dBm/tone Δf = 1MHz to 20MHz	36	42	-	dBm
		Pout = +5dBm/tone up to 15dBm/tone Δf = 100MHz	31	37	-	dBm
Output 1dB Compression Point	OP1dB	-	28	30	-	dBm
ACLR	ACLR	LTE 20MHz signal, Pout = 18dBm, 9dB PAR, CCDF = 0.01%.	-	-51	-	dBc
Stability K-Factor	K_{FACT}	f_{RF} = Up to 20GHz	1	-	-	-

2.4.5. 2300MHz to 2800MHz Specifications

Typical specifications apply when operated as an amplifier with tuning optimized for 2300MHz to 2800MHz band, V_{CC} = +5.0V, V_{BIAS} = +5.0V, f_{RF} = 2600MHz, T_{EPAD} = +25°C, STBY = HIGH, Z_S = Z_L = 50Ω. Minimum and maximum specifications apply across process, recommended operating voltage, full performance temperature, and tuned frequency range unless otherwise stated. Evaluation Board trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	-	-	17.5	-	dB
			14	-	-	dB
Gain Variation Over Process	G_{PROC}	-	-	-	±1.5	dB
Gain Variation Over Temperature	G_{TEMP}	-	-	-	+1.3 / -2.2	dB
Gain Flatness	G_{FLAT}	±100MHz BW	-	-	±0.3	dB
		±200MHz BW	-	-	±0.5	dB
STBY Mode Gain	G_{STBY}	STBY = logic LOW, PIN ≤ -10dBm f_{RF} = 2600MHz	-	-17	-	dB
RF Input Return Loss	RL_{RFIN}	-	-	11	-	dB
RF Output Return Loss	RL_{RFOUT}	-	-	10	-	dB
Reverse Isolation	ISO_{REV}	-	-	32	-	dB
Noise Figure	NF	-	-	4.5	7.2	dB
Output Third Order Intercept Point	OIP3	Pout = +5dBm/tone up to 15dBm/tone Δf = 1MHz to 20MHz	33	39	-	dBm
		Pout = +5dBm/tone up to 15dBm/tone Δf = 100MHz	31	37	-	dBm
Output 1dB Compression Point	OP1dB	-	27	30	-	dBm
ACLR	ACLR	LTE 20MHz signal, Pout = 18dBm, 9dB PAR, CCDF = 0.01%.	-	-50	-	dBc
Stability K-Factor	K_{FACT}	f_{RF} = Up to 20GHz	1	-	-	-

3. Typical Operating Conditions

Unless otherwise noted, the following conditions apply for the TOC graphs on the following pages:

- V_{CC} = +5.0V
- Z_L = Z_S = 50Ω Single-ended
- T_{EPAD} = +25°C
- All temperatures are referenced to the exposed paddle
- ACLR measurements used with LTE signal, 20MHz, PAR = 9dB at 0.01% probability
- Evaluation Board traces and connector losses are de-embedded

4. Typical Performance Characteristics

4.1 700MHz to 900MHz

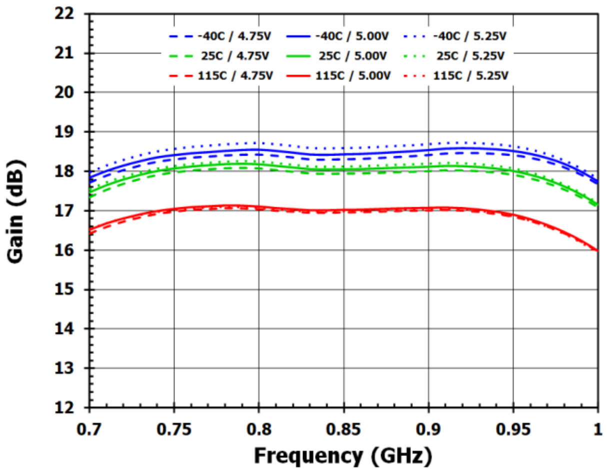


Figure 3. Gain

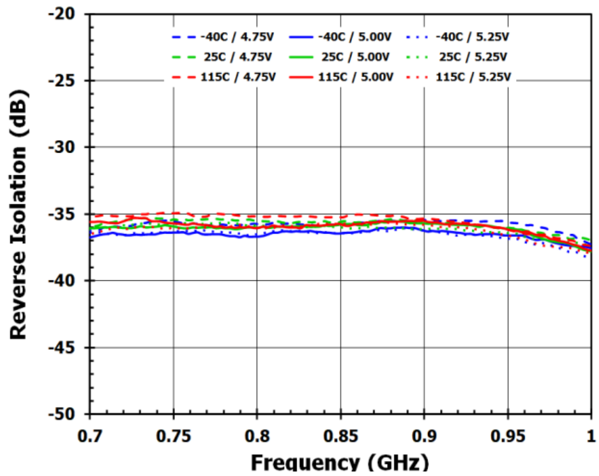


Figure 4. Reverse Isolation

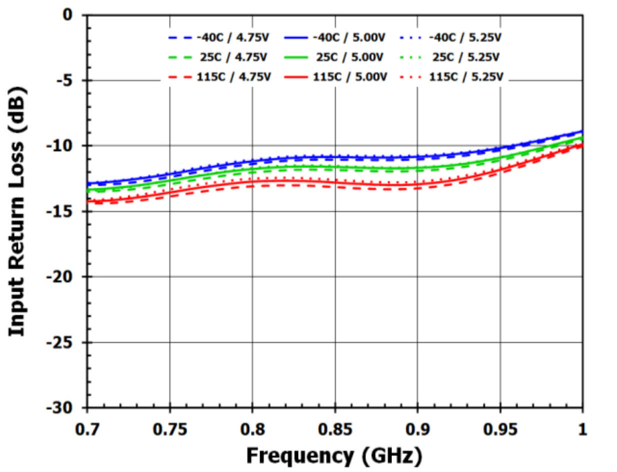


Figure 5. Input Return Loss

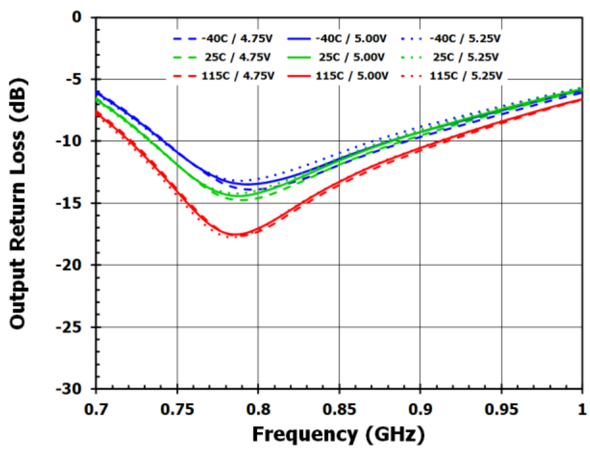


Figure 6. Output Return Loss

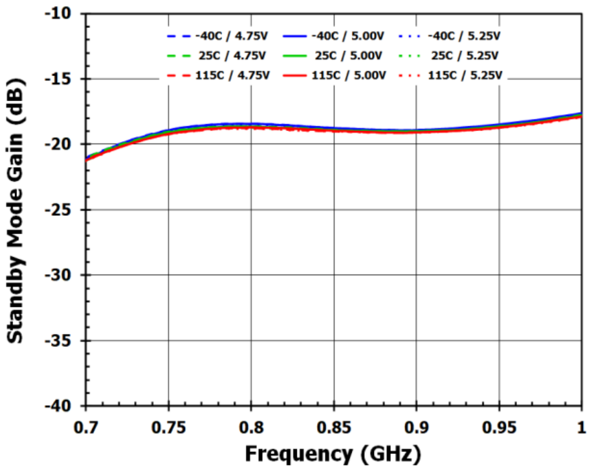


Figure 7. Standby Mode Gain

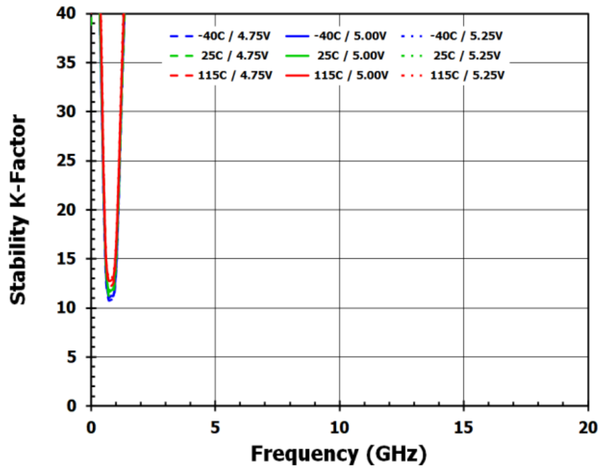


Figure 8. Stability K-Factor

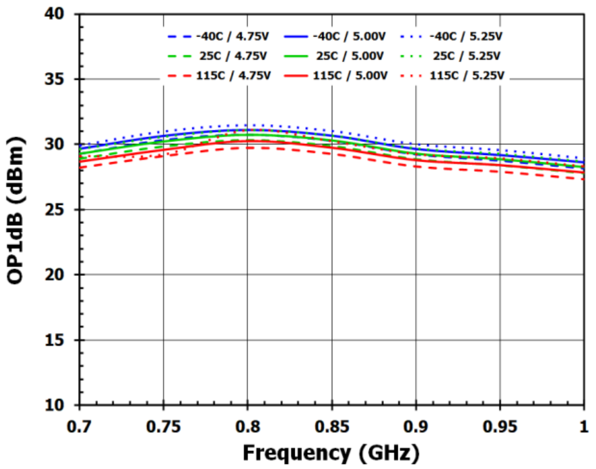


Figure 9. OP1dB

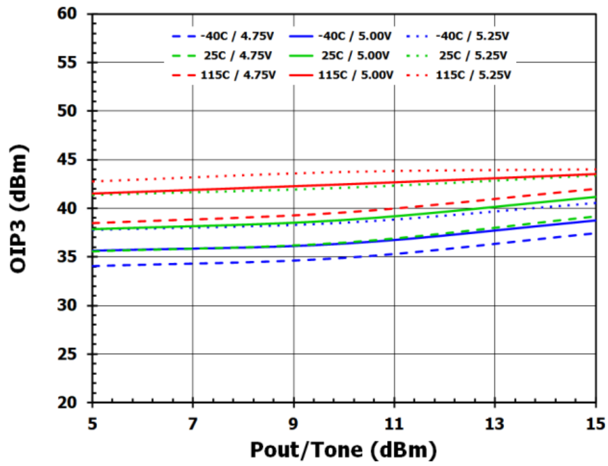


Figure 10. OIP3 – Frequency = 0.8GHz, Δf = 1MHz

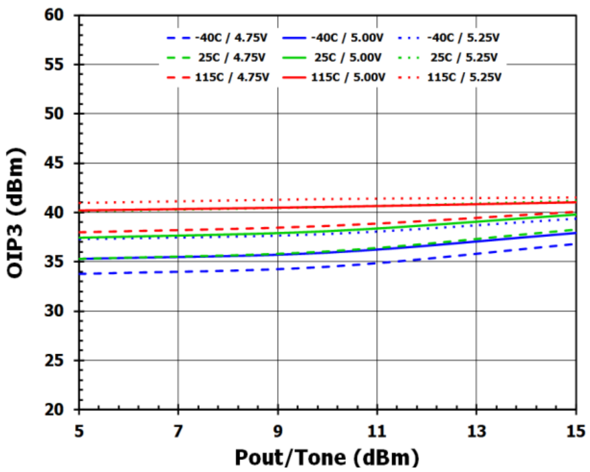


Figure 11. OIP3 – Frequency = 0.8GHz, Δf = 20MHz

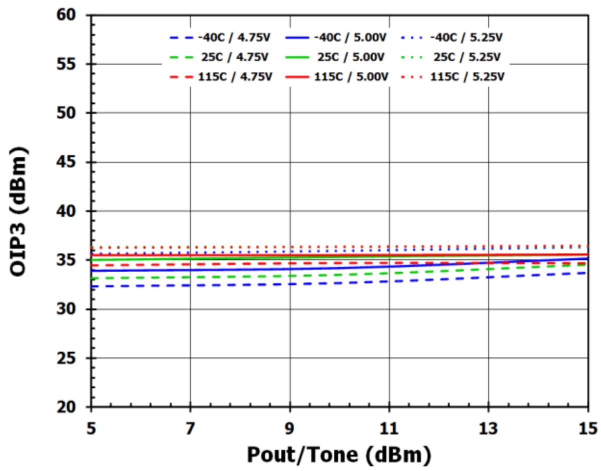


Figure 12. OIP3 – Frequency = 0.8GHz, Δf = 100MHz

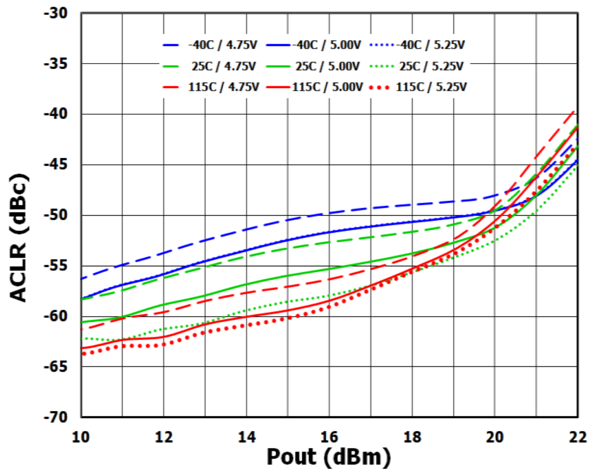


Figure 13. ACLR – Frequency = 0.8GHz, LTE 20MHz

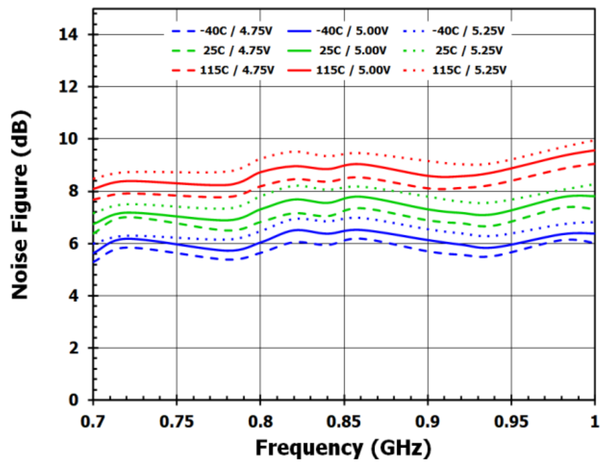


Figure 14. Noise Figure

4.2 1350MHz to 1750MHz

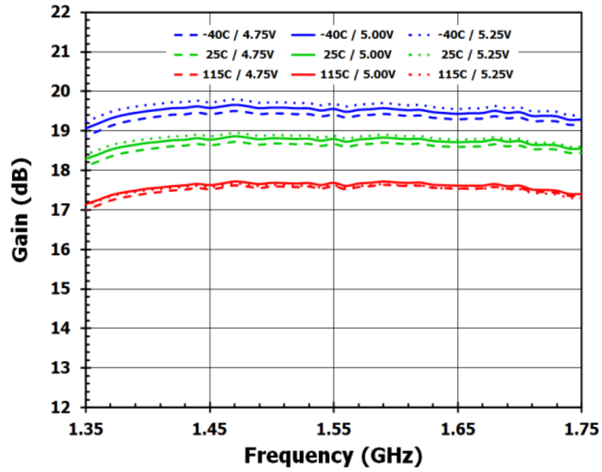


Figure 15. Gain

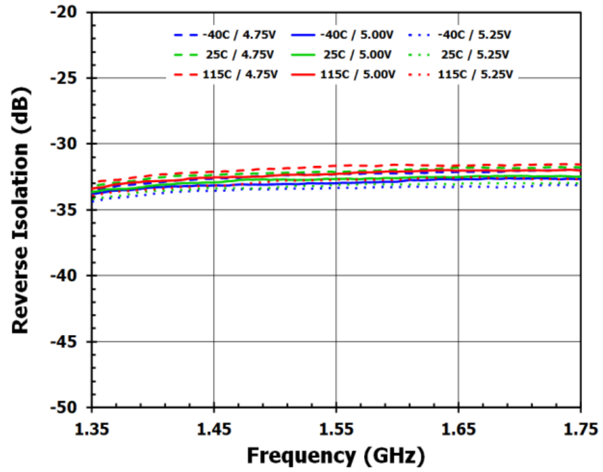
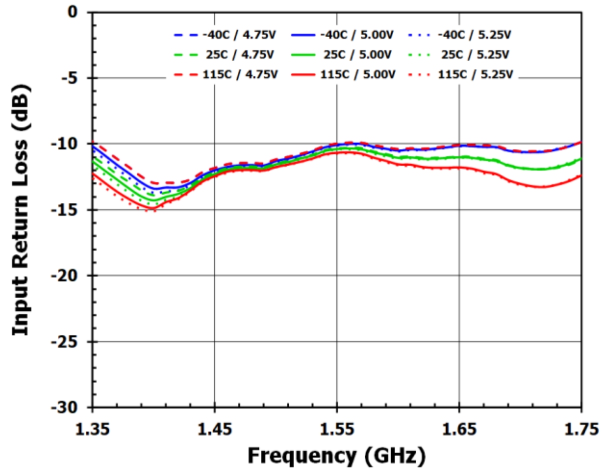


Figure 16. Reverse Isolation



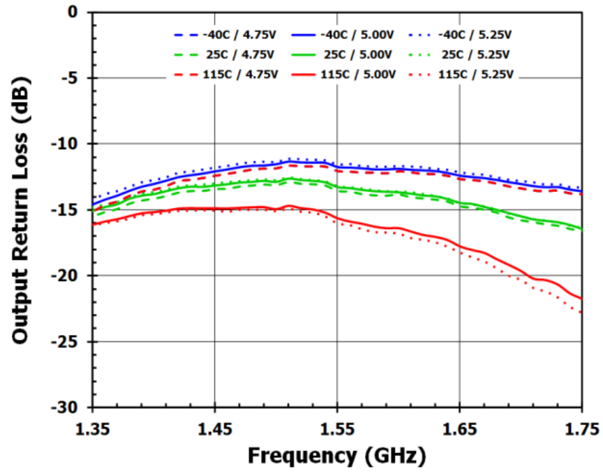


Figure 17. Input Return Loss

Figure 18. Output Return Loss

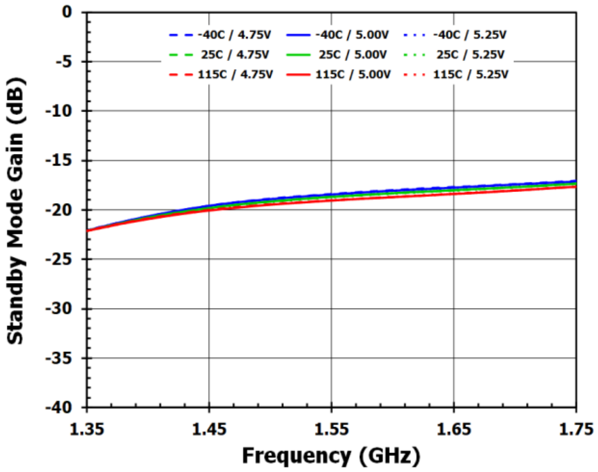


Figure 19. Standby Mode Gain

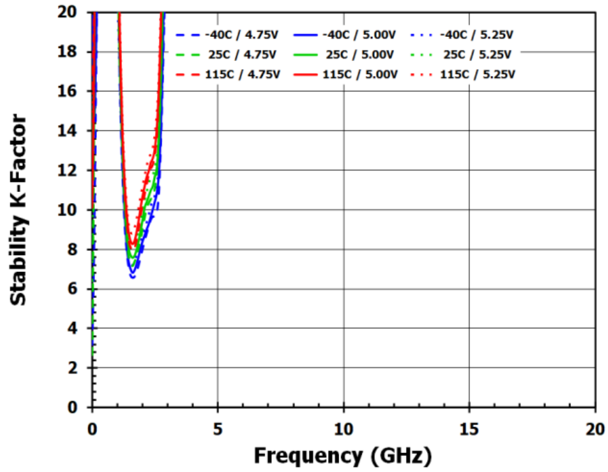


Figure 20. Stability K-Factor

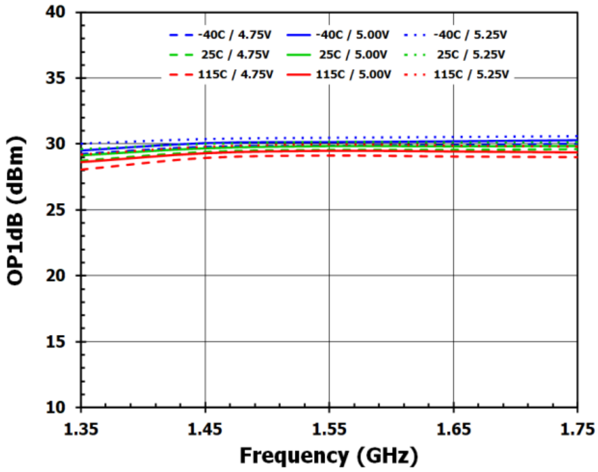


Figure 21. OP1dB

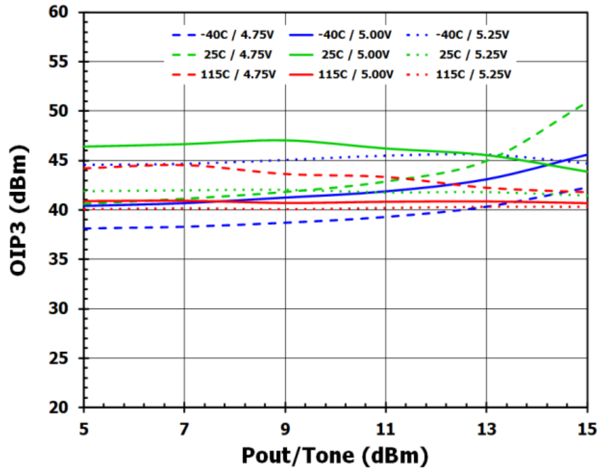
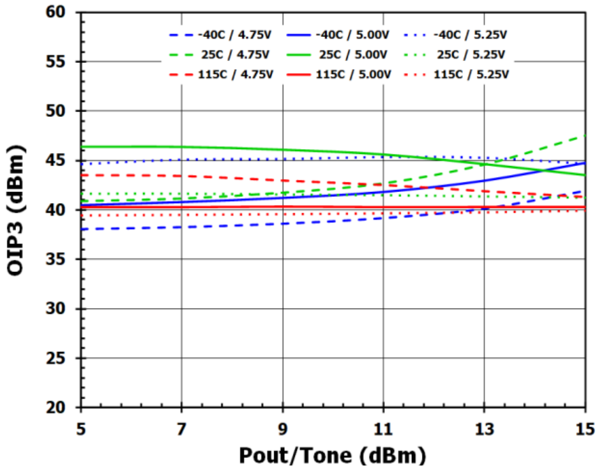


Figure 22. OIP3 – Frequency = 1.55GHz, Δf = 1MHz



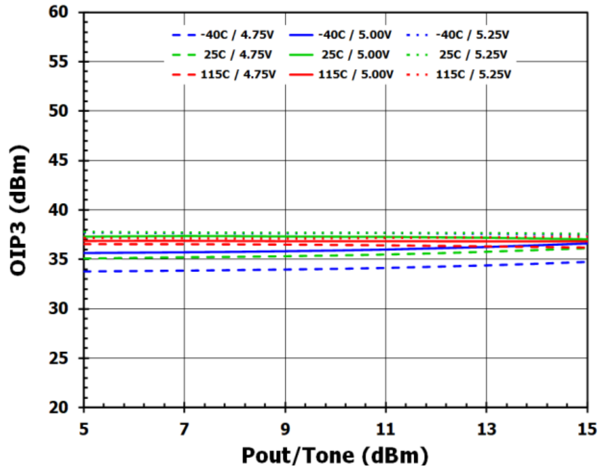


Figure 23. OIP3 – Frequency = 1.55GHz, Δf = 20MHz

Figure 24. OIP3 – Frequency = 1.55GHz, Δf = 100MHz

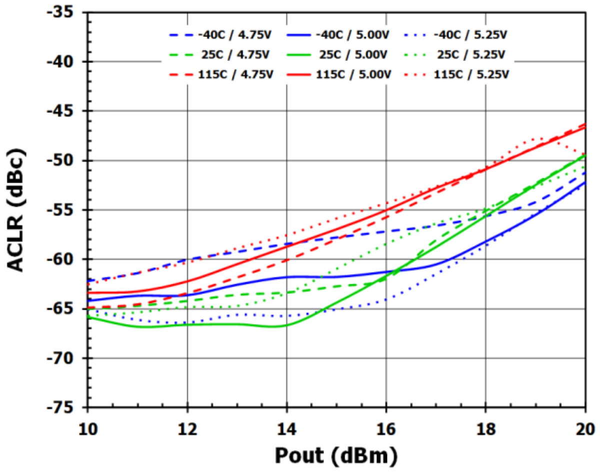


Figure 25. ACLR – Frequency = 1.55GHz, LTE 20MHz

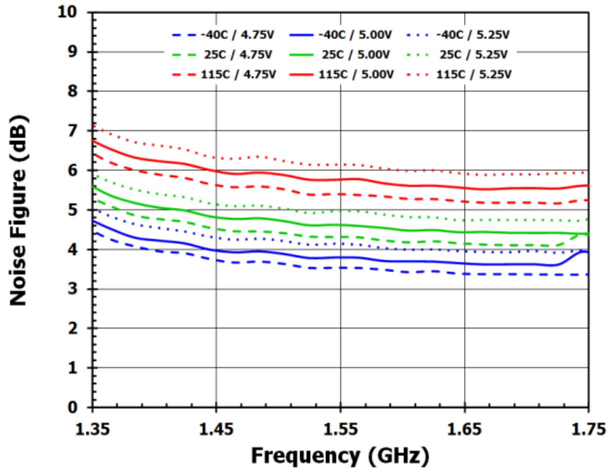


Figure 26. Noise Figure

4.3 1750MHz to 2250MHz

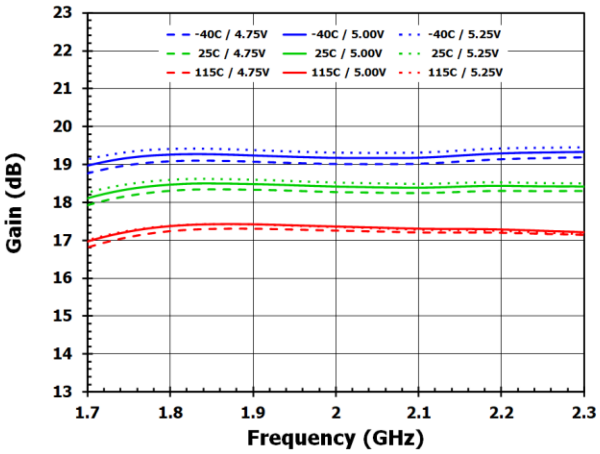


Figure 27. Gain

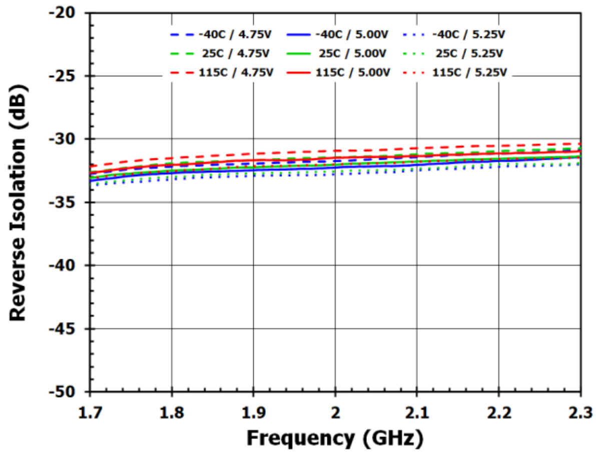


Figure 28. Reverse Isolation

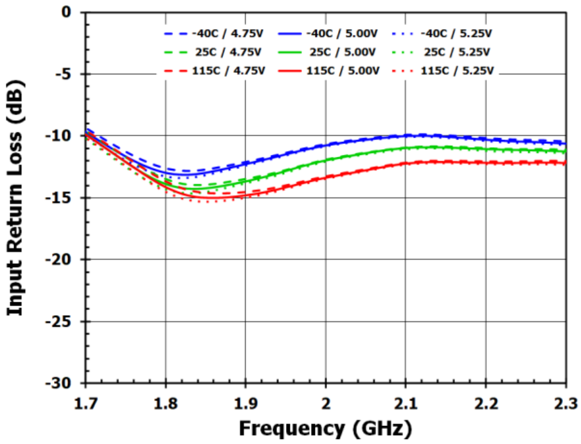


Figure 29. Input Return Loss

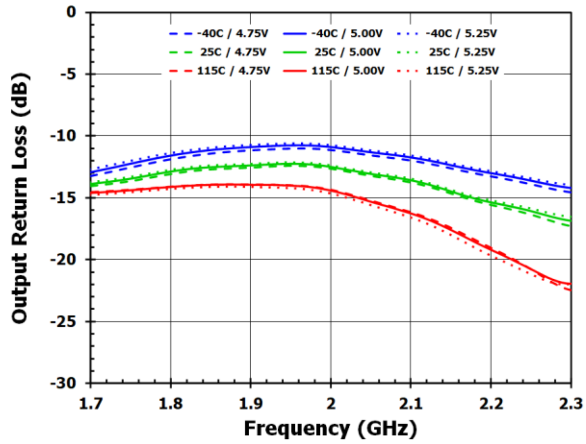


Figure 30. Output Return Loss

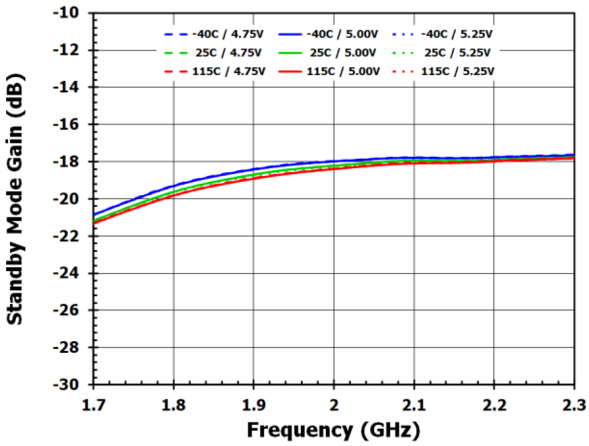


Figure 31. Standby Mode Gain

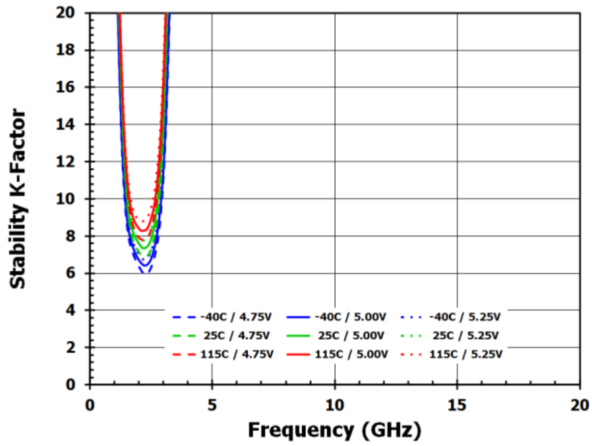


Figure 32. Stability K-Factor

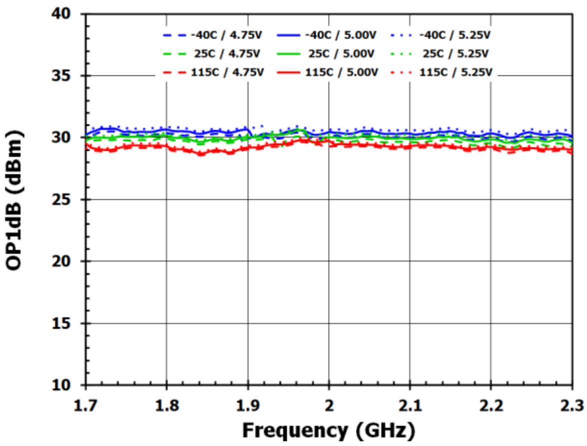


Figure 33. OP1dB

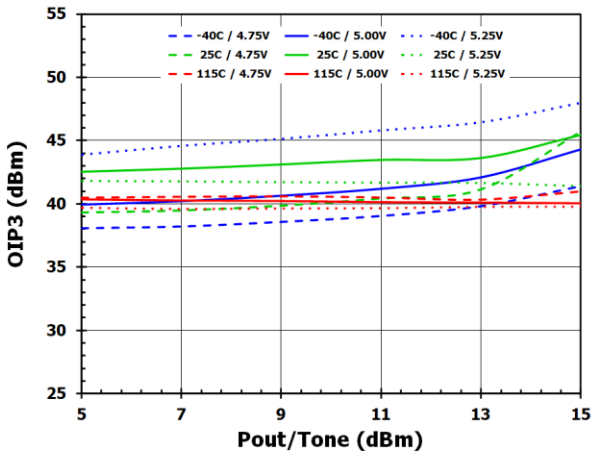


Figure 34. OIP3 – Frequency = 2GHz, Δf = 1MHz

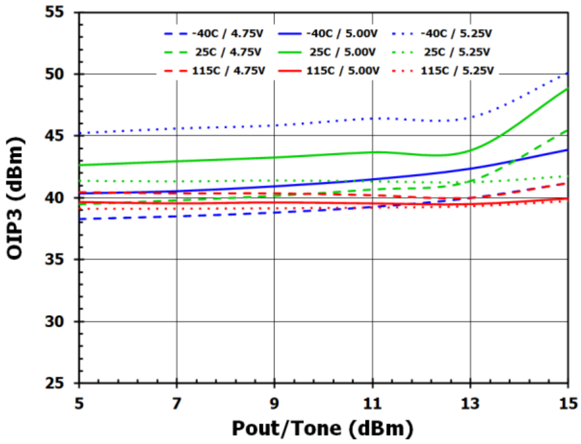


Figure 35. OIP3 – Frequency = 2GHz, Δf = 20MHz

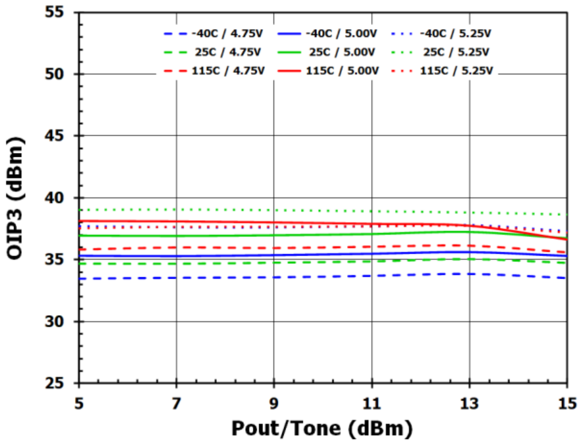


Figure 36. OIP3 – Frequency = 2GHz, Δf = 100MHz

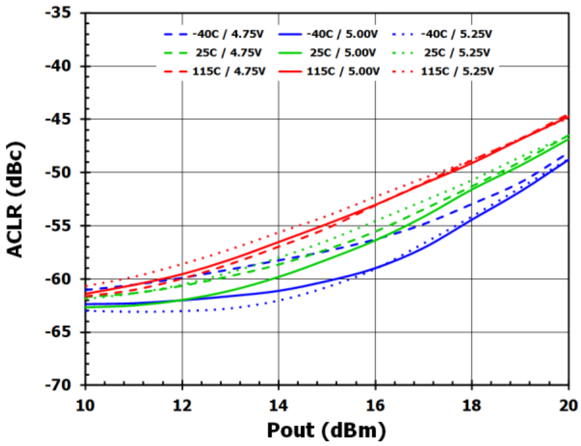


Figure 37. ACLR – Frequency = 2GHz, LTE 20MHz

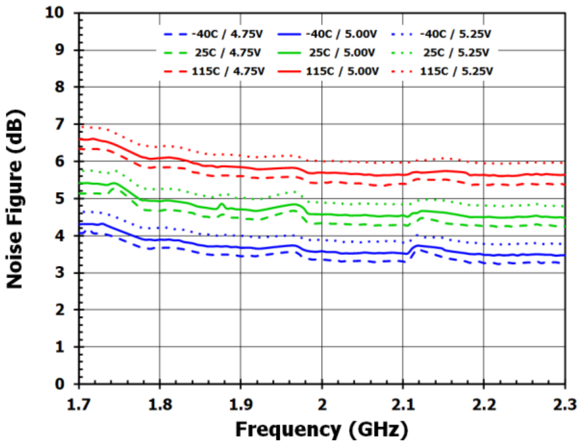


Figure 38. Noise Figure

4.4 2300MHz to 2800MHz

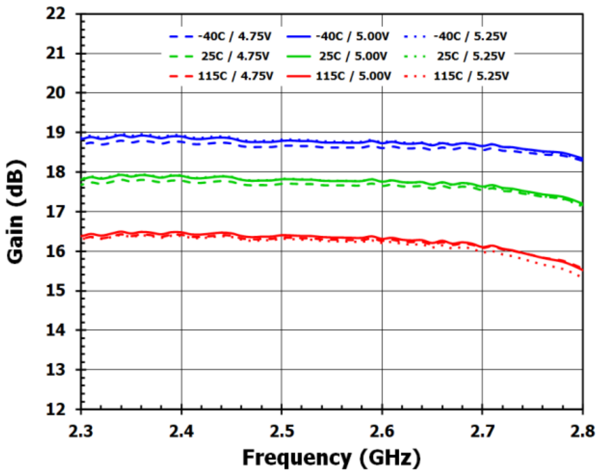


Figure 39. Gain

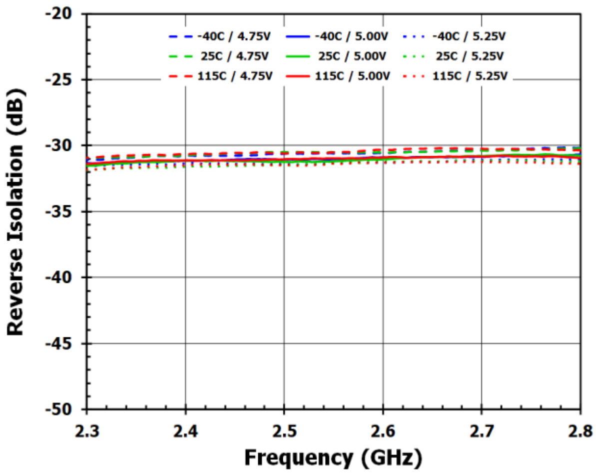


Figure 40. Reverse Isolation

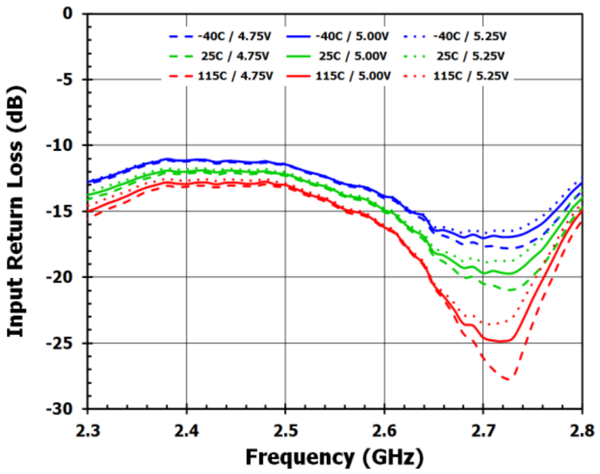


Figure 41. Input Return Loss

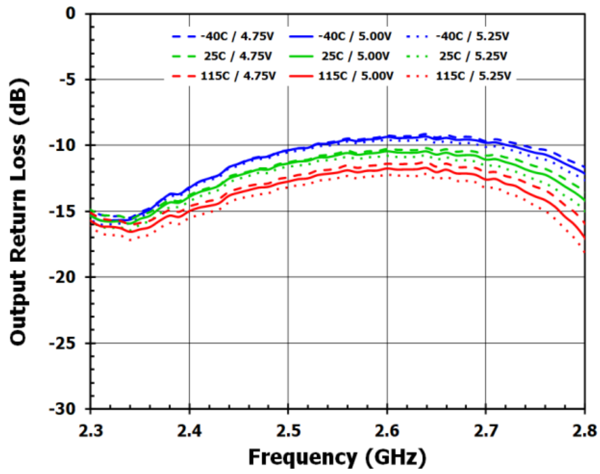


Figure 42. Output Return Loss

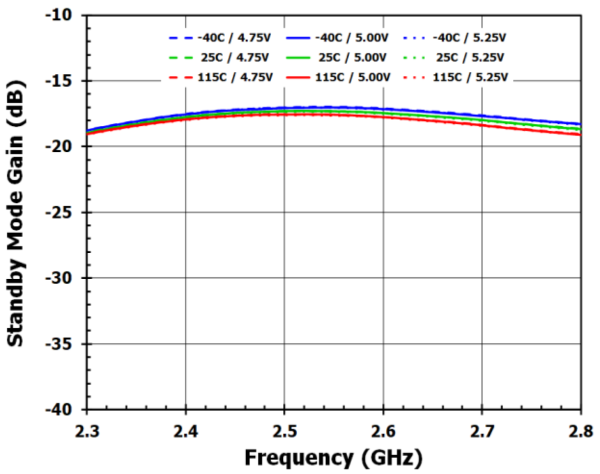


Figure 43. Standby Mode Gain

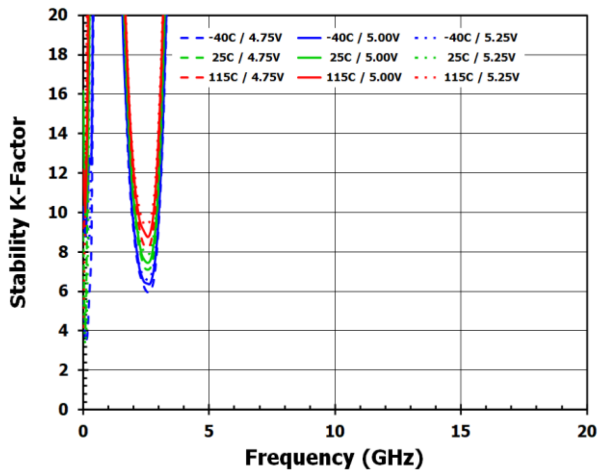


Figure 44. Stability K-Factor

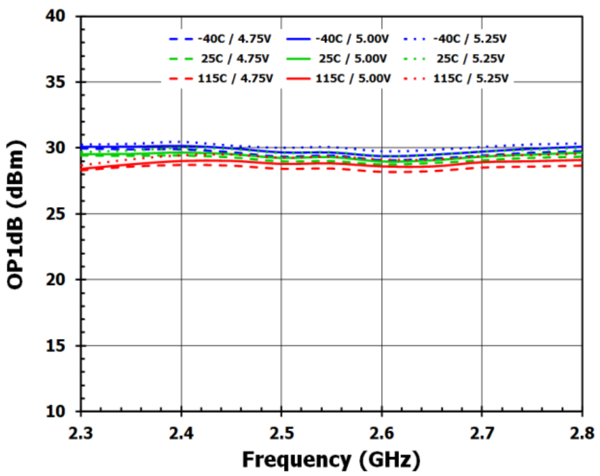


Figure 45. OP1dB

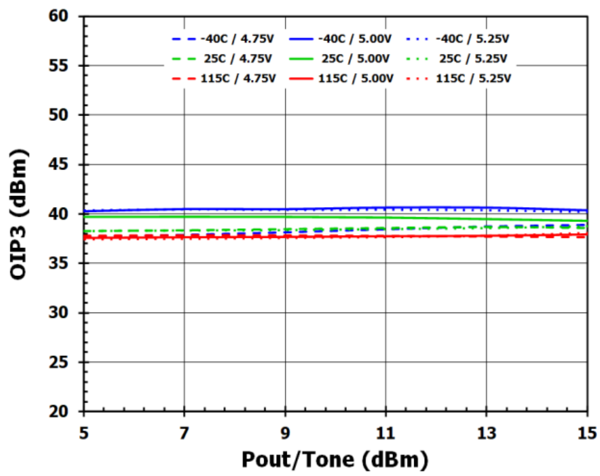


Figure 46. OIP3 – Frequency = 2.6GHz, Δf = 1MHz

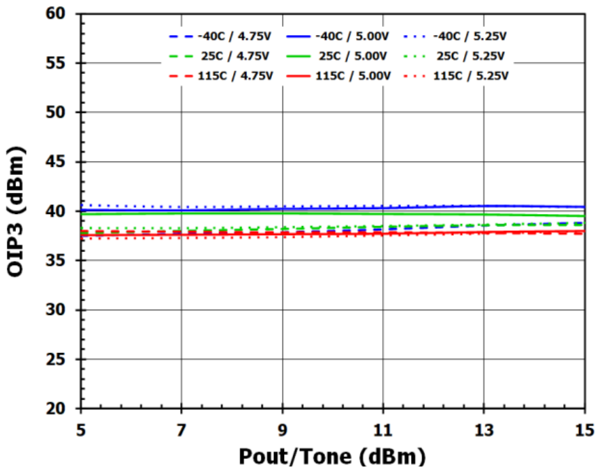


Figure 47. OIP3 – Frequency = 2.6GHz, Δf = 20MHz

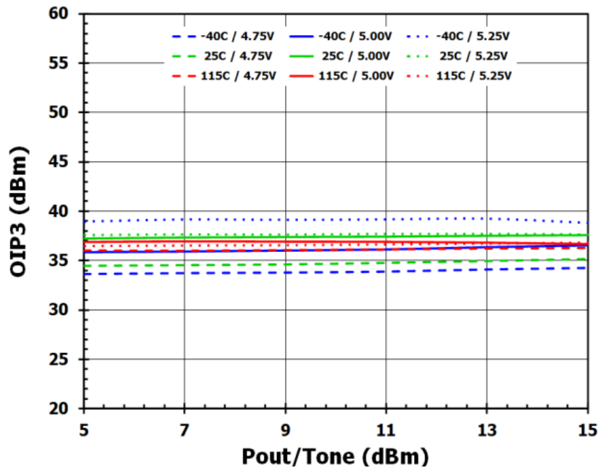


Figure 48. OIP3 – Frequency = 2.6GHz, Δf = 100MHz

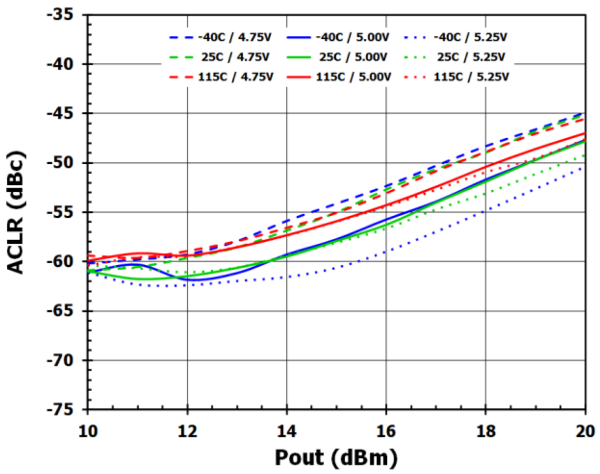


Figure 49. ACLR – Frequency = 2.6GHz, LTE 20MHz

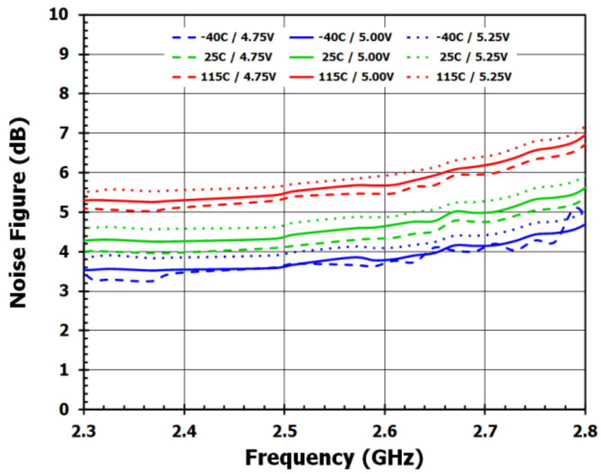


Figure 50. Noise Figure

5. Functional Information

The F1475 includes a STBY feature.

Table 1. STBY Truth Table

STBY	State
Logic HIGH or NC	Full Operation
Logic LOW	Amplifier OFF

6. Evaluation Board Information

6.1 Evaluation Board

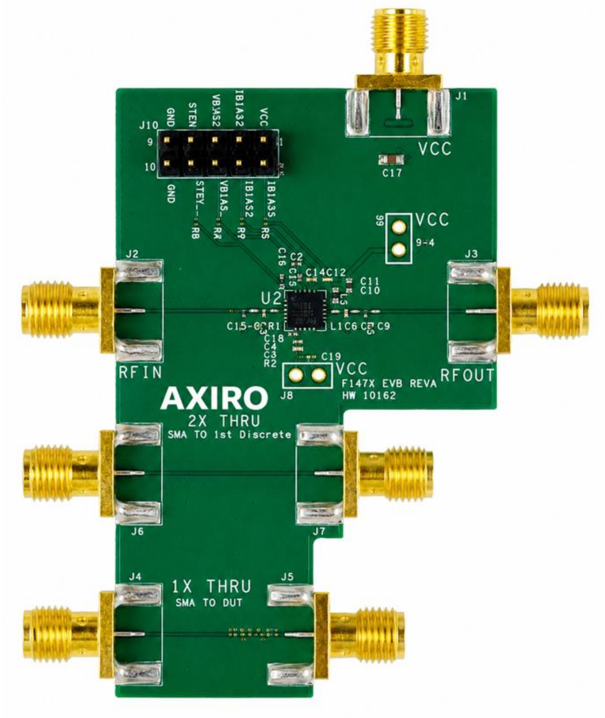


Figure 51. Evaluation Board – Top View

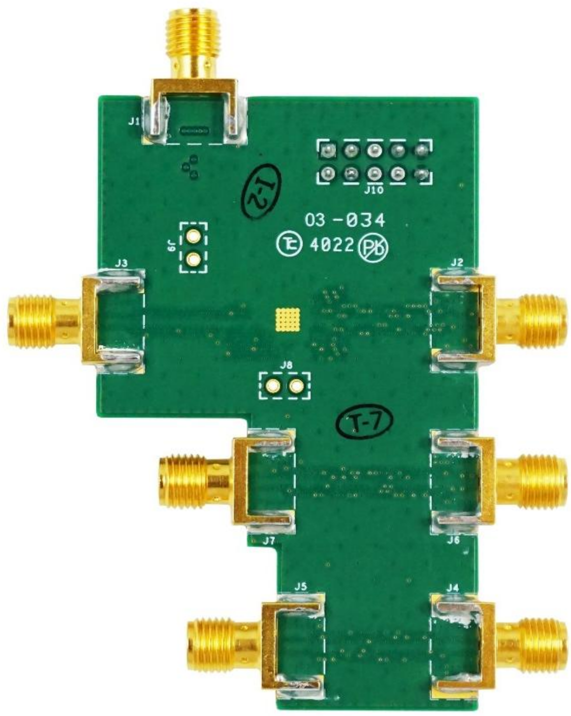
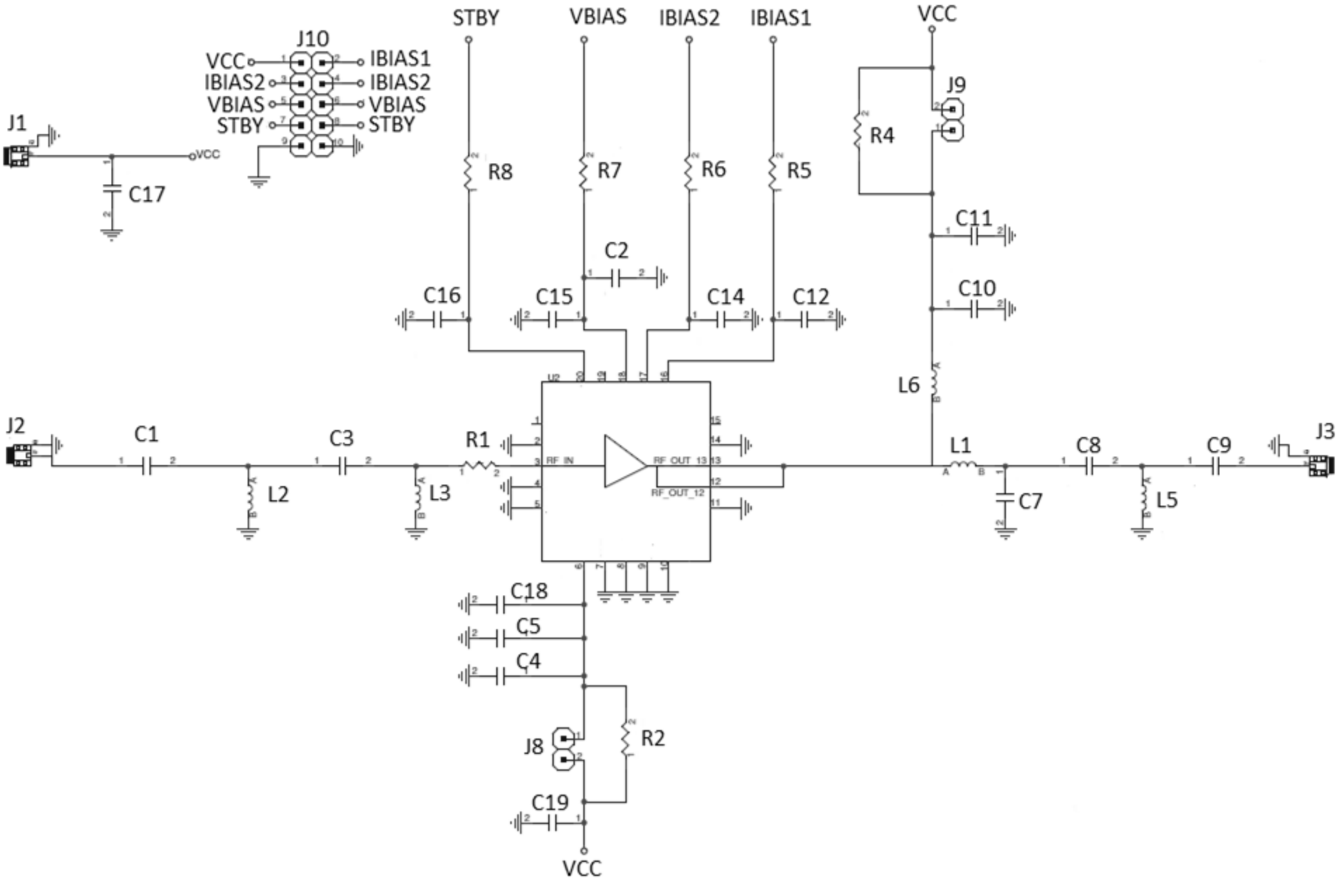


Figure 52. Evaluation Board – Bottom View



6.2 Evaluation Board Schematic

Figure 53. Evaluation Board Schematic

6.3 Bill of Materials

6.3.1. 700MHz to 900MHz

Reference Designator	Qty	Description	Manufacturer Part Number	Manufacturer
R2, R3, R4, R8, C13, C6	6	0 Ohm, RES SMD 1/20W JUMPER (0201)	ERJ1GN0R00C	Panasonic
R1	1	0.6nH ±0.05nH, 1100mA, Thich Film inductor (0201)	LQP03HQ0N6W02	Murata
R7	1	1kOhm, ±0.5%, 0.05W, Chip Resistor (0201)	ERJ1RHD1001C	Panasonic
L1	1	0 Ohm, RES SMD 1/20W JUMPER (0201)	ERJ1GN0R00C	Panasonic
L2	1	3.9nH ±0.1nH, 350mA, Thick Film Inductor (0201)	LQP03TG3N9B02	Murata
L3	1	22pF ±5%, Ceramic Capacitor,25V (0201)	GRM0335C1E220JD01B	Murata
L5	1	5.6nH ±5%, 250mA, Thick Film Inductor (0201)	LQP03TG5N6H02	Murata

Reference Designator	Qty	Description	Manufacturer Part Number	Manufacturer
L6	1	8.2nH ±5%, 300mA, Thick Film Inductor (0402)	LQG15HS8N2J02	Murata
C1	1	15 Ohm ±1%, 0.05W, Chip Resistor (0201)	CRCW020115R0FNED	Vishay Dale
C3	1	11pF ±2%, Ceramic Capacitor,50V (0201)	GJM0335C1H110GB01	Murata
C7	1	5pF ±0.25pF, Ceramic Capacitor,25V (0201)	GRM0335C1E5R0CD01B	Murata
C8	1	6pF ±0.5pF, Ceramic Capacitor,25V (0201)	GRM0335C1E6R0DD01B	Murata
C9	1	22pF ±5%, Ceramic Capacitor,25V (0201)	GRM0335C1E220JD01B	Murata
C10	1	1000pF ±5%, Ceramic Capacitor, 50V (0201)	GRM0335C1H102JE01	Murata
C11	1	100nF, Ceramic Capacitor, 25V (0201)	GRM033C81E104ME14	Murata
C5, C15, C16	3	100pF ±5%, Ceramic Capacitor, 50V (0201)	GRM0335C1H101JA01	Murata
C17	1	4.7µF ±10%, Ceramic Capacitor, 25V (0603)	GRM188C81E475KE11	Murata
C2, C4, C12, C14, C18, R5, R6, L4, L7, J8, J9	11	DNI	-	-
J1, J2, J3	3	Edge Launch SMA (0.375-inch pitch ground, tab), 50 Ohm	142-0701-851	Emerson Johnson
J10	1	Vertical Header Strip 2x5, Male, 100mil Pitch	-	Any Vendor
EVK	1	F147X EVB REVA	-	Axiro
Module	1	RA81F1475SEG	-	Axiro

6.3.2. 1350MHz to 1750MHz

Reference Designator	Qty	Description	Manufacturer Part Number	Manufacturer
R2, R3, R4, R8, C13, C6	6	0 Ohm, RES SMD 1/20W JUMPER (0201)	ERJ1GN0R00C	Panasonic
R1	1	18pF ±2%, Ceramic Capacitor,25V (0201)	GJM0335C1E180GB01	Murata
R7	1	1kOhm, ±1%, 0.05W, Chip Resistor (0201)	ERJ1GNF1001C	Panasonic
L1	1	47pF ±2%, Ceramic Capacitor,50V (0201)	GRM0335C1H470GA01D	Murata
L2	1	3.9nH ±0.1nH, 400mA, Thick Film Inductor (0201)	LQP03TN3N9B02	Murata
L3	1	4.7pF ±1pF, Ceramic Capacitor, 50V (0201)	GJM0335C1H4R7BB01	Murata
L5	1	5.1nH ±0.1nH, 350mA, Thick Film Inductor (0201)	LQP03TN5N1H02	Murata
L6	1	3nH ±0.1nH, 750mA, Wirewound Inductor(0402)	LQW15AN3N0B00	Murata
C1	1	2.2pF ±0.1pF, Ceramic Capacitor, 50V (0201)	GJM0335C1H2R2BB01	Murata

Reference Designator	Qty	Description	Manufacturer Part Number	Manufacturer
C3	1	2.0pF ±0.1pF, Ceramic Capacitor, 50V (0201)	GJM0335C1H2R0BB01	Murata
C7	1	5.1pF ±0.1pF, Ceramic Capacitor, 50V (0201)	GJM0335C1H5R1BB01	Murata
C8	1	3.0pF ±0.1pF, Ceramic Capacitor, 50V (0201)	GJM0335C1H3R0BB01	Murata
C9	1	39pF ±2%, Ceramic Capacitor, 25V (0201)	GRM0335C1H390GA01D	Murata
C10	1	1000pF ±5%, Ceramic Capacitor, 50V (0201)	GRM0335C1H102JE01	Murata
C11	1	100nF, Ceramic Capacitor, 25V (0201)	GRM033C81E104ME14	Murata
C5, C15, C16	3	100pF ±5%, Ceramic Capacitor, 50V (0201)	GRM0335C1H101JA01	Murata
C17	1	4.7µF ±10%, Ceramic Capacitor, 25V (0603)	GRM188C81E475KE11	Murata
C2, C4, C12, C14, C18, R5, R6, L4, L7, J8, J9	11	DNI	-	-
J1, J2, J3	3	Edge Launch SMA (0.375-inch pitch ground, tab), 50 Ohm	142-0701-851	Emerson Johnson
J10	1	Vertical Header Strip 2x5, Male, 100mil Pitch	-	Any Vendor
EVK	1	F147X EVB REVA	-	Axiro
Module	1	RA81F1475SEG	-	Axiro

6.3.3. 1750MHz to 2250MHz

Reference Designator	Qty	Description	Manufacturer Part Number	Manufacturer
R2, R3, R4, R8, C13, C6	6	0 Ohm, RES SMD 1/20W JUMPER (0201)	ERJ1GN0R00C	Panasonic
R1	1	18pF ±2%, Ceramic Capacitor,25V (0201)	GJM0335C1E180GB01	Murata
R7	1	1kOhm, ±1%, 0.05W, Chip Resistor (0201)	ERJ1GNF1001C	Panasonic
L1	1	33pF ±2%, Ceramic Capacitor,25V (0201)	GJM0335C1E330GB01	Murata
L2	1	5.6nH ±3%, 350mA, Thick Film Inductor (0201)	LQP03TN5N6H02	Murata
L3	1	2.0pF ±0.1pF, Ceramic Capacitor, 50V (0201)	GJM0335C1H2R0BB01	Murata
L5	1	4.7nH ±3%, 350mA, Thick Film Inductor (0201)	LQP03TN4N7H02	Murata
L6	1	3nH ±0.1nH, 750mA, Wirewound Inductor(0402)	LQW15AN3N0B00	Murata
C1	1	3 Ohm ±1%, 0.05W, Chip Resistor (0201)	CRCW02013R00FXED	Vishay Dale
C3	1	1.5pF ±0.1pF, Ceramic Capacitor, 50V (0201)	GJM0335C1H1R5BB01	Murata
C7	1	3.6pF ±0.1pF, Ceramic Capacitor, 50V (0201)	GJM0335C1H3R6BB01	Murata

Reference Designator	Qty	Description	Manufacturer Part Number	Manufacturer
C8	1	2.1pF ±0.1pF, Ceramic Capacitor, 50V (0201)	GJM0335C1H2R1BB01	Murata
C9	1	24pF ±2%, Ceramic Capacitor, 25V (0201)	GJM0335C1E240GB01	Murata
C10	1	1000pF ±5%, Ceramic Capacitor, 50V (0201)	GRM0335C1H102JE01	Murata
C11	1	100nF, Ceramic Capacitor, 25V (0201)	GRM033C81E104ME14	Murata
C5, C15, C16	3	100pF ±5%, Ceramic Capacitor, 50V (0201)	GRM0335C1H101JA01	Murata
C17	1	4.7µF ±10%, Ceramic Capacitor, 25V (0603)	GRM188C81E475KE11	Murata
C2, C4, C12, C14, C18, R5, R6, L4, L7, J8, J9	11	DNI	-	-
J1, J2, J3	3	Edge Launch SMA (0.375-inch pitch ground, tab), 50ohm	142-0701-851	Emerson Johnson
J10	1	Vertical Header Strip 2x5, Male, 100mil Pitch	-	Any Vendor
EVK	1	F147X EVB REVA	-	Axiro
Module	1	RA81F1475SEG	-	Axiro

6.3.4. 2300MHz to 2800MHz

Reference Designator	Qty	Description	Manufacturer Part Number	Manufacturer
R2, R3, R4, R8, C13, C6	6	0 Ohm, RES SMD 1/20W JUMPER (0201)	ERJ1GN0R00C	Panasonic
R1	1	24pF ±2%, Ceramic Capacitor,25V (0201)	GJM0335C1E240GB01	Murata
R7	1	1kOhm, ±1%, 0.05W, Chip Resistor (0201)	ERJ1GNF1001C	Panasonic
L1	1	4.3pF ±0.1pF, Ceramic Capacitor,50V (0201)	GJM0335C1H4R3BB01	Murata
L2	1	3.9nH ±0.1nH, 400mA, Thick Film Inductor (0201)	LQP03TN3N9B02	Murata
L3	1	1.6pF ±0.1pF, Ceramic Capacitor, 50V (0201)	GJM0335C1H1R6BB01	Murata
L5	1	1.9nH ±0.1nH, 600mA, Thick Film Inductor (0201)	LQP03TN1N9B02	Murata
L6	1	3nH ±0.1nH, 750mA, Wirewound Inductor(0402)	LQW15AN3N0B00	Murata
C1	1	3.6pF ±0.1pF, Ceramic Capacitor, 50V (0201)	GJM0335C1H3R6BB01	Murata
C3	1	1.2pF ±0.1pF, Ceramic Capacitor, 50V (0201)	GJM0335C1H1R2BB01	Murata
C7	1	4.3pF ±0.1pF, Ceramic Capacitor, 50V (0201)	GJM0335C1H4R3BB01	Murata
C8	1	2.2pF ±0.1pF, Ceramic Capacitor, 50V (0201)	GJM0335C1H2R2BB01	Murata
C9	1	5.1pF ±0.1pF, Ceramic Capacitor, 50V (0201)	GJM0335C1H5R1BB01	Murata

Reference Designator	Qty	Description	Manufacturer Part Number	Manufacturer
C10	1	1000pF ±5%, Ceramic Capacitor, 50V (0201)	GRM0335C1H102JE01	Murata
C11	1	100nF, Ceramic Capacitor, 25V (0201)	GRM033C81E104ME14	Murata
C5, C15, C16	3	100pF ±5%, Ceramic Capacitor, 50V (0201)	GRM0335C1H101JA01	Murata
C17	1	4.7µF ±10%, Ceramic Capacitor, 25V (0603)	GRM188C81E475KE11	Murata
C2, C4, C12, C14, C18, R5, R6, L4, L7, J8, J9	11	DNI	-	-
J1, J2, J3	3	Edge Launch SMA (0.375-inch pitch ground, tab), 50 Ohm	142-0701-851	Emerson Johnson
J10	1	Vertical Header Strip 2x5, Male, 100mil Pitch	-	Any Vendor
EVK	1	F147X EVB REVA	-	Axiro
Module	1	RA81F1475SEG	-	Axiro

7. Package Outline Drawings

The package outline drawings are accessible from the Axiro website. The package information is the most current data available and is subject to change without revision of this document.

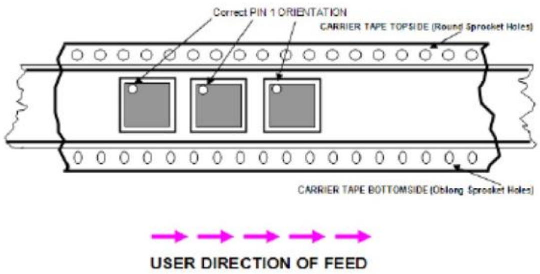
8. Marking Diagram

Top Marking Illustration	Marking	Representation
	RA81F1475SEG	Manufacturer Part Number
	$	Assembly Site Mark Code
	Y	Last Digit of the Year
	WW	Work Week
	***	Lot Sequential Code

9. Ordering Information

Part Number	Package	MSL Rating	Carrier Type	Temperature Range
RA81F1475SEGNK#BB0	4 × 4 mm 20-VFQFPN	MSL1	Tray	-40° to +115°C
RA81F1475SEGNK#HB0	4 × 4 mm 20-VFQFPN	MSL1	Tape and Reel	-40° to +115°C
RTKA81F14750P800RU	Evaluation Board 700MHz to 900MHz Tune			
RTKA81F14751P600RU	Evaluation Board 1350MHz to 1750MHz Tune			
RTKA81F14752P000RU	Evaluation Board 1750MHz to 2250MHz Tune			
RTKA81F14752P500RU	Evaluation Board 2300MHz to 2800MHz Tune			

Table 1. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
HB0	Quadrant 1 (EIA-481-C)	

10. Revision History

Revision	Date	Description of Change
2.00	Aug 4, 2026	Updated document branding and layout to Axiro Semiconductor standard. No changes to device functionality or specifications.