F1280

Dual VGA 0.001MHz to 1200MHz

The F1280 is a highly integrated 0.001MHz to 1200MHz dual VVA+VGA with integrated RMS detectors. The two independently controlled VVA+VGAs each provide 24dB of gain range with four different selectable gain ranges. The VGA gain ranges and switchable VGA2 inputs are controlled through an SPI interface with a 10MHz maximum clock operating frequency.

Competitive Advantage

- High level of integration

Applications

- Wireless infrastructure
- Medical devices
- General RF

Features

- 200Ω Differential inputs and 100Ω outputs
- Dual VVA+VGA with output RMS detectors
- SPI configurable VGA gain range
- 24dB gain range for each VVA
- Switchable dual inputs for VGA2
- Power-down feature
- Supply voltage: +4.75V to +5.25V
- Total supply current: 145mA
- 5 × 5 mm, 32-VFQFPN package
- -40°C to +105°C exposed pad operating temperature range

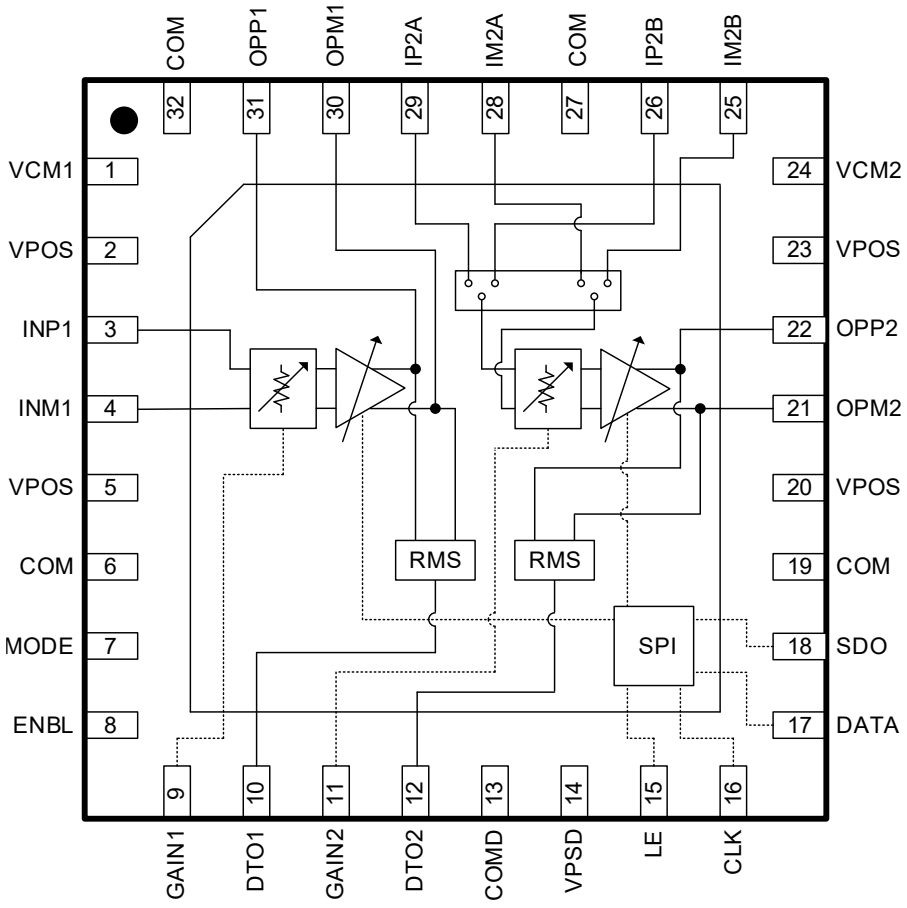

Figure 1. Block Diagram

Contents

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1. Pin Information

1.1 Pin Assignments

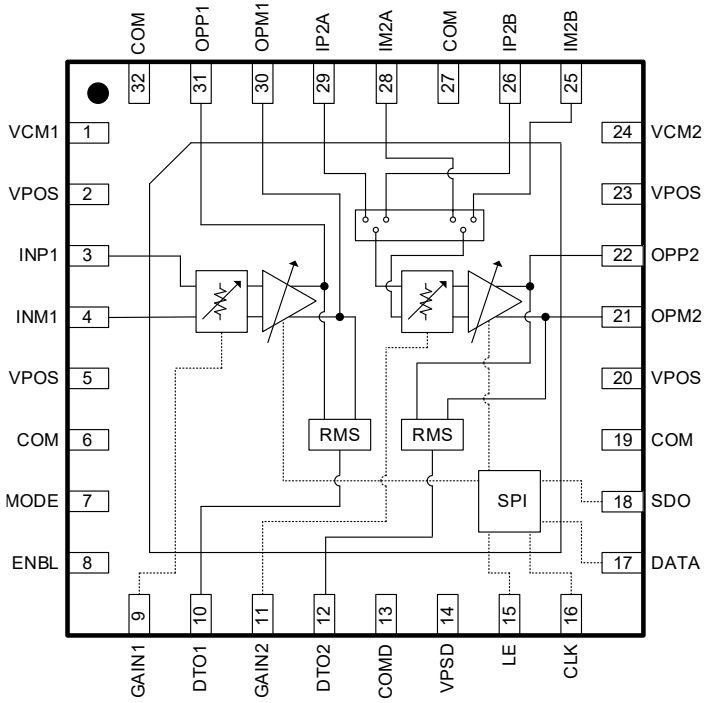


Figure 2. Pin Assignments – Top View

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 24	VCM1, VCM2	Common-Mode Voltages. Decouple to common for AC-coupled operation.
2, 5, 14, 20, 23	VPOS, VPSD	Analog and Digital Positive Supply voltage.
3, 4, 25, 26, 28, 29	INP1, INM1, IM2B, IP2B, IM2A, IP2A	Differential Inputs. 200Ω input impedance; AC coupling recommended.
6, 13, 19, 27, 32	COM, COMD	Analog and Digital Common. Connect via lowest possible impedance to external circuit common.
7	MODE	Gain Mode Control. Pull high for VGA mode with positive gain slope and pull low for AGC mode with negative gain slope.
8	ENBL	Chip Enable. Pull high to enable for normal operation and pull low to power down the device with minimal current consumption for power savings.
9, 11	GAIN1, GAIN2	VVA Analog Gain Control (0V to 1.1V).
10, 12	DTO1, DTO2	Detector outputs.
15, 17, 18	LE, DATA, SDO	SPI Programming and Data Readout pins.
16	CLK	SPI clock.
21, 22, 30, 31	OPM2, OPP2, OPM1, OPP1	Differential Outputs. 100Ω output impedance; AC coupling recommended.

-	EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

2. Specifications

2.1 Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Minimum	Maximum	Unit
VDD to GND (VPOS, VPSD)	V_{DD}	-0.3	+5.5	V
LE, CLK, DATA, SDO	V_{SPI}	-0.3	VPOS + 0.5	V
ENBL, MODE	V_{CTRL1}	-0.3	VPOS + 0.5	V
INP1, INM1, IP2A, IM2A, IP2B, IM2B	V_{RF_IN}	-0.3	VPOS + 0.5	V
OPP1, OPM1, OPP2, OPM2	V_{RF_OUT}	-0.3	VPOS + 0.5	V
DTO1, DTO2, GAIN1, GAIN2	V_{ANALOG}	-0.3	VPOS/2 + 0.5	V
Maximum Input Voltage	V_{MAX}	-	8	Vp-p
Internal Power Dissipation	P_{DISS}	-	945	mW
Junction Temperature	T_{JMAX}	-	+150	°C
Storage Temperature Range	T_{ST}	-65	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}	-	+260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}	-	1000 (Class 1C)	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)	V_{ESDCDM}	-	500 (Class C2)	V

2.2 Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
VDD to GND (VPOS, VPSD)	V_{DD}	-	4.75	5.0	5.25	V
Operating Temperature Range	T_{EP}	Exposed Paddle	-40	-	+105	°C
RF Frequency Range	f_{RF}	3dB bandwidth	0.001	-	1200	MHz
		1dB bandwidth	0.001	-	600	MHz

1. T_{EP} = Temperature of the exposed paddle.

2.3 Electrical Specifications – General

See the F1280 Evaluation Board/ Applications Circuit. Specifications apply when operated with V_{DD} = +5.0V, T_{EP} = +25°C, Z_S = 200Ω, Z_{LVGA1} = Z_{LVGA2} = 100Ω, RF_{IN} = -20dBm, f_{RF} = 140MHz, maximum gain settings, Evaluation Board trace and connector losses are de-embedded unless otherwise noted. 1:4 balun voltage gain is not included. All dBm numbers are with respect to each VGA's load impedance.

Parameter	Symbol	Condition	Minimum[1]	Typical	Maximum	Unit
Digital Logic	-	-	-	-	-	-
Input High Voltage	V_{IH}	VMODE, ENBL pins	***2***	-	***V_{DD}***	V
Input Low Voltage	V_{IL}	VMODE, ENBL pins	***-0.3***	-	***0.8***	V
Input Current	I_{IL}, I_{IH}	VMODE, ENBL pins	***-100***	-	***100***	µA
SPI Input High Voltage	V_{IH_SPI}	LE, CLK, DATA pins	***2***	-	***V_{DD}***	V
SPI Input Low Voltage	V_{IL_SPI}	LE, CLK, DATA pins	***-0.3***	-	***0.8***	V
SPI Output High Voltage	V_{OH_SPI}	SDO pin	***2.4***	-	-	V
SPI Output Low Voltage	V_{OL_SPI}	SDO pin	-	-	***0.4***	V
SPI Input Current	I_{IL}, I_{IH}	LE, CLK, DATA, SDO pins	***-100***	-	***100***	µA
SPI Input Capacitance	C_{IN}	LE, CLK, DATA, SDO pins	-	-	2	pF
Power and Enable	**-**	**VPOS, VPSD, COM, COMD, ENBL**	-	-	**-**	**-**
Total Supply Current	I_{DD}	ENBL = 5V, VMODE = 0V	-	145	***180***	mA
Total Supply Current	I_{DD}	ENBL = 5V, VMODE = 5V	-	120	***145***	mA
Disable Current	I_{DIS}	ENBL = 0V	-	10	-	mA
Enable Response Time	T_{EN}	50% VCTRL low-to-high transition until device meets full specifications in VGA mode.	-	1	-	ms
Disable Response Time	T_{DIS}	50% VCTRL high-to-low transition until device produces full attenuation in VGA mode.	-	500	-	ns
SPI Timing	**-**	**LE, CLK, DATA SDO**	-	-	**-**	
CLK frequency	f_{CLK}	-	-	-	10	MHz
DATA hold time	t_{DH}	-	5	-	-	ns
DATA setup time	t_{DS}	-	5	-	-	ns
LE hold time	t_{LH}	-	5	-	-	ns
LE setup time	t_{LS}	-	5	-	-	ns
CLK high pulse width	t_{PW}	-	5	-	-	ns
CLK-to-SDO delay	t_D	-	5	-	-	ns

Parameter	Symbol	Condition	Minimum[1]	Typical	Maximum	Unit
RMS Detectors	-	**DTO1, DTO2**	-	-	**-**	**-**
Frequency Range	DTO_{FRQ}	-	50	-	700	MHz
Output Setpoint	DTO_{SET}	SPI controlled, 3dB steps	-24	-	-3	dBV
Output Range	DTO_{RNG}	-	0	-	VDD	V
AGC Step Response Range	DTO_{STP}	5dB input step, C_{AGC} = 0.1µF	**-**	1	**-**	ms
Capacitor range for AGC. Modulation dependent.	DET_{CAP}	-	0.05	0.1	1	µF

1. Items in min/max columns in ***bold italics*** are confirmed by test. Items in min/max columns NOT in bold italics are confirmed by design characterization.

2.4 Electrical Specifications – RF Performance

See the F1280 Evaluation Board/ Applications Circuit. Specifications apply when operated with V_{DD} = +5.0V, T_{EP} = +25°C, Z_S = 200Ω, Z_{LVGA1} = Z_{LVGA2} = 100Ω, RF_{IN} = -20dBm, f_{RF} = 140MHz, maximum gain settings, Evaluation Board trace and connector losses are de-embedded unless otherwise noted. 1:4 balun voltage gain is not included. All dBm numbers are with respect to each VGA's load impedance. AGC DTO output RC filter values are R = 1kΩ and C = 3.3µF.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Maximum Input	VIN_{DIFF}	INP1/INM1, IP2A/IM2A, IP2B/IM2B differential	-	8	-	Vp-p
Maximum Output	$VOUT_{DIFF}$	OPP1/OPM1 differential at P1dB (VGA1 output)	-	3	-	Vp-p
		OPP2/OPM2 differential at P1dB (VGA2 output)	-	4.6	-	
AC Input Impedance	Z_{AC_IN}	Differential across INP1, INM1	-	200	-	Ω
		Selected Input Differential across IP2A, IM2A or IP2B, IM2B	-	200	-	Ω
		Unselected Input Differential across IP2A, IM2A or IP2B, IM2B	-	10	-	kΩ
AC Output Impedance	Z_{AC_OUT}	Differential across OPP1, OPM1, or OPP2, OPM2	-	100	-	Ω
Gain Control Interface	-	**Gain, Mode**	-	-	-	-
VVA + VGA Voltage Gain Range GAIN from 0V to 1.1V	G_{RANGE}	Gain Code 00	-12	-	12	dB
		Gain Code 01	-9.5	-	14.5	
		Gain Code 10	-7.5	-	16.5	
		Gain Code 11	-5.5	-	18.5	

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
VVA Gain Step Response Time	G_{STEP}	8.5dB Gain Step. Time to reach 0.1dB of final RF value.	-	20	50	µs
		24dB Gain Step. Time to reach 0.1dB of final RF value.	-	20	50	
VVA Gain Slope	G_{SLOPE}	MODE = V_{DD}	-	31	-	mV/dB
VVA Gain Error	G_{ERR}	From the mid-point of the linear region ±0.3V	-	±0.5	-	dB
Input Impedance	Z_{IN}	V_{GAINx} to COM	-	6	-	MΩ
f_{RF} = 140MHz						
VVA1 + VGA1 Noise Figure	NF_{1A}	Gain Code 00, V_{GAIN} = 1.1V	-	6.6	-	dB
		Gain Code 11, V_{GAIN} = 1.1V	-	5.4	-	
SW + VVA2 + VGA2 Noise Figure	NF_{2A}	Gain Code 00, V_{GAIN} = 1.1V	-	7.2	-	dB
		Gain Code 11, V_{GAIN} = 1.1V	-	5.6	-	
VGA1 Output IP3 Output Voltage Level of 1.0Vp-p	$OIP3_{1A}$	Gain Code 00, V_{GAIN} = 1.1V	13.5 (23.5)	15 (25)	-	dBV (dBm)
		Gain Code 11, V_{GAIN} = 1.1V	16 (26)	18 (28)	-	
VGA1 Output P1dB [2]	$OP1dB_{1A}$	Gain Code 00, V_{GAIN} = 1.1V	-1 (9.5)	2 (12)	-	dBV (dBm)
		Gain Code 11, V_{GAIN} = 1.1V	-1 (9.5)	2 (12)	-	
VGA2 Output IP3 Output Voltage Level of 1.0Vp-p	$OIP3_{2A}$	Gain Code 00, V_{GAIN} = 1.1V	18 (28)	24 (34)	-	dBV (dBm)
		Gain Code 11, V_{GAIN} = 1.1V	18 (28)	25 (35)	-	
VGA2 Output P1dB [2]	$OP1dB_{2A}$	Gain Code 00, V_{GAIN} = 1.1V	0 (10)	3.5 (13.5)	-	dBV (dBm)
		Gain Code 11, V_{GAIN} = 1.1V	0 (10)	4.5 (14.5)	-	
f_{RF} = 300MHz						
VVA1 + VGA1 Noise Figure	NF_{1B}	Gain Code 00, V_{GAIN} = 1.1V	-	7.2	-	dB
		Gain Code 11, V_{GAIN} = 1.1V	-	6	-	
SW + VVA2 + VGA2 Noise Figure	NF_{2B}	Gain Code 00, V_{GAIN} = 1.1V	-	7.5	-	dB
		Gain Code 11, V_{GAIN} = 1.1V	-	6	-	
VGA1 Output IP3 Output Voltage Level of 1.0Vp-p	$OIP3_{1B}$	Gain Code 00, V_{GAIN} = 1.1V	13 (23)	14.5 (24.5)	-	dBV (dBm)
		Gain Code 11, V_{GAIN} = 1.1V	13.5 (23.5)	15 (25)	-	
VGA1 Output P1dB [2]	$OP1dB_{1B}$	Gain Code 00, V_{GAIN} = 1.1V	-2.5 (7.5)	-1 (9)	-	dBV (dBm)
		Gain Code 11, V_{GAIN} = 1.1V	-2.5 (7.5)	0 (10)	-	
VGA2 Output IP3 Output Voltage Level of 1.0Vp-p	$OIP3_{2B}$	Gain Code 00, V_{GAIN} = 1.1V	17 (27)	22 (32)	-	dBV (dBm)
		Gain Code 11, V_{GAIN} = 1.1V	17 (27)	21 (31)	-	

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
VGA2 Output P1dB [2]	$OP1dB_{2B}$	Gain Code 00, V_{GAIN} = 1.1V	-1 (9)	3 (13)	-	dBV (dBm)
		Gain Code 11, V_{GAIN} = 1.1V	-1 (9)	3 (13)	-	
f_{RF} = 700MHz						
VVA1 + VGA1 Noise Figure	NF_{1C}	Gain Code 00, V_{GAIN} = 1.1V	-	8.1	-	dB
		Gain Code 11, V_{GAIN} = 1.1V	-	7.1	-	
SW + VVA2 + VGA2 Noise Figure	NF_{2C}	Gain Code 00, V_{GAIN} = 1.1V	-	9.1	-	dB
		Gain Code 11, V_{GAIN} = 1.1V	-	7.6	-	
VGA1 Output IP3 Output Voltage Level of 1.0Vp-p	$OIP3_{1C}$	Gain Code 00, V_{GAIN} = 1.1V	-	4 (14)	-	dBV (dBm)
		Gain Code 11, V_{GAIN} = 1.1V	-	6 (16)	-	
VGA1 Output P1dB [2]	$OP1dB_{1C}$	Gain Code 00, V_{GAIN} = 1.1V	-	-6 (4)	-	dBV (dBm)
		Gain Code 11, V_{GAIN} = 1.1V	-	-5 (5)	-	
VGA2 Output IP3 Output Voltage Level of 1.0Vp-p	$OIP3_{2C}$	Gain Code 00, V_{GAIN} = 1.1V	-	16 (26)	-	dBV (dBm)
		Gain Code 11, V_{GAIN} = 1.1V	-	17 (27)	-	
VGA2 Output P1dB [2]	$OP1dB_{2C}$	Gain Code 00, V_{GAIN} = 1.1V	-	1 (11)	-	dBV (dBm)
		Gain Code 11, V_{GAIN} = 1.1V	-	2 (12)	-	

1. Items in min/max columns in ***bold italics*** are confirmed by test. Items in min/ max columns NOT in bold italics are confirmed by design characterization.
2. The 1dB compression point is a linearity figure of merit. For the maximum RF operating input power levels, see Absolute Maximum Ratings.

2.5 Thermal Characteristics

Parameter	Symbol	Value	Unit
Junction to Ambient Thermal Resistance	θ_{JA}	32.8	°C/W
Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	θ_{JC_BOT}	7.2	°C/W
Moisture Sensitivity Rating (Per J-STD-020)	-	1	-

3. Typical Operating Conditions

Unless otherwise noted:

- V_{DD} = +5.0V
- T_{EP} = +25°C
- Z_S = 200Ω
- Z_{LVGA1} = 100Ω
- Z_{LVGA2} = 100Ω
- Small signal parameters measured with RF_{IN} = -20dBm
- Maximum gain settings for both VVAs and VGAs
- All temperatures are referenced to the exposed paddle
- Evaluation Board traces and connector losses are de-embedded

4. Typical Performance Graphs

V_{DD} = 5V, T_A = 25°C, Z_S = 200Ω, Z_L VGA1 = 100Ω, Z_L VGA2 = 100Ω, RF input = −20dBm at 140MHz, unless otherwise noted. Gain code = 11, VGAIN = 1.1V, setpoint code = 000, MODE = 5V (VGA mode) for both amplifiers, unless otherwise noted.

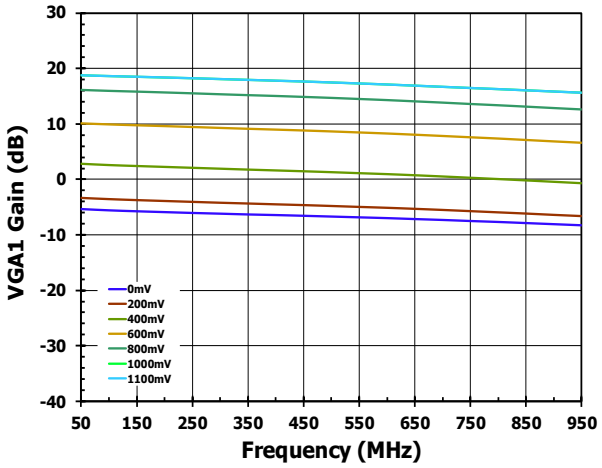


Figure 3. Gain vs. Frequency over V_{GAIN} at Gain Code 11 for VGA1

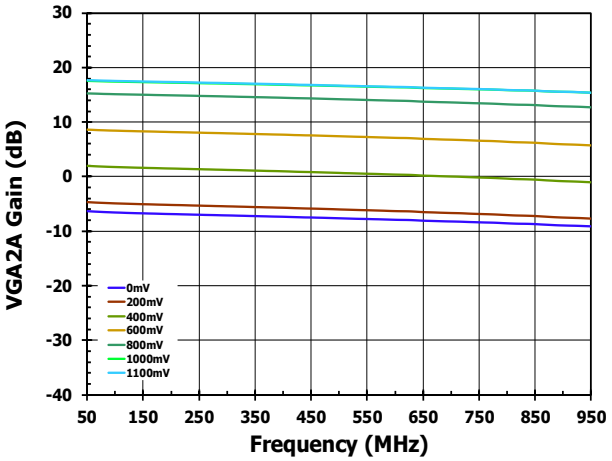


Figure 4. Gain vs. Frequency over V_{GAIN} at Gain Code 11 for VGA2

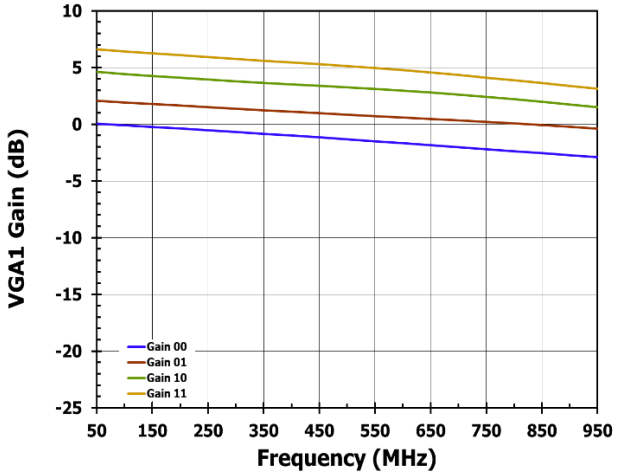


Figure 5. Gain vs. Frequency over Gain Code at V_{GAIN} = 0.5V for VGA1

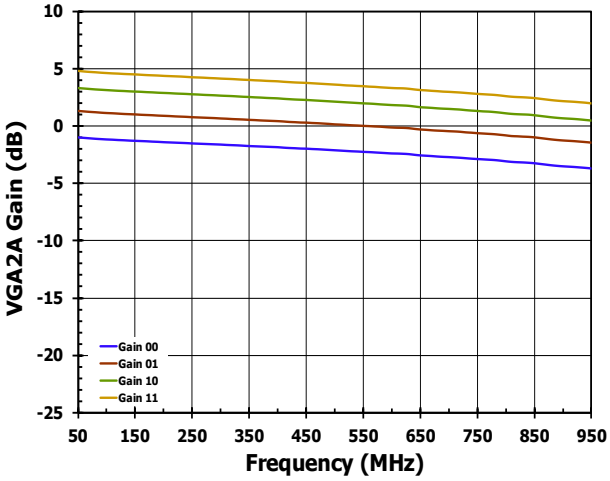


Figure 6. Gain vs. Frequency over Gain Code at V_{GAIN} = 0.5V for VGA2

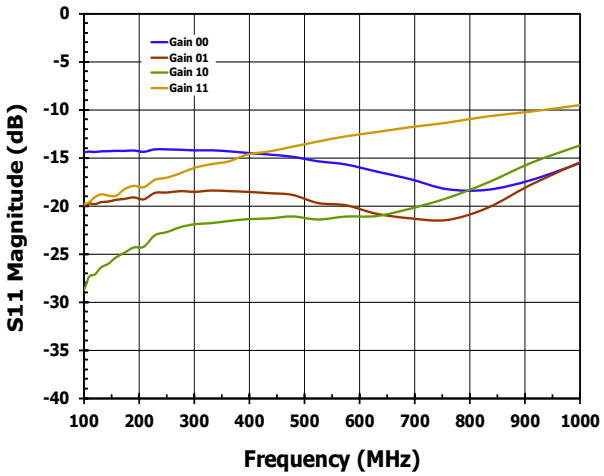


Figure 7. S11 (re: 200Ω) Magnitude over Frequency for VGA1

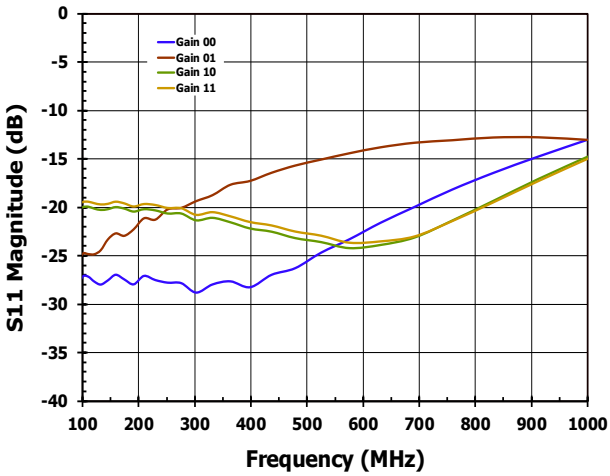


Figure 8. S11 (re: 200Ω) Magnitude over Frequency for VGA2

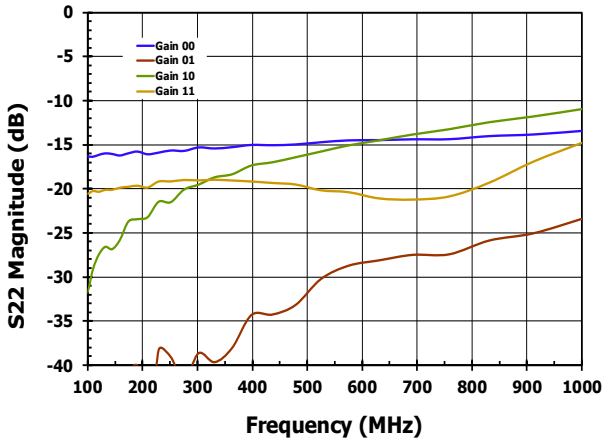


Figure 9. S22 (re: 100Ω) Magnitude over Frequency for VGA1

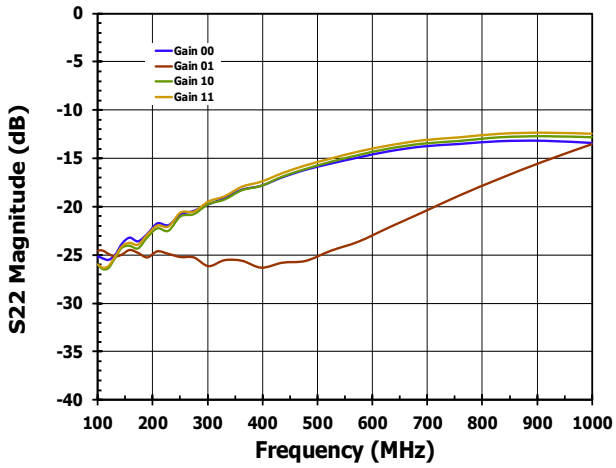


Figure 10. S22 (re: 100Ω) Magnitude over Frequency for VGA2

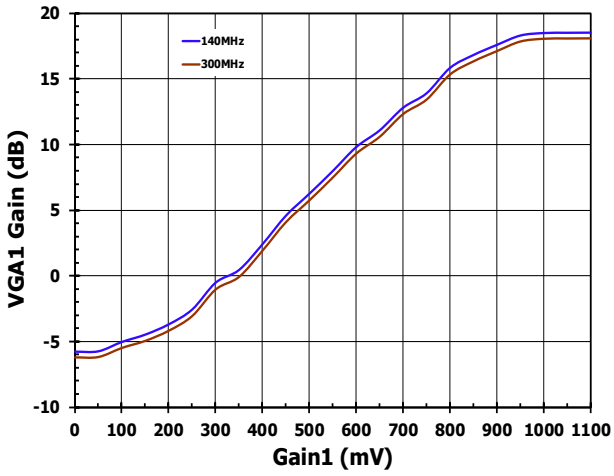


Figure 11. Gain vs. V_{GAIN} over Frequency at Gain Code 11 for VGA1

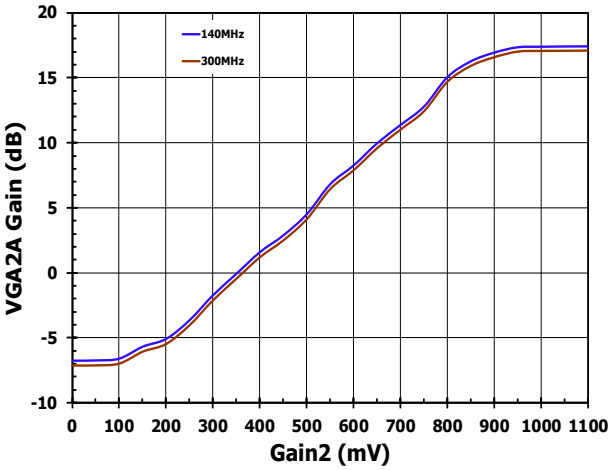


Figure 12. Gain vs. V_{GAIN} over Frequency at Gain Code 11 for VGA2

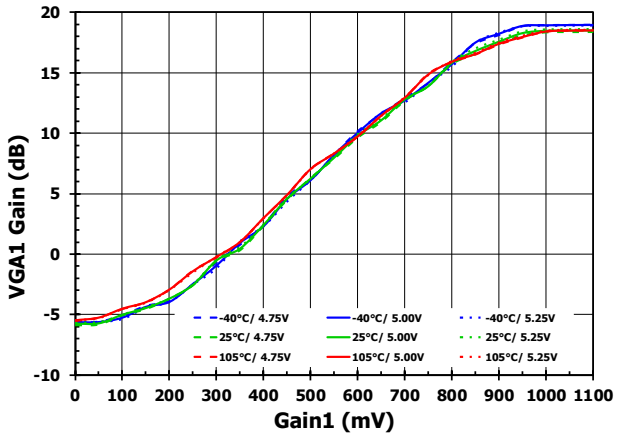


Figure 13. Gain Conformance over Temperature for VGA1

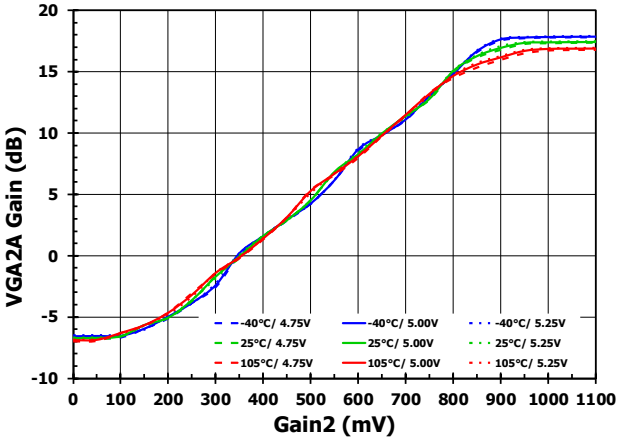


Figure 14. Gain Conformance over Temperature for VGA2

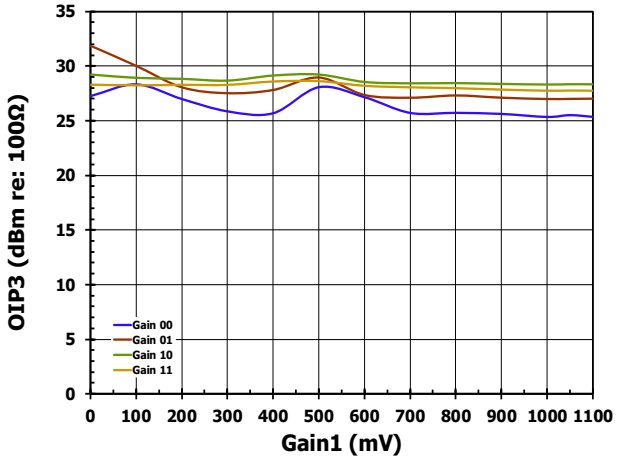


Figure 15. OIP3 vs. V_{GAIN} over Gain Code for VGA1

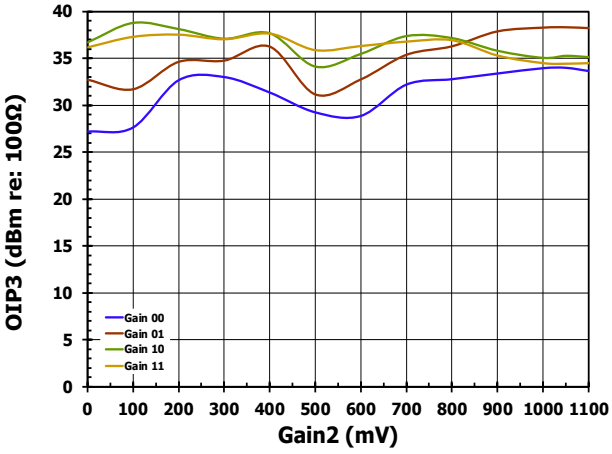


Figure 16. OIP3 vs. V_{GAIN} over Gain Code for VGA2

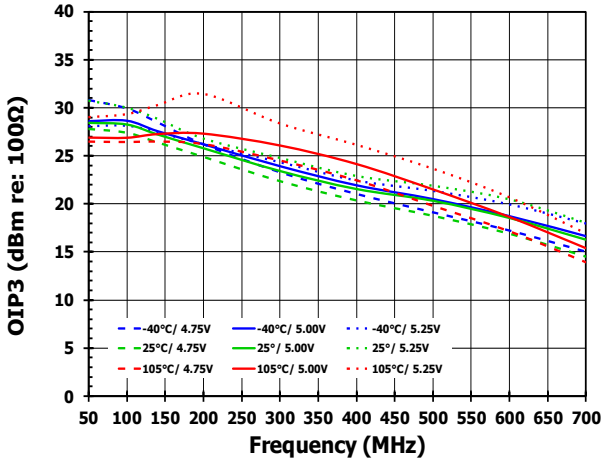


Figure 17. OIP3 vs. Frequency over Supply Voltage and Temperature for VGA1

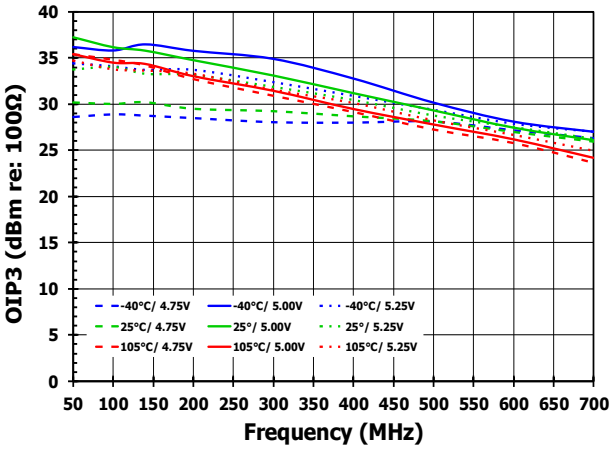


Figure 18. OIP3 vs. Frequency over Supply Voltage and Temperature for VGA2

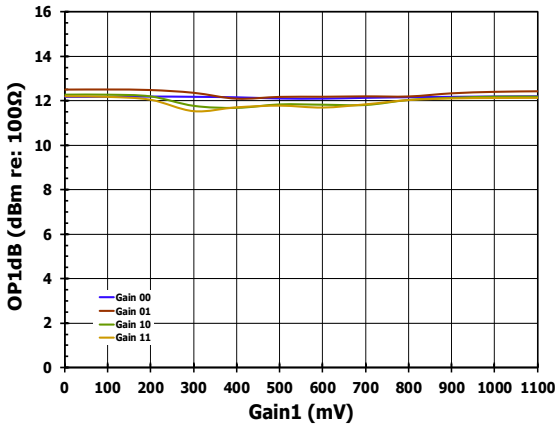


Figure 19. OP1dB vs. V_{GAIN} over Gain Code for VGA1

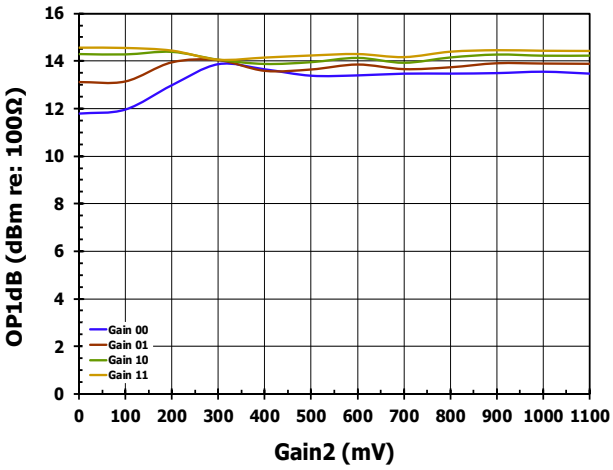


Figure 20. OP1dB vs. V_{GAIN} over Gain Code for VGA2

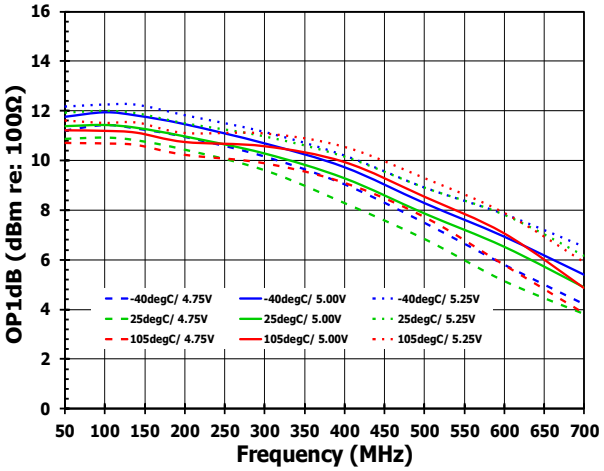


Figure 21. OP1dB vs. Frequency over Supply Voltage and Temperature for VGA1

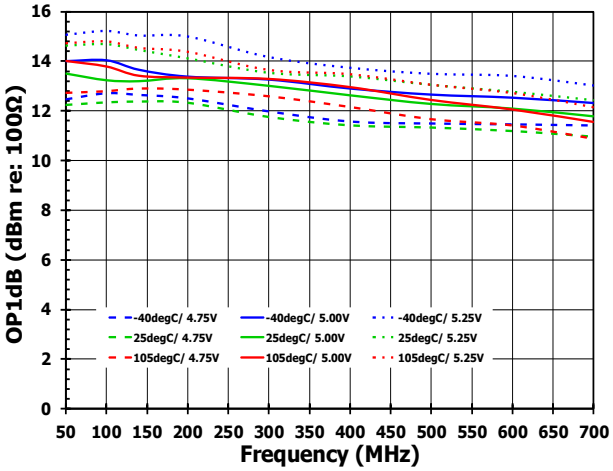


Figure 22. OP1dB vs. Frequency over Supply Voltage and Temperature for VGA2

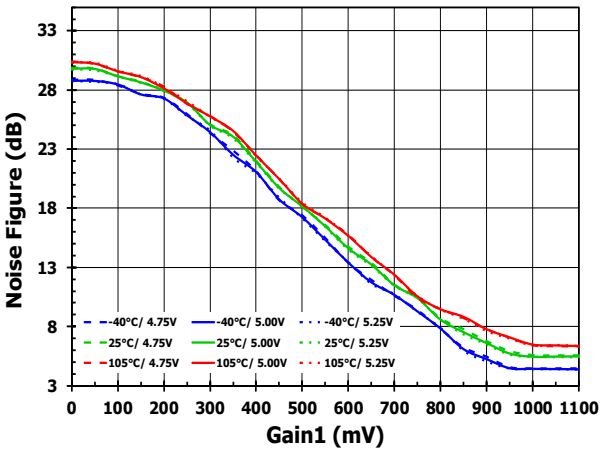


Figure 23. Noise Figure vs. V_{GAIN} over Supply Voltage and Temperature for VGA1

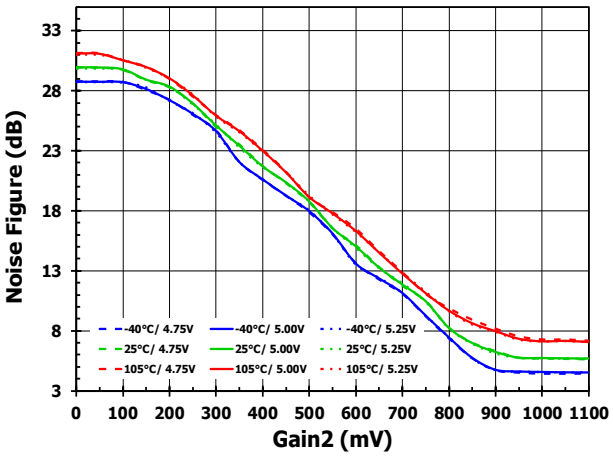


Figure 24. Noise Figure vs. V_{GAIN} over Supply Voltage and Temperature for VGA2

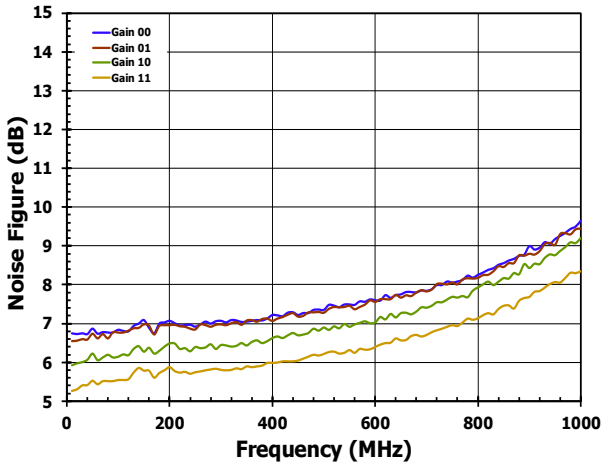


Figure 25. Noise Figure vs. Frequency over Maximum V_{GAIN} for VGA1

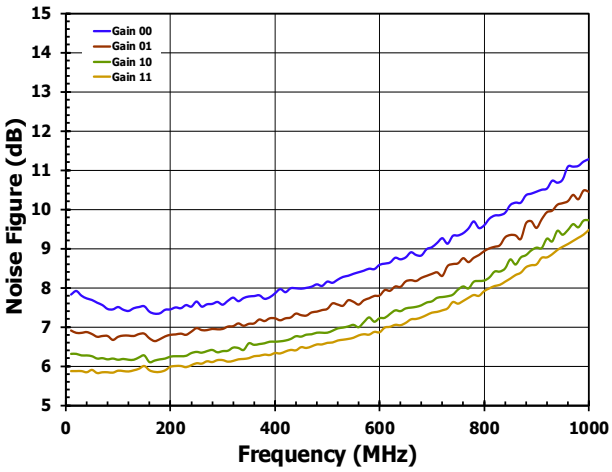


Figure 26. Noise Figure vs. Frequency over Maximum V_{GAIN} for VGA2

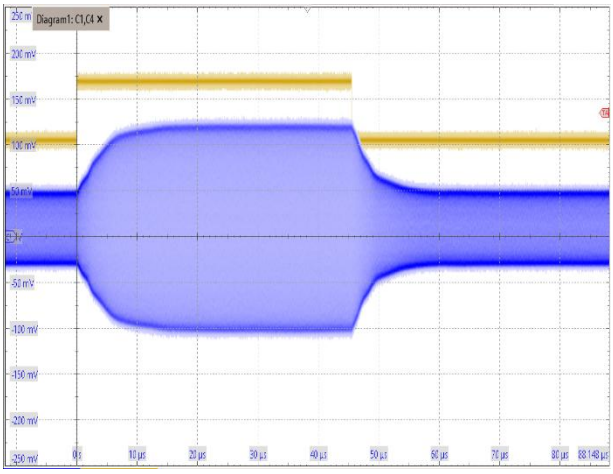


Figure 27. V_{GAIN} Step Response for VGA1

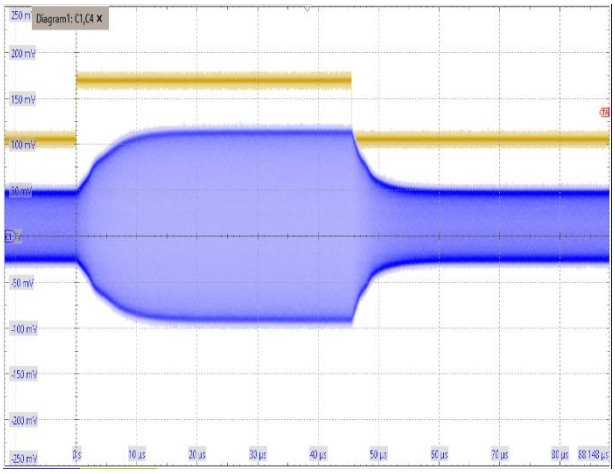


Figure 28. V_{GAIN} Step Response for VGA2

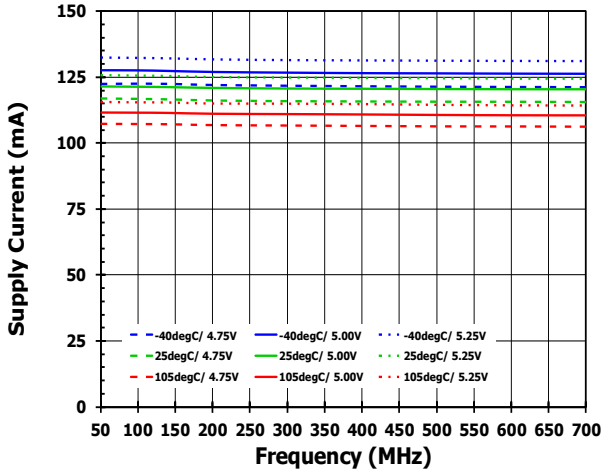


Figure 29. Supply Current over Temperature for VGA1

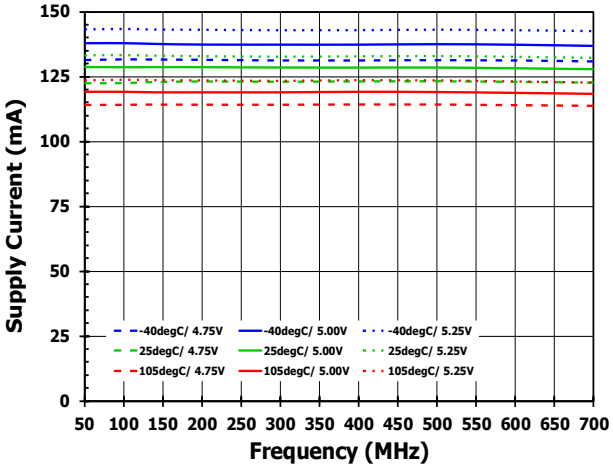


Figure 30. Supply Current over Temperature for VGA2

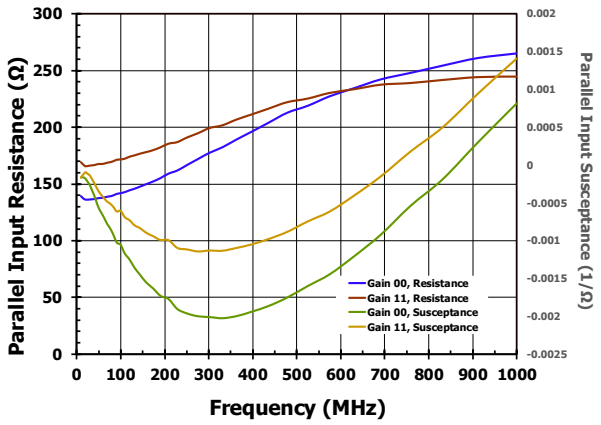


Figure 31. Parallel Input Resistance and Reactance vs. Frequency for VGA1

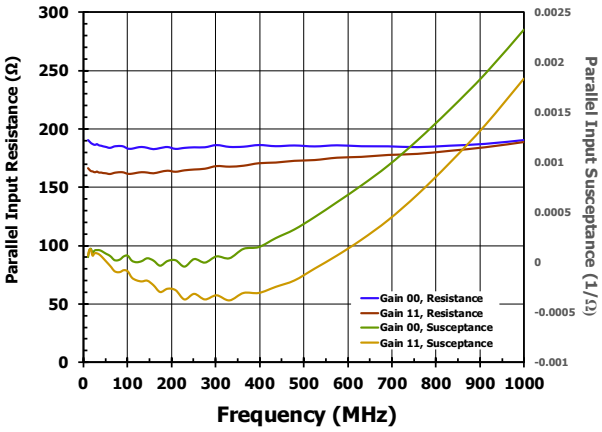


Figure 32. Parallel Input Resistance and Reactance vs. Frequency for VGA2

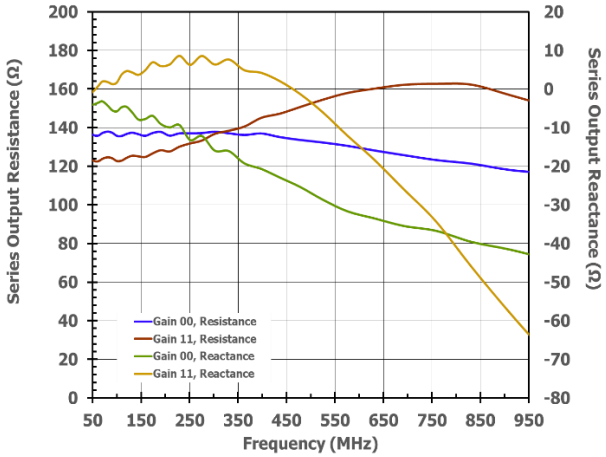


Figure 33. Series Output Resistance and Reactance vs. Frequency for VGA1

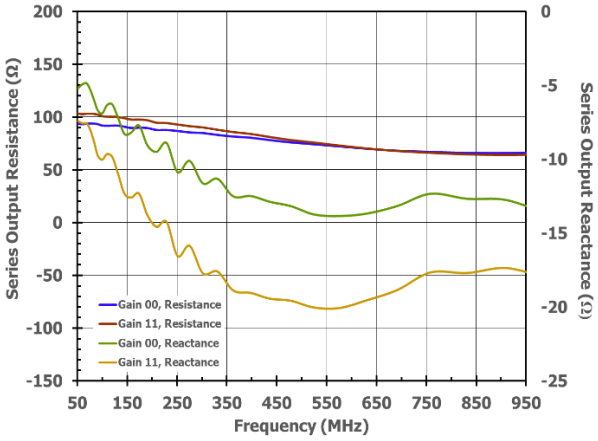


Figure 34. Series Output Resistance and Reactance vs. Frequency for VGA2

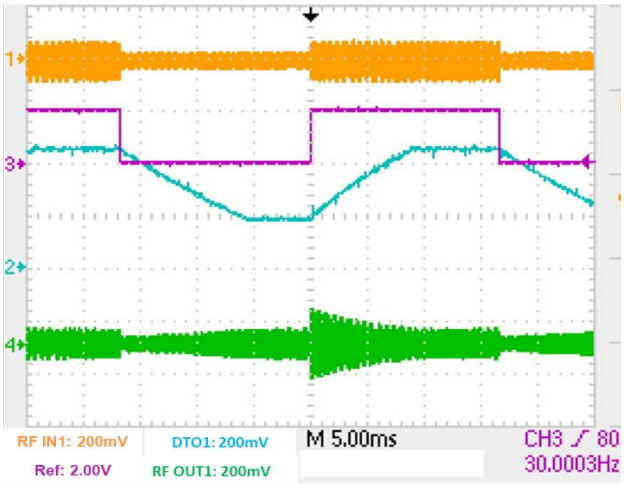


Figure 35. RSSI Step Response (AGC Mode) for VGA1

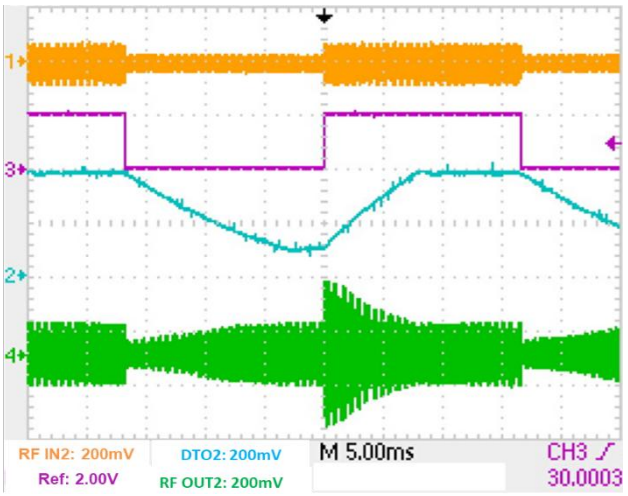


Figure 36. RSSI Step Response (AGC Mode) for VGA2

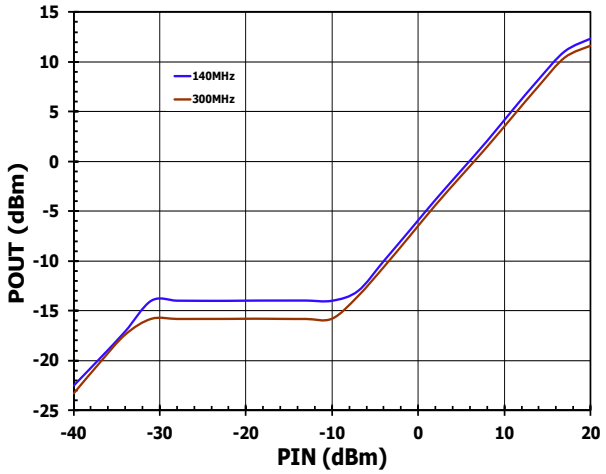


Figure 37. POUT vs. Input Power (PIN) over Frequency (AGC Mode, Set Point 000) for VGA1

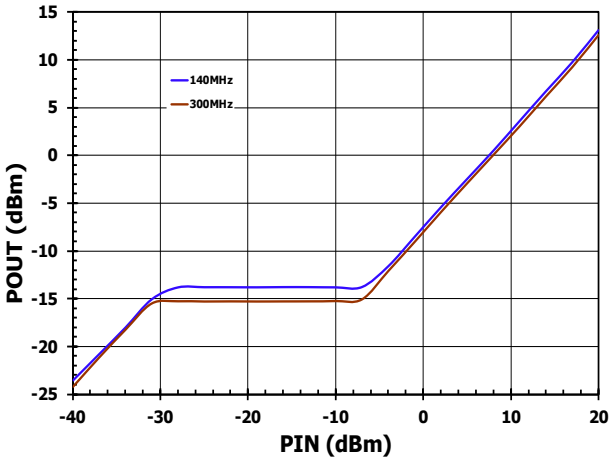


Figure 38. POUT vs. Input Power (PIN) over Frequency (AGC Mode, Set Point 000) for VGA2

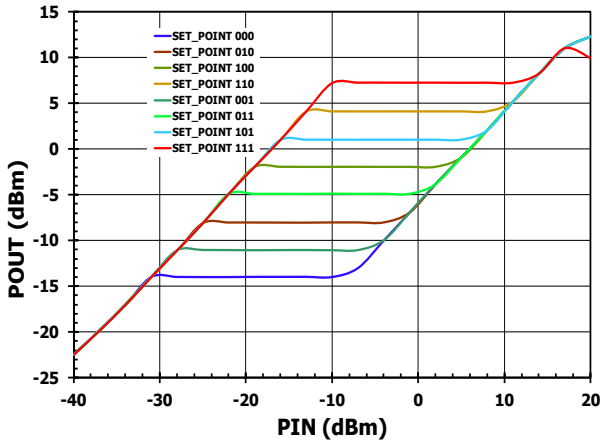


Figure 39. POUT vs. Input Power (PIN) over Setpoint (AGC Mode) for VGA1

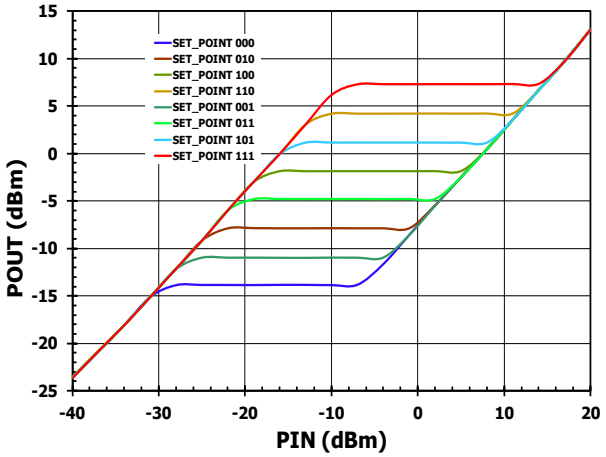


Figure 40. POUT vs. Input Power (PIN) over Setpoint (AGC Mode) for VGA2

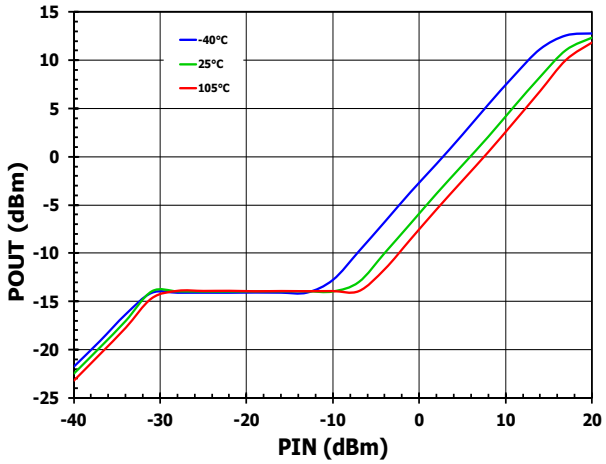


Figure 41. POUT vs. Input Power (PIN) over Temperature (AGC Mode, Set Point 000) for VGA1

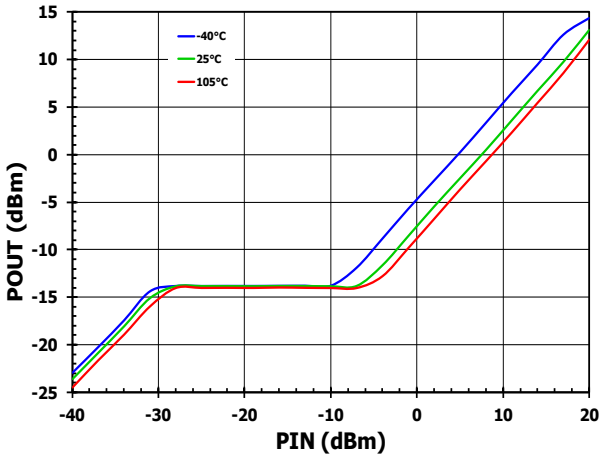


Figure 42. POUT vs. Input Power (PIN) over Temperature (AGC Mode, Set Point 000) for VGA2

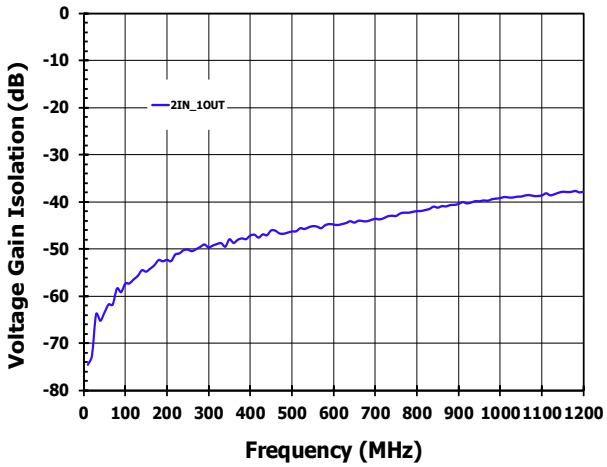


Figure 43. Amplifier Isolation vs. Frequency; VGA2 Differential Input A (IN2(a)) to VGA1 Differential Output (OUT1)

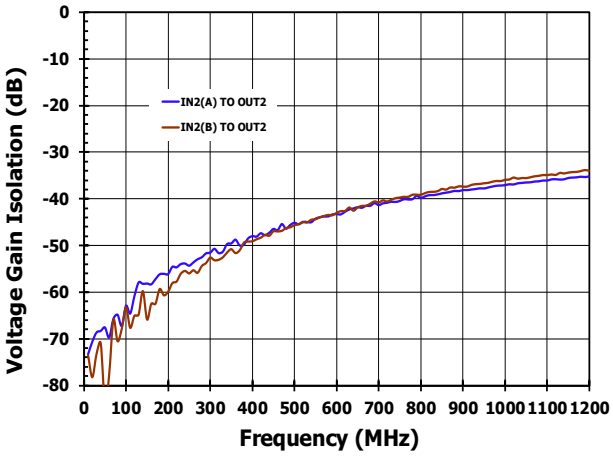


Figure 44. VGA2 Input Switch Isolation vs. Frequency; VGA2 Disabled Differential Input (IN2(a), IN2(b)) to VGA2 Differential Output (OUT2)

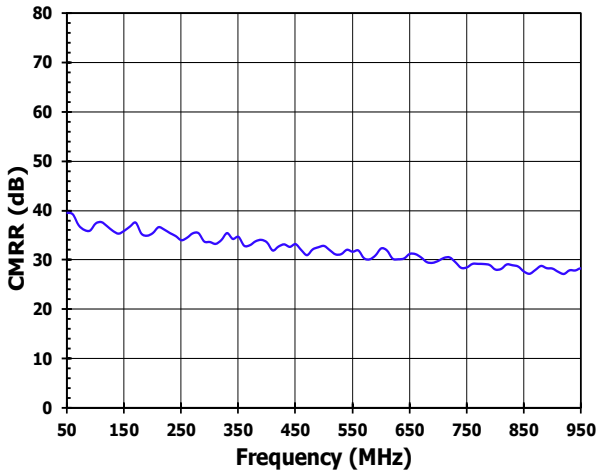


Figure 45. CMRR vs. Frequency for VGA1

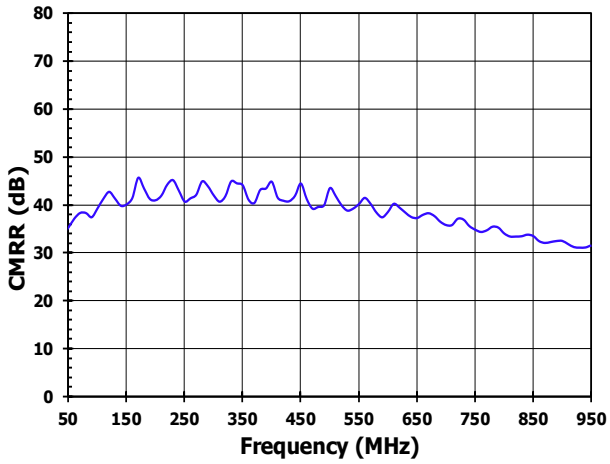


Figure 46. CMRR vs. Frequency for VGA2

5. Control Mode

5.1 Overview

The F1280 contains two pairs of Voltage Variable Attenuators (VVAs) and Variable Gain Amplifiers (VGAs) offering high gain performance and gain control up to 24dB per VVA+VGA pair, from low frequencies up to 1GHz. Each pair is individually programmable via SPI programming as shown in the following sections. VGA2 also has the capability of a switchable input programmable via the SPI. The VGAs can be cascaded to provide a total gain range of 48dB. The gain control interface can operate in either a gain-up or a gain-down mode. When the MODE pin is pulled high, the gain increases with increasing gain voltages. This is the VGA mode. With the MODE pin pulled low, the gain decreases with increasing gain voltages. This is the AGC mode.

The VGAs have independent RMS detectors for Automatic Gain Control. This is known as the AGC mode of the VGA and can be set using the Gain Mode Control pin (pin 7, MODE) of the F1280. When the MODE pin is pulled down to a logic low, the F1280 functions under the AGC mode. Each detector setpoint can be programmed individually using the SPI interface from -24dBV to -3dBV in 3dB steps.

The internally connected detectors are connected to the outputs of the VGAs through a programmable attenuator. The detector compares the output of the attenuator to an internal reference of 63mV rms. If the amplifier is operated in VGA mode or the detector is not used, the setpoint should be programmed to maximum attenuation so that the VGA output does not overdrive the input to the detector, adversely affecting both the detector and the VGA output.

5.2 Register Map

The device includes a single register that can be read and write. Below are the bit definitions for the single register.

MSB **LSB**

B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
VGA2_gain1	VGA2_gain0	VGA1_gain1	VGA1_gain0	VGA2_sw	AGC2_set2	AGC2_set1	AGC2_set0	AGC1_set2	AGC1_set1	AGC1_set0

5.3 Differential Output RMS Setpoint Map

Setpoint Word			RMS Output (mV rms/dBV)
AGC_set2	AGC_set1	AGC_set0	
0	0	0	+62.5 / -24
0	0	1	+88 / -21
0	1	0	+125 / -18
0	1	1	+176 / -15
1	0	0	+250 / -12
1	0	1	+353 / -9 [1]
1	1	0	+500 / -6
1	1	1	+707 / -3

1. For SETPOINT = 5 (101b), temperature variation is +1.5dB from 25°C to 105°C and -1.5dB from 25°C to -40°C with part to part variation at ±3dB.

5.4 VGA2 Input Switch Logic

VGA2_sw	Selected Input
0	IP2A, IM2A
1[1]	IP2B, IM2B

1. VGA1 is disabled when VGA2 switch is set to logic 1 (IP2B, IM2B selected input).

5.5 Maximum Gain Map

VGA_gain1	VGA_gain0	VGA1 Maximum Gain (dB)	VGA2 Maximum Gain (dB)
0	0	12	12
0	1	14.5	14.5
1	0	16.5	16.5

1	1	18.5	18.5

5.6 Timing Diagrams

5.6.1. Write Mode

The first data bit determines whether the device is writing to or reading from the internal register. For a write operation, the first bit should be a logic 1. The data word is then registered into the data pin on consecutive rising edges of the clock.

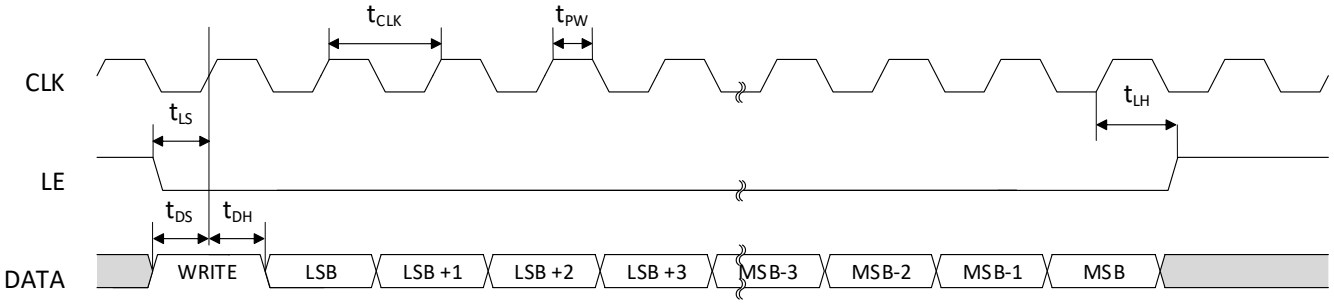


Figure 47. Write Mode Timing Diagram

5.6.2. Read Mode

The first data bit determines whether the device is writing to or reading from the internal register. For a read operation, the first bit should be a logic 0. The data word is then updated at the SDO pin on consecutive falling edges of the clock.

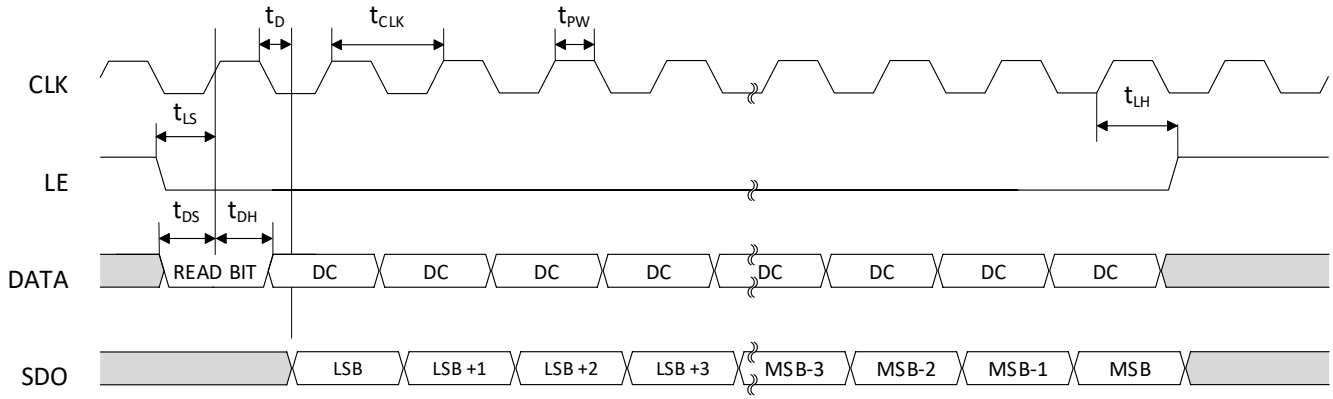


Figure 48. Read Mode Timing Diagram

6. Evaluation Board (EVB) Information

6.1 Evaluation Board Applications Circuit

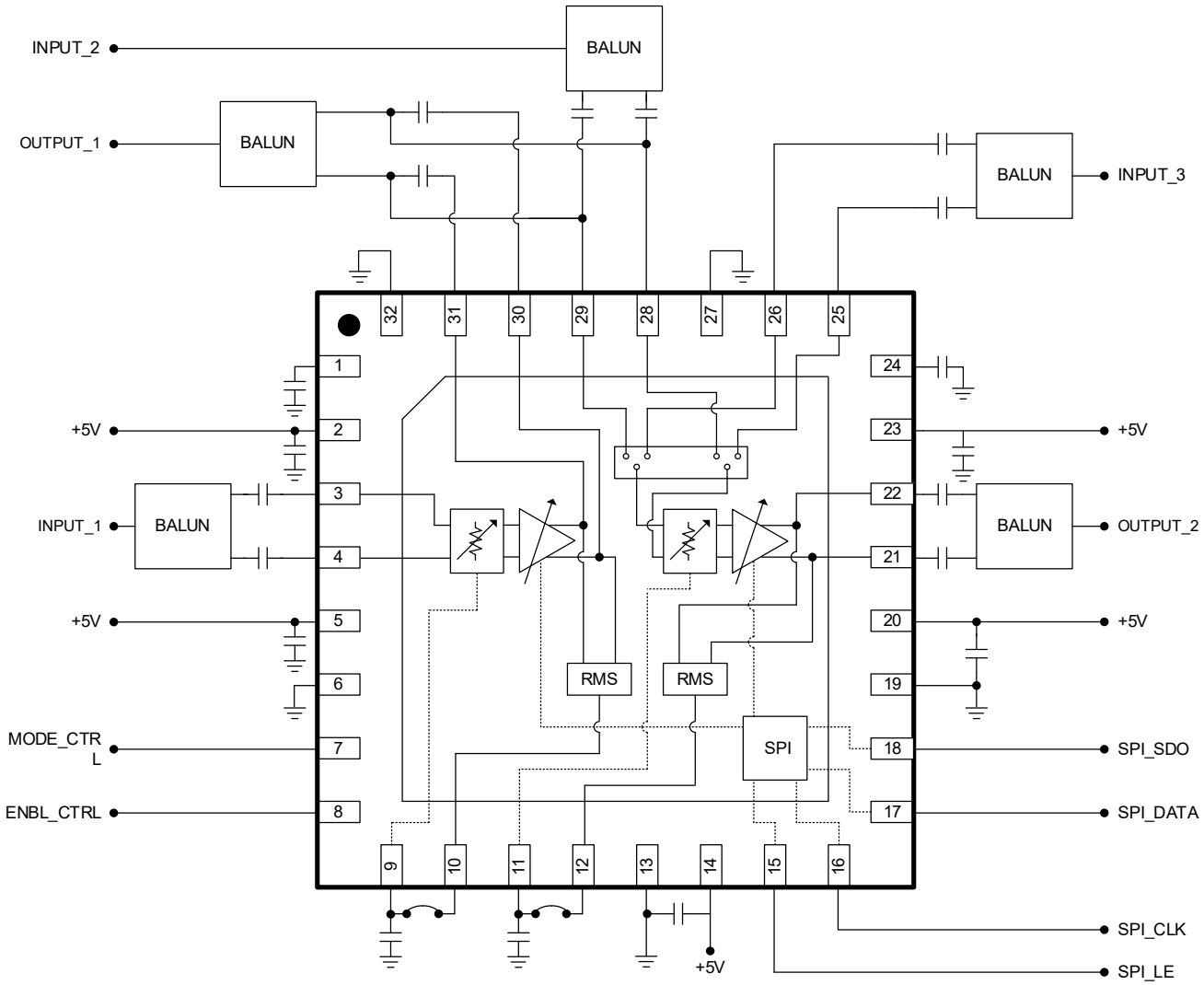


Figure 49. Evaluation Board Application Circuit

6.2 Evaluation Board Images

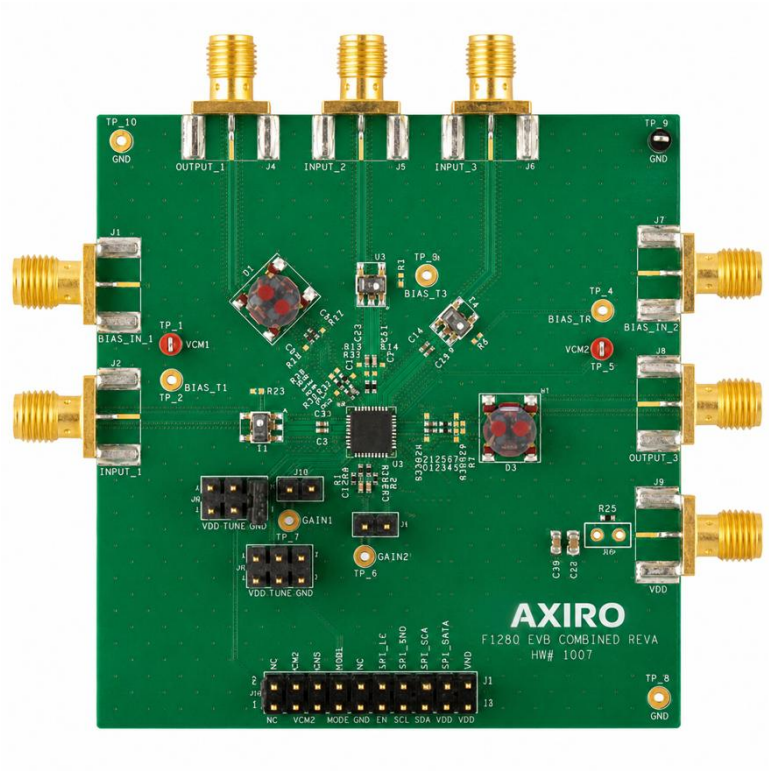


Figure 50. Evaluation Board – Top View

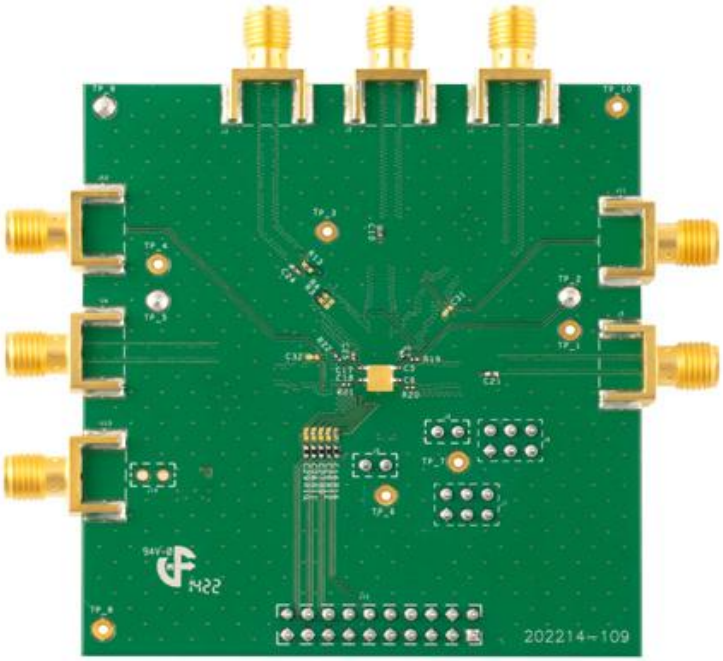


Figure 51. Evaluation Board – Bottom View

6.3 Evaluation Board Schematic

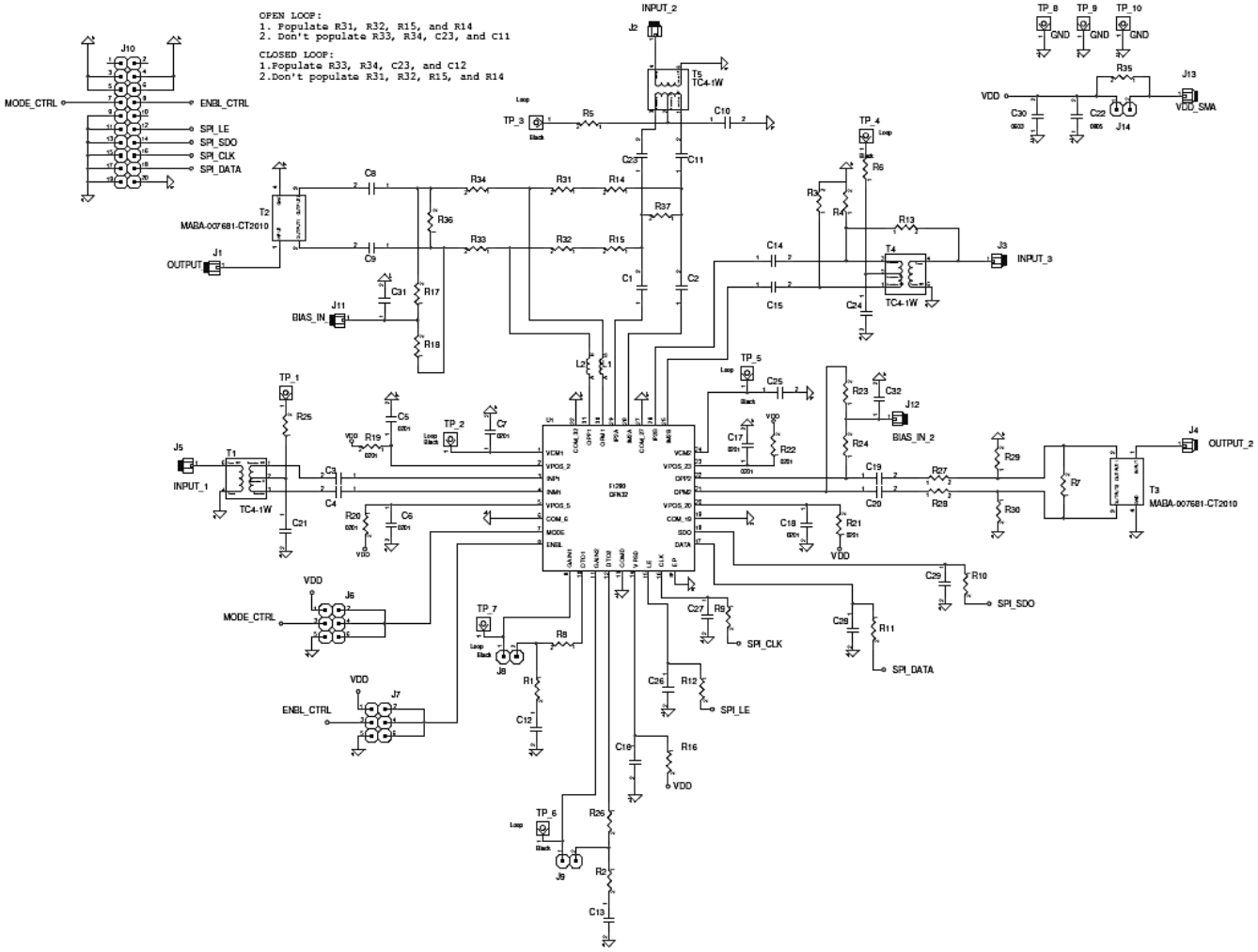


Figure 52. Evaluation Board Schematic

6.4 Evaluation Kit (EVK) Information

For instructions on how to use the EVB and graphical user interface software, see the *F1280 EVK Manual.*

6.5 Bill of Materials

Part Reference	Qty	Description	Manufacturer Part No.	Manufacturer
R1, R2, R9, R10, R11, R12, R16, R27, R28, R33, R34, R35	14	0Ω Resistors (0402)	ERJ-2GE0R00X	Panasonic
R19, R20, R21, R22	4	0Ω Resistors (0201)	ERJ1GE0R00C	Panasonic
R8, R26	2	1 kOhms ±1%, 0.1W, 1/10W Chip Resistor 0402	ERJ-2RKF1001X	Panasonic
C12, C13	2	3.3µF ±10% 16V Ceramic Capacitor X6S 0603	C1608X6S1C335K080AC	TDK
C22	1	10µF ±20%, 16V, X6S Ceramic Capacitor (0805)	GRM21BC81C106ME15L	Murata

Part Reference	Qty	Description	Manufacturer Part No.	Manufacturer
C30	1	1µF ±10%, 16V, X7R Ceramic Capacitor (0603)	GRM188R71C105K	Murata
C5, C6, C7, C17, C18, C25	6	0.1µF ±10%, 16V, X7R Ceramic Capacitor (0201)	GRM033C71C104ME14D	Murata
C3, C4, C8, C9, C10, C11, C14, C15, C16, C19, C20, C21, C23, C24	16	0.1µF ±10%, 16V, X7R Ceramic Capacitor (0402)	GRM155R71C104K	Murata
C26, C27, C28, C29, C31, C32, R3, R4, R5, R6, R7, R13, R14, R15, R17, R18, R23, R24, R25, R29, R30, R31, R32, R36, R37	25	DNI	-	-
C1, C2	2	0Ω Resistors (0402)	ERJ-2GE0R00X	Panasonic
L1, L2	2	0Ω Resistors (0402)	ERJ-2GE0R00X	Panasonic
TP_1, TP_2, TP_3, TP_4, TP_5, TP_6, TP_7, TP_8, TP_9, TP_10	10	Test Point (T2 and T5 red) (T9 Black)	RED = P/N 5000 / BLACK = 5001	-
T1, T4, T5	3	BALUN 5MHz-1.2GHz 1:2 4-SMD Module	MABA-007681-CT2010	MACOM Technology Solutions
T2, T3	2	RF Balun 3MHz ~ 800MHz 1:4 5-SMD Module	TC4-1W+	Minicircuits
J1, J2, J3, J4, J5, J11, J13	8	Edge Launch SMA (0.375inch pitch ground, tab) (50 Ohm)	142-0701-851	Emerson Johnson
J6, J7	2	CONN HEADER VERT DBL 3 X 2 POS GOLD	67997-106HLF	AMPHENOL FCI
J8, J9, J14	3	CONN HEADER VERT SGL 2 X 1 POS GOLD	961102-6404-AR	3M
J10	2	CONN HEADER VERT DBL 10 X 2 POS GOLD	67997-120HLF	Amphenol FCI
U1	1	RA81F1280ST	F1280	Axiro
EVB	1	Printed Circuit Board (Rev A)	F1280_EVB_COMBINED	Axiro

7. Applications Information

The F1280 is optimized for use in high-performance RF applications from 0.001MHz to 1000MHz.

7.1 Basic Connections

The basic connections for a typical F1280 application are shown in Figure 52.

7.2 Power Supplies

Bypass supply pins with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20µs. In addition, all control pins should remain at 0V (±0.3V) while the supply voltage ramps or while it returns to zero.

A nominal +5V V_{DD} supply voltage should be applied to the pins. The supply voltage is between the limits of 4.75V and 5.25V. The supply pins must be decoupled to ground with at least one low inductance, surface-mount ceramic capacitor of 0.1µF. Place these decoupling capacitors as close as possible to the F1280 DUT.

7.3 Signal Paths

The F1280 has three input signal paths. Each of the three pairs of input pins (INP1/INM1, IP2A/IM2A, and IP2B/IM2B) has a differential input impedance of 200Ω. Two of the inputs lead to VGA2 via a programmable input switch, and the third input is for VGA1. There is a balun provided on the evaluation board as seen on the application circuit shown in Figure 52.

The F1280 also has two output signal paths. One signal path per VGA with a differential output impedance of 100Ω. The output of VGA1 can be coupled to the input of VGA2, CH A in order be used in a cascaded manner. A 100Ω differential load can be presented to the output of VGA2 via a 1:2 balun.

7.4 RMS Detectors

The F1280 has a pair of RMS detectors. Each VGA output is applied to a detector. This can be seen on the block diagram shown in Figure 52. These on-board detectors are used when the device is programmed for the AGC mode of operation.

7.5 VGA and AGC Modes

For the VGA mode, when the MODE pin (pin 7) is pulled high, the RMS detectors are OFF. The AGC loop is open, the VGain pins 9 and 11 are disconnected from the DTO pins 10 and 12, respectively, and the VGain is controlled externally. Whereas, for the AGC mode, when the MODE pin is pulled low, the RMS detectors are ON. Pins 9 and 10 will need to be shorted; the same applies to pins 11 and 12 (these are the Gain and DTO pins as shown in the pin assignments diagram as well as in Figure 52). This closes the AGC loop and the AGC will now lock the VGA output to a specific setpoint which is configured using the SPI programming and set according to section 5.3.

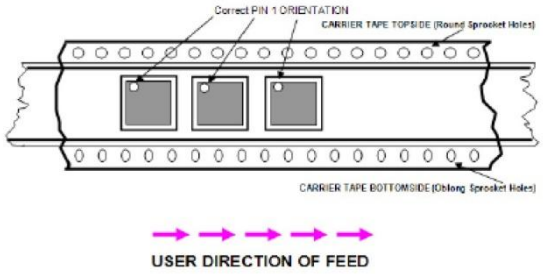
8. Package Outline Drawings

The package outline drawings are accessible from the Axiro website. The package information is the most current data available and is subject to change without revision of this document.

9. Ordering Information

Part Number	Package	MSL Rating	Carrier Type	Temp. Range
RA81F1280STGNH#BD0	5 × 5 mm, 32-VFQFPN	1	Tray	-40° to +105°C
RA81F1280STGNH#HD0	5 × 5 mm, 32-VFQFPN	1	Tape & Reel	-40° to +105°C
RTKA81F1280ST000RU	Evaluation Board (EVB)			

Table 1. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
HD0	Quadrant 1 (EIA-481-C)	

10. Revision History

Revision	Date	Description
2.00	May 14, 2026	Updated document branding and layout to Axiro Semiconductor standard. No changes to device functionality or specifications.