F39510

RF Power Amplifier Bias Controller

The F39510 is a precise, temperature-stable bias controller for RF power amplifier (PA) applications. The F39510 features six 13-bit DACs with two auxiliary DACs providing a programmable clamp voltage, one -40°C to 150°C internal temperature sensor, and one 12-bit ADC for internal and remote temperature supervision of an RF power amplifier.

The F39510 features two DAC output modes that support a wide programmable range. The first mode supports GaN PA applications with a range of -10V to 0V, while the second mode supports LDMOS PA applications with a range of 0V to +5V. The ADC has a switchable input that can read between the internal temperature sensor, and a remote temperature diode sensor through the TEMP+ and TEMP- inputs.

Competitive Advantage

- Precise programmable bias generation
- Wide operating temperature range
- High Sourcing and Sinking DAC output current

Applications

- GaN or LDMOS PA bias controller
- 5G mMIMO/Macro base-stations
- Wireless infrastructure
- General consumer products

Features

- Six 13-bit DAC output channels
- Selectable range:
  - -10V to 0V (GaN applications)
  - 0 to 5V (LDMOS applications)
- High current capability:
  - Sourcing: up to 100mA
  - Sinking: up to 30mA
- Auto-range detector
- Selectable clamp voltage
- Output On/Off control:
  - Switching delay TSW 55ns (typical)
  - Switch Ron 2.5Ω (typical)
- 12-bit SAR ADC
  - 1 remote temperature sensing input
- Out of range alarm
- Internal temperature sensor
  - Accuracy: -40°C to 125°C, ±3.5°C
- Configurable I3C basic/I²C and SPI interface
- Absolute maximum junction temperature: -40°C to +150°C
- Specification temperature (Exposed pad): -40°C to +125°C
- 4 × 4 mm 24-VFQFPN package

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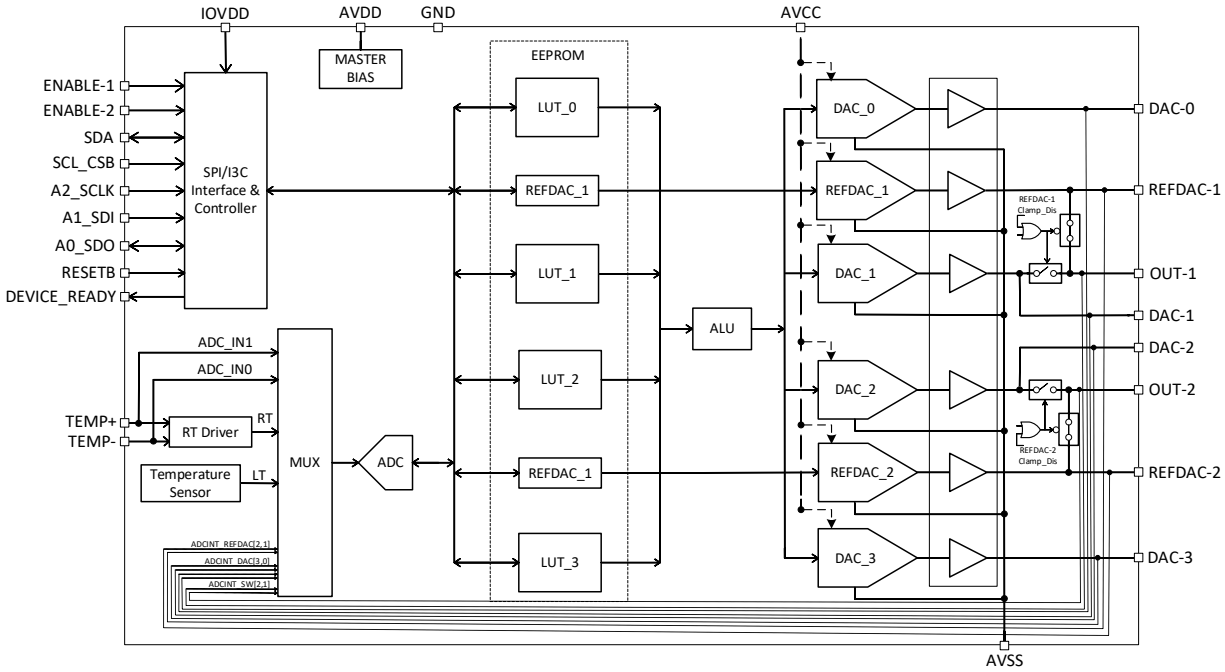

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1. Overview

1.1 Block Diagram

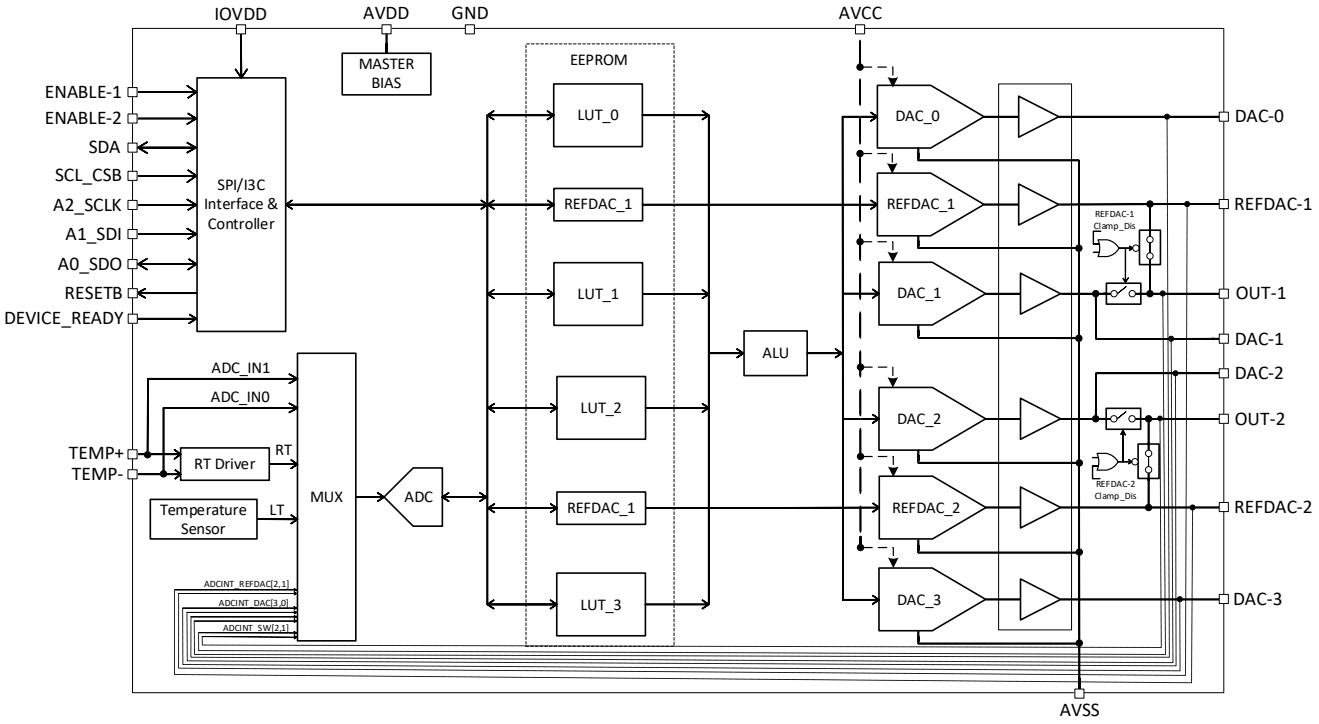
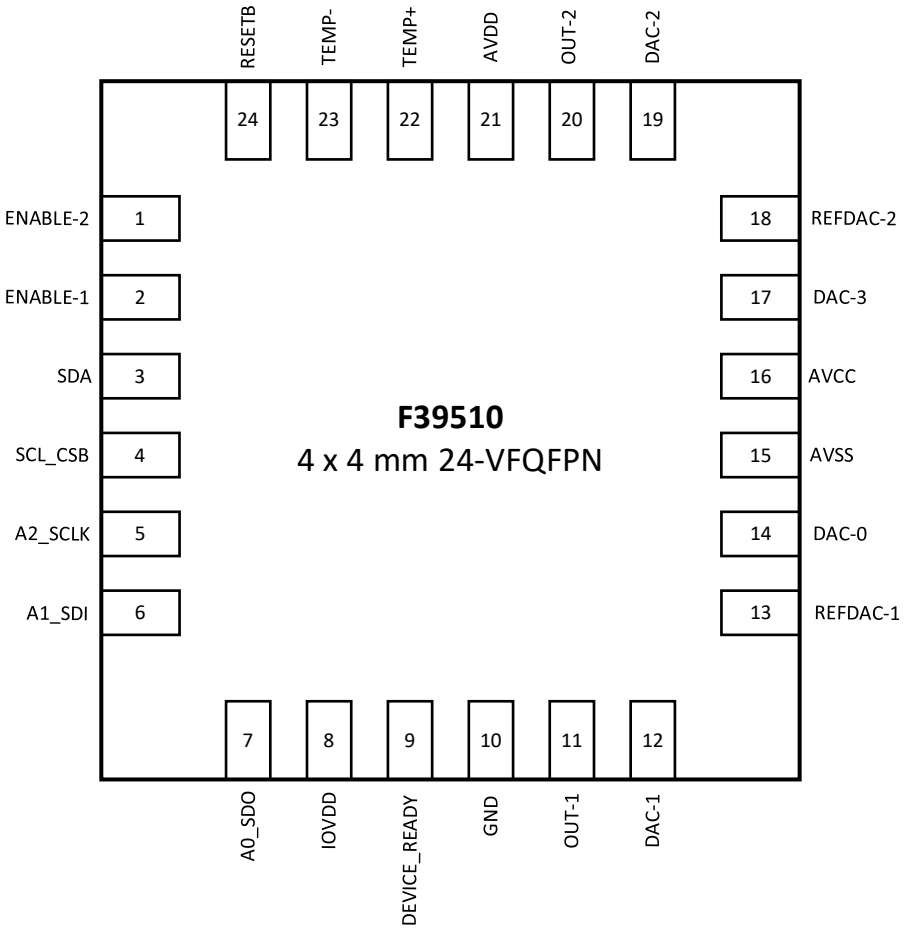


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	ENABLE-2	Control signal to select OUT-2 between DAC-2 and REFDAC-2.
2	ENABLE-1	Control signal to select OUT-1 between DAC-1 and REFDAC-1.
3	SDA	I3C BASIC/I2C Bidirectional data line. SDA pin connected to GND in SPI mode.
4	SCL_CSB	I3C BASIC/I^{2}C clock line or SPI enable serial data.
5	A2_SCLK	I3C BASIC/ I^{2}C address 2 or SPI Clock.
6	A1_SDI	I3C BASIC/ I^{2}C address 1 or SPI Data In.
7	A0_SD0	I3C BASIC/ I^{2}C address 0 or SPI Data Out.
8	IOVDD	Digital interface supply.

Pin Number	Pin Name	Description
9	DEVICE_READY	Digital output signal for bias sequencing.
10	GND	Ground.
11	OUT-1	Switched output signal between DAC-1 and REFDAC-1, controlled by Enable-1.
12	DAC-1	DAC-1 buffer output signal.
13	REFDAC-1	DAC-1 reference output signal.
14	DAC-0	DAC-0 buffer output signal.
15	AVSS	DAC Negative supply 0: -10 or GND.
16	AVCC	DAC Positive supply 0: 5V or GND.
17	DAC-3	DAC-3 buffer output signal.
18	REFDAC-2	DAC-2 reference output signal.
19	DAC-2	DAC-2 buffer output signal.
20	OUT-2	Switched output signal between DAC-2 and REFDAC-2, controlled by Enable-0.
21	AVDD	5.4V Analog input supply.
22	TEMP+	Remote temperature sensor 1 – Positive input.
23	TEMP-	Remote temperature sensor 1 – Negative input.
24	RESETB	Active low reset input. Logic low on this pin causes the device to initiate a reset event. Alternatively, this pin can be configured as an active low alarm signal in the device to initiate an alarm event.
-	Thermal Pad	The thermal pad is located on the bottom-side of the device package. The thermal pad should be tied to GND.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter		Minimum	Maximum	Unit
Supply Voltage	IOVDD to GND	-0.3	6	V
	AVDD to GND	-0.3	6	
	AVCC to GND	-0.3	6	
	AVSS to GND	-11	0	
Pin Voltage	TEMP± analog input voltage to GND	0	5	V
	DAC-[0-3] outputs to GND	AVSS - 0.3	AVCC + 0.3	
	SDA, RESET, DEVICE_READY to GND	-0.3	IOVDD + 0.3	
	OUT-1 output to GND	AVSS - 0.3	AVCC + 0.3	
	OUT-2 output to GND	AVSS - 0.3	AVCC + 0.3	
	A0_SDO, A1_SDI, A2_SCLK, SCL_CSB to GND	-0.3	IOVDD + 0.3	
	ENABLE-1, ENABLE-0	-0.3	IOVDD+ 0.3	
Pin Current	TEMP± analog input current	-0.10	0.10	mA
	DAC_[0-3] analog input current	-200	200	
	OUT-1 analog input current	-200	200	
	OUT-2 analog input current	-200	200	
Operating Temperature Referenced from Exposed Paddle (T_{EP})		-40	150	°C
Junction Temperature, TJmax		-40	150	°C
Storage Temperature, Tstg		-40	150	°C
ESD Rating – Human Body Model (Tested per JS-001-2017)		2		kV
ESD Rating – Charged-Device Model (Tested per JS-002-2014)		500		V

3.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JB} (°C/W)
24-VFQFPN, 4 × 4 mm	37.11	2.82

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct-attach features. See TB379.
2. For θ_{JB}, the board temperature is taken on the board near the edge of the package, on a copper trace at the center of one side. See TB379.

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
I_{OVDD}	1.7	3.6	V
A_{VDD}	4.7	5.5	V
A_{VCC}	0	5.5	V
A_{VSS}	-10	0	V
Operational Temperature[1]	-40	125[2]	°C

1. Temperature is referenced to the package bottom exposed pad.
2. Should the operational temperature exceed 125°C for a short time interval, the F39510 will remain operational as long as the junction temperature does not cross 150°C. Exposure to these conditions for extended periods of time may affect device reliability.

3.4 Electrical Specifications: DAC

The electrical ratings specified in this section apply to all specifications in this document unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device's parametric or functional specifications for the life of the product containing it. All specifications are guaranteed by design and characterization unless otherwise mentioned. For DAC groups in negative mode: A_{VDD} = 4.7V to 5.5V, I_{OVDD} = 1.8V to 3.6V, A_{VCC} = 0V, GND = 0 V, A_{VSS} = -8V. For DAC groups in positive mode: A_{VDD} = 4.7V to 5.5V, I_{OVDD} = 1.8V to 3.6V, A_{VCC} = 5V, GND = 0 V, A_{VSS} = 0V. No load on the DACs, T_{EP} = -40°C to 125°C.

Parameter	Conditions	Minimum	Typical	Maximum	Unit
DAC DC Accuracy					
Resolution		13	-	-	Bits
INL Relative Accuracy	Measured by a line passing through codes. -8V to -1V range.	-	±2.5	±4	LSB
	Measured by a line passing through codes. 0.5V to 4.5V range.	-	±2	±3.5	
DNL Differential Nonlinearity (1)	Measured by a line passing through codes. -8V to -1V range.	-	1	±2	LSB
	Measured by a line passing through codes. 0.5V to 4.5V range.	-	±1.5	±2	
Offset Error	T_{EP} = 25°C, Negative Mode - measured by a line passing through codes, -8V to -1V range.	-	±2.5	±25	mV
	T_{EP} = 25°C, Positive Mode - measured by a line passing through codes, 0.5V to 4.5V range.	-	±1.5	±10	mV

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Mid-code Error	T_{EP} = 25°C, Negative Mode, -8V to -1V range.	-	±2.5	±25	mV
	T_{EP} = 25°C, Positive Mode, 0.5V to 4.5V range.	-	±2	±15	mV
Gain Error (2)	T_{EP} = 25°C, measured by a line passing through codes, -8 V to -1V range.	-	±0.05	±0.35	%FSR
	T_{EP} = 25°C, measured by a line passing through codes, 0.5V to 4.5V range.	-	±0.05	±0.35	
DAC Output Characteristics					
Output Voltage Settling Time	Switching from -9.9V to -0.1V, 90% settling C_L = 15µF. -10V to 0V range.	-	2	-	ms
	Switching from 0.1V to 4.9V, 90% settling C_L = 15µF. 0V to 5V range.	-	2	-	ms
Short Circuit Current	Full-scale current shorted to the DAC group A_{VSS} or A_{VCC} voltage.	-80	-	200	mA
Load Current(3)	Negative Mode: Source or sink with 2V headroom from the DAC group A_{VCC} or A_{VSS} voltage.	-30	-	+100	mA
	Positive Mode: Source or sink with 2V headroom from the DAC group A_{VCC} or A_{VSS} voltage.	-20	-	+50	
Maximum Capacitive Load(4)	R_L = ∞, Low capacitance range (default range).	0	-	0.1	µF
	R_L = ∞, High capacitance range.	0.1	-	15	µF
Clamp Outputs					
Clamp Output Voltage(5)	DAC output range: Negative Mode, A_{VSS} = -8V.	-	AVSS	-	V
	DAC output range: Positive Mode, A_{VSS} = GND.	-	0	-	V
Clamp Output Impedance	-	-	5	-	kΩ

1. Glitches in the DNL are not included in the specification. For more information refer to section 5.3.1.1.
2. The internal reference contribution not included.
3. The output voltage of each DAC group must not be greater than that of the corresponding A_{VCC} pin or lower than that of the corresponding A_{VSS} pin.
4. If all channels are simultaneously loaded, care must be taken to ensure the thermal conditions for the device are not exceeded.
5. To be sampled during initial release to ensure compliance, not subject to production testing.
6. No DAC load to the DAC group A_{VSS} pin.

3.5 Electrical Characteristics: ADC and Temperature Sensor

The electrical ratings specified in this section apply to all specifications in this document unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device's parametric or functional specifications for the life of the product containing it. All specifications are guaranteed by design and characterization unless otherwise mentioned. A_{VDD} = 4.7V to 5.5V, I_{OVDD} = 1.8V to 3.6V, T_{EP} = -40°C to 125°C.

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Resolution	-	12	-	-	-
Integral Nonlinearity	-	-	-	±2	LSB
Differential Nonlinearity	-	-	-	±1.5	LSB
Unipolar Analog Inputs: ADC-[0] to ADC-[1]					
Absolute Input Voltage Range	-	0	-	5	V
Full-scale Input Range	-	0	-	2 × Vref	V
DC Input Leakage Current	Unselected ADC input	-	-	±10	µA
Offset Error	T_{EP} = 25°C	-	±1.5	±5	LSB
Gain Error(1)	T_{EP} = 25°C	-	±1.5	±5	LSB
Update Time	Single unipolar input, temperature sensor disabled	-	11.5	-	µs
Temperature Sensor					
Operating Range	-	-40	-	150	°C
Accuracy	Local Temperature Sensor T_{EP} = -40°C to 125°C, A_{VDD} = 5V	-	±1.5	±3.5	°C
	Local Temperature Sensor T_{EP} = 125°C to 150°C, A_{VDD} = 5V	-	-	±5.5	
	Remote Temperature Sensor [2] T_{DIODE} = -40°C to 25°C	-	±1	±3	°C
	Remote Temperature sensor [2] T_{DIODE} = 25°C to 150°C	-	-	±5	
Resolution	LSB size	-	0.25	-	°C
Conversion Time	Local Temperature Sensor	-	157.44 [3]	-	µs
	Remote Temperature Sensor	-	250 [3]	-	µs
Remote Sensor Source Current	-	10	-	120	µA

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
ADC Update Time					
Internal Oscillator Frequency	-	5.68	6.50	6.57	MHz
ADC Update Time	2 Unipolar ADC inputs enabled, Temperature sensor disabled.	-	14.7	-	µs
	2 Unipolar ADC inputs enabled, Temperature sensor enabled.	-	171	-	µs

1. The internal reference contribution is not included.
2. Characterized using external transistor.
3. Based on typical oscillator frequency of 26MHz.

3.6 Electrical Characteristics: General

The electrical ratings specified in this section apply to all specifications in this document unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device's parametric or functional specifications for the life of the product containing it. All specifications are guaranteed by design and characterization unless otherwise mentioned. For DAC groups in negative mode: A_{VDD} = 4.7V to 5.5V, I_{OVDD} = 1.8V to 3.6V, A_{VCC} = 0V, GND = 0 V, A_{VSS} = -8V. For DAC groups in positive mode: A_{VDD} = 4.7V to 5.5V, I_{OVDD} = 1.8V to 3.6V, A_{VCC} = 5V, GND = 0 V, AVSS = 0V. No load on the DACs, T_{EP} = -40°C to 125°C

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
A_{VSS} Detector					
A_{VSS} Threshold Detector (A_{VSS})	-	-3.5	-	-1.5	V
Power Requirements					
I_{AVDD} A_{VDD} Supply Current	(Negative Range) No DAC load, all DACs at 0x1000 code and ADC at the fastest auto conversion rate.	-	12	15	mA
I_{IOVDD} I_{OVDD} Supply Current		-	0.1	1	
I_{AVCC} A_{VCC} Supply Current		-	10	12	
I_{AVSS} A_{VSS} Supply Current		-	15	18	
Power Consumption		-	180	-	mW
I_{AVDD} A_{VDD} Supply Current	(Positive Range) No DAC load, all DACs at 0x1000 code and ADC at the fastest auto conversion rate.	-	9	12	mA
I_{IOVDD} I_{OVDD} Supply Current		-	0.1	1	
I_{AVCC} A_{VCC} Supply Current		-	6	8	
I_{AVSS} A_{VSS} Supply Current		-	8	11	
Power Consumption		-	75		mW
I_{AVDD} A_{VDD} Supply Current	(Negative Range): Power-down mode.	-	11	14	mA
I_{IOVDD} I_{OVDD} Supply Current		-	0.1	1	
I_{AVCC} A_{VCC} Supply Current		-	3	5	
I_{AVSS} A_{VSS} Supply Current		-	9	12	

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Power Consumption		-	127	-	mW
I_{AVDD} A_{VDD} Supply Current	(Positive Range): Power-down mode.	-	11	13	mA
I_{IOVDD} I_{OVDD} Supply Current		-	0.1	1	
I_{AVCC} A_{VCC} Supply Current		-	2	4	
I_{AVSS} A_{VSS} Supply Current		-	7	9	
Power Consumption		-	65	-	mW

3.7 Output Switching Specifications

All specifications are guaranteed by design and characterization unless otherwise mentioned. Recommended operating conditions, For DAC groups in negative mode: A_{VDD} = 4.7V to 5.5V, I_{OVDD} = 1.8V to 3.6V, A_{VCC} = 0V, GND = 0 V, A_{VSS} = -8V. For DAC groups in positive mode: AVDD = 4.7V to 5.5V I_{OVDD} = 1.8V to 3.6V, A_{VCC} = 5V, GND = 0 V, A_{VSS} = 0V. No load on the DACs, T_{EP} = -40°C to 125°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Unit
Source Current Capability	I_{SOURCE}	Negative Mode	-	-	100	mA
		Positive Mode	-	-	50	
Sink Current Capability	I_{SINK}	Negative Mode	-	-	30	mA
		Positive Mode	-	-	20	
Resistance in DAC Position (on-resistance)	R_{ON}	-	-	2.5	-	Ω
Resistance in Vref Position (off-resistance)	R_{OFF}	-	-	1	-	MΩ
DAC Load Capacitor [2]	C1	Low Capacitance Range	0	-	0.1	µF
		High Capacitance Range	0.1	-	15	µF
OUT-1/2 Load Capacitor[1]	C2	-	-	12	-	nF
Switch Delay [1]	T_{SW}	With load capacitor = 12nF	-	55	70	ns
OUT-1/2 Output Voltage [3][3]	-	Positive DAC range	0	-	5	V
	-	Negative DAC range	-10	-	-0	V

1. See timing diagram Figure 3.
2. See Figure 4.
3. Series switch is ON, OUT-1/2 output = DAC Output. Shunt switch is ON, OUT-1/2 output = REFDAC-1 or REFDAC-2 Output depending on DAC group.
4. Positive DAC range max limited to 3.5V when Series switch is OFF (Shunt switch is ON).

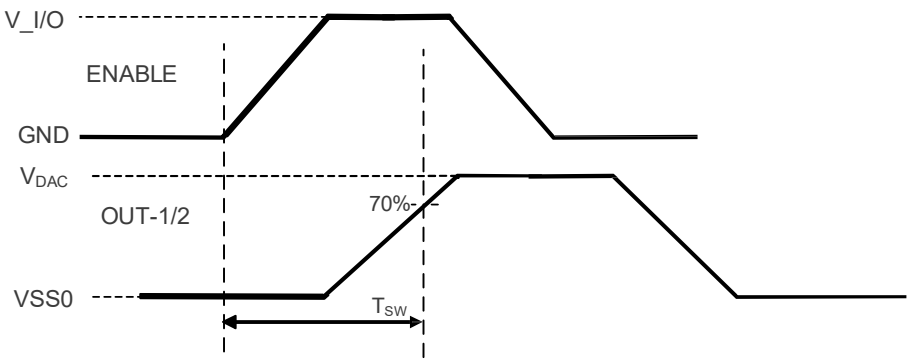


Figure 3. Timing Diagram Output Switch

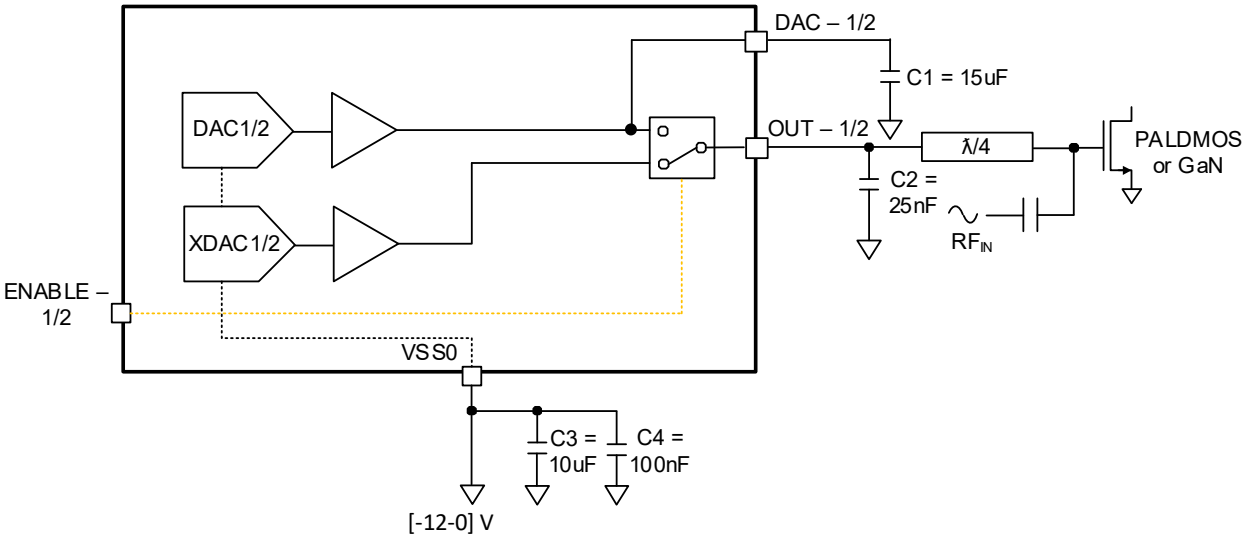


Figure 4. Output Switch Loading Application Diagram

3.8 SPI Interface Specifications

C_{SB} = 0V, I_{OVDD} = 1.8V to 3.6V, A_{VDD} = 4.7V to 5.5V, A_{VCC} = 0V, GND = 0V, A_{VSS} = -10V (for DAC groups in negative range) and A_{VDD} = 4.7V to 5.5V, A_{VCC} = 5V, GND = 0V, A_{VSS} = 0V (for DAC groups in positive ranges), DAC output range = 0 to 5V for all groups, no load on the DACs, T_{EP} = -40°C to 125°C.

Parameter	Test Conditions	Min	Typ	Max	Unit
Serial Interface [1]					
IOV_{DD} (internal)	-	-	1.8	-	V
$f_{(SCLK)}$ SCLK Frequency	-	-	-	15	MHz
t_p SCLK Period [2]	-	66.67	-	-	ns
t_{PH} SCLK Pulse Width High [2]	-	30	-	-	ns
t_{PL} SCLK Pulse Width Low [2]	-	30	-	-	ns
t_{su} MISO Setup [2]	-	10	-	-	ns
t_h MISO Hold [2]	-	10	-	-	ns
$t_{(ODZ)}$ MOSI Driven to Tri-state [3][4]	-	0	-	15	ns
$t_{(OZD)}$ MOSI Tri-state to	-	0	-	23	ns
$t_{(OD)}$ MOSI Output Delay [3][4]	-	0	-	23	ns
$t_{su(CM)}$ CM Setup [2]	-	5	-	-	ns
$t_{h(CM)}$ CM Hold [2]	-	20	-	-	ns
$t_{(IAG)}$ Inter-access Gap [2]	-	10	-	-	ns
Digital Logic					
High-level Input Voltage		0.7 × IOV_{DD}	-	-	V
Low-level Input Voltage		-	-	0.45	V
High-level Output Voltage: $I_{(LOAD)}$ = -1mA		IOV_{DD} – 0.4	-	-	V
Low-level Output Voltage: $I_{(LOAD)}$ = 1mA		-	-	0.4	V
Reset Delay; Delay-to-Normal Operation from Reset		-	100	250	µs
Power-down Recovery Time		-	-	70	µs
Convert Pulse Width		20	-	-	ns
Reset Pulse Width		20	-	-	ns
ADC WAIT State(5); the wait time from when the ADC enters the IDLE state to when the ADC is ready for trigger		2	-	-	µs

1. Specified by design and characterization. Not tested during production.
2. See Figure 5 and Figure 6.
3. MISO loaded with 10pF load capacitance for SDO timing specifications.
4. See Figure 6.
5. Specified by design; not subject to production testing.

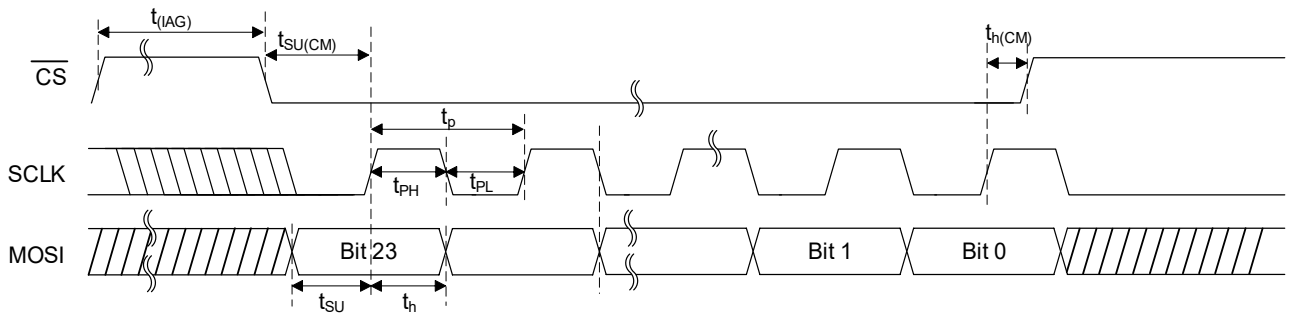


Figure 5. Serial Interface Write Timing Diagram

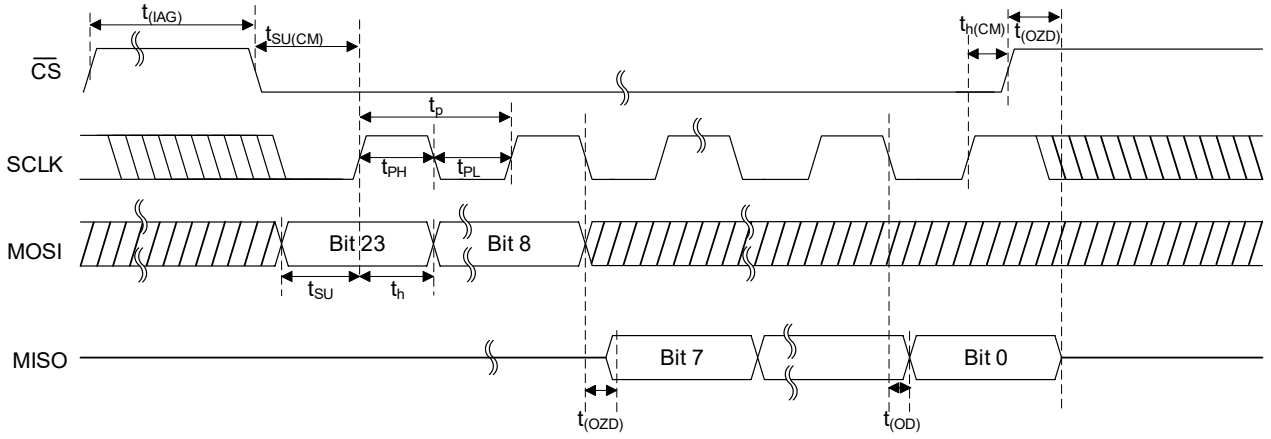


Figure 6. Serial Interface Read Timing Diagram

3.9 I3C BASIC and I²C Interface Specification

C_{SB} = 1.8V (I3C 1.8V) or 3.3V (I3C 3.3V), I_{OVDD} = 1.8V to 3.6V, A_{VDD} = 4.7V to 5.5V, A_{VCC} = 0V, GND = 0V, A_{VSS} = -10V (for DAC groups in negative range) and A_{VDD} = 4.7V to 5.5V, GND = 0V, A_{VCC} = 5V, A_{VSS} = 0V (for DAC groups in positive ranges), DAC output range = 0V to 5V for all groups, no load on the DACs, T_{EP} = -40°C to 125°C.

Table 1. I3C I/O Stage Characteristics Common to Push-Pull Mode and Open Drain Mode

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Operating Voltage	V_{DD}	-	1.65	1.80	1.95	V
			2.97	3.30	3.63	
Low-Level Input Voltage	V_{IL}	-	-0.1 * V_{DD}	-	0.3 * V_{DD}	V
High-Level Input Voltage	V_{IH}	-	0.7 * V_{DD}	-	1.1 * V_{DD}	V
Schmitt Trigger Inputs Hysteresis	Vhys	-	0.1 * V_{DD}	-	-	V
Output Low Level	V_{OL}	For V_{DD} ≥ 1.4V: I_{OL} = 3 mA	-	-	0.27	V
Input Current (per Input-Only I/O Pin)	Ii	-100mV < Vi < V_{DD} + 100mV for ≥ 1.8V nominal	-10	-	10	µA
Capacitance (per I/O pin)	Ci	For ≥ 1.8V nominal	-	-	10	pF

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Capacitance Mismatch Between Pins	ΔC	Difference between SDA and SCL capacitance C_L ≤ 5pF	-	-	1.5	pF
		Difference between SDA and SCL capacitance C_L > 5pF	-	-	3	pF
Push-Pull Only						
Output High Level	V_{OH}	For V_{DD} ≥ 1.4V: I_{OH} = -3mA	V_{DD} – 0.27	-	-	V
Legacy Mode with Pull-Up						
Pull-Up for Open Drain	Rp	tr = Max rise time Cb = Bus Capacitance V_{DD} = 1.8V, or 3.3V	$\frac{V_{DD} - V_{OL}}{3\ mA}$ for $V_{DD} \geq 1.4V$		$\frac{t_r}{0.8473 \times Cb}$	Ω
		tr = 120ns Cb = 50pF			-	

Table 2. I3C Interface AC Characteristics of I²C Legacy Modes

No. [1]	Parameter	Symbol	Legacy Mode 400kHz / Fm		Unit
			Minimum	Maximum	
-	SCL Clock Frequency	f_{SCL}	0.01	0.4	MHz
1	Setup Time for a Repeated START	$t_{SU\ STA}$	600	-	ns
2	Hold Time for a (Repeated) START	$t_{HD\ STA}$	600	-	ns
3	SCL Clock Low Period	t_{LOW}	1300	-	ns
4	SCL Clock High Period	t_{HIGH}	600	-	ns
5	Data Setup Time	t_{SU_DAT}	100	-	ns
6	Data Hold Time	t_{HD_DAT}	-	-	ns
7	Setup Time for STOP	t_{SU_STO}	600	-	ns
-	SCL and SDA Timeout	$t_{TIMEOUT}$	25	35	ms

1. See Figure 7.

Table 3. I3C Open Drain Timing Parameters

No. [1]	Parameter	Symbol	I3C Open Drain Mode		Unit
			Minimum	Maximum	
8	SCL Clock Low Period	t_{LOW_OD}	200	-	ns
-	SCL Clock High Period (for First Broadcast Address)	t_{HIGH_INIT}	200	-	ns
9	SCL Clock High Period (for Mixed Bus)	t_{HIGH}	-	41	ns
9	SCL Clock High Period (for Pure Bus)	t_{HIGH}	24	-	ns
10		t_{DIG_H}	32	-	ns

No. [1]	Parameter	Symbol	I3C Open Drain Mode		Unit
			Minimum	Maximum	
11	Data Setup Time During Open Drain	t_{SU_OD}	3	-	ns

1. See Figure 8.

Table 4. I3C Push-Pull Timing Parameters for SDR Mode

No. [1]	Parameter	Symbol	I3C Push-Pull Mode			Unit
			Minimum	Typical	Maximum	
-	SCL clock frequency 1.8V	f_{SCL}	0.01	TBD	TBD	MHz
-	SCL clock frequency 3.3V	f_{SCL}	0.01	12.5	12.9	MHz
12	SCL Clock Low Period	t_{LOW}	24	-	-	ns
13		t_{DIG_L}	32	-	-	ns
14	SCL Clock High Period (for Mixed Bus)	t_{HIGH_MIXED}	24	-	-	ns
15		$t_{DIG_H_MIXED}$	32	-	45	ns
14	SCL Clock High Period (for Pure Bus)	t_{HIGH}	24	-	-	ns
15		t_{DIG_H}	32	-	-	ns
16	SDA Signal Data Hold	t_{HD_PP}	0	-	-	ns
17	SDA Signal Data Setup	t_{SU_PP}	3	-	N/A	ns
-	Capacitive Load per Bus Line (SDA/SCL)	Cb	-	-	50	pF

1. See Figure 8.

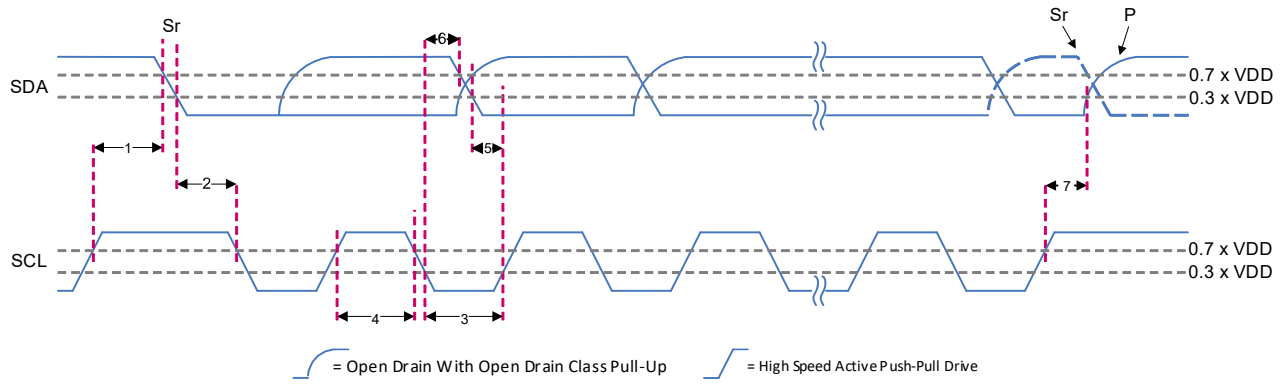


Figure 7. I3C Interface I²C Legacy Mode Timing

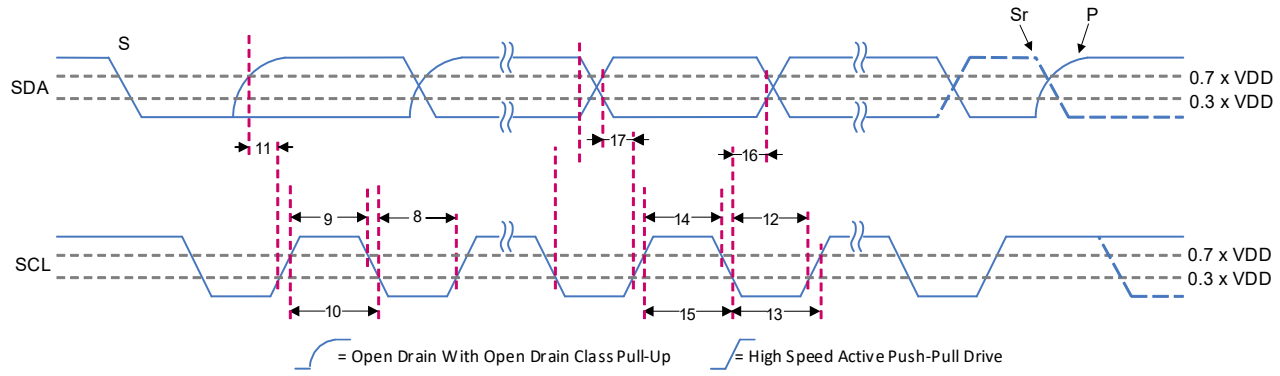


Figure 8. I3C Interface SDR Mode Timing

4. Typical Performance Graphs

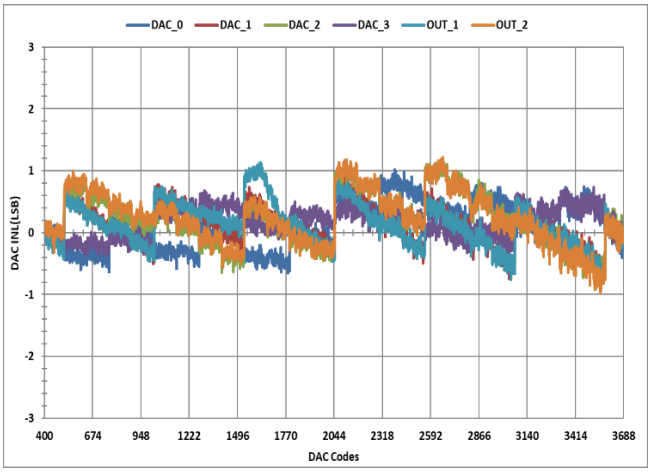


Figure 9. DAC INL, 25C (Positive Mode)

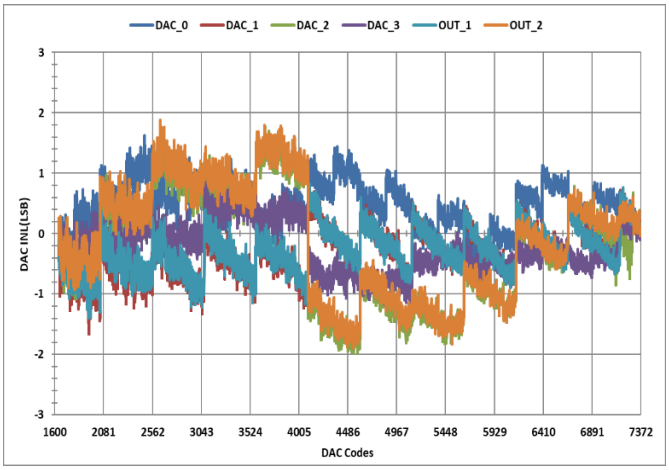


Figure 10. DAC INL, 25C (Negative Mode)

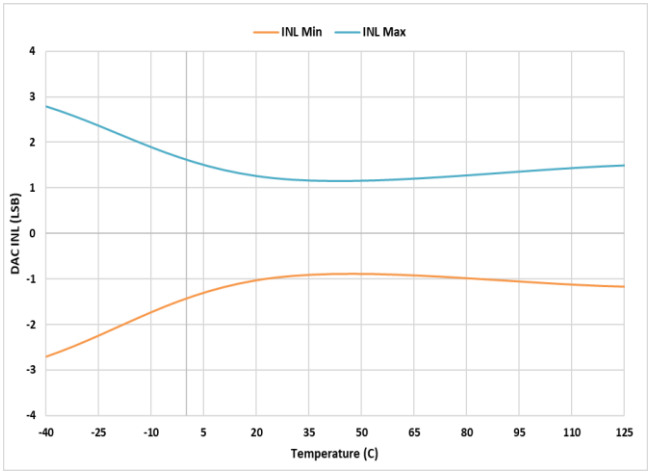


Figure 11. DAC INL vs. Temperature (Positive Mode)

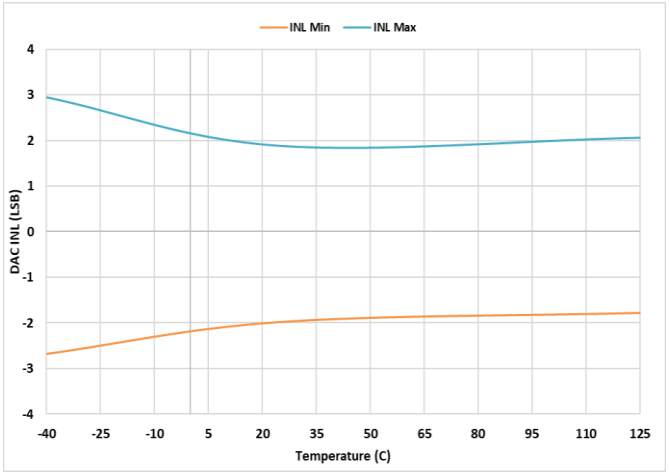


Figure 12. DAC INL vs. Temperature (Negative Mode)

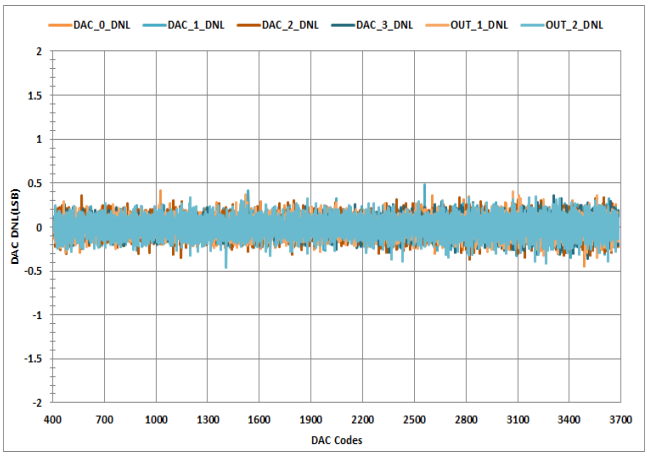


Figure 13. DAC DNL, 25C (Positive Mode)

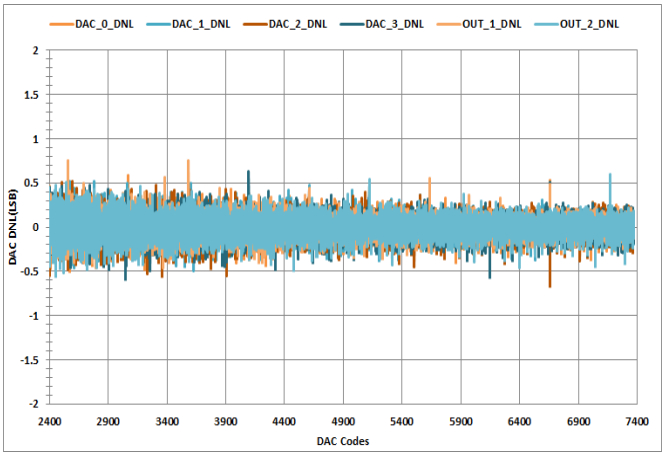


Figure 14. DAC DNL, 25C (Negative Mode)

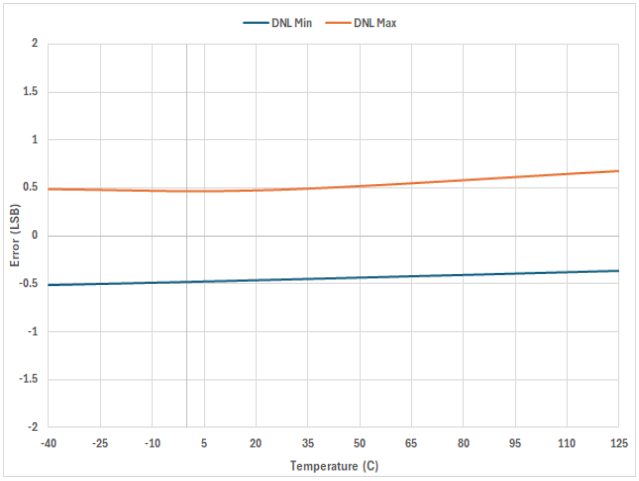


Figure 15. DAC DNL vs. Temperature (Positive Mode)

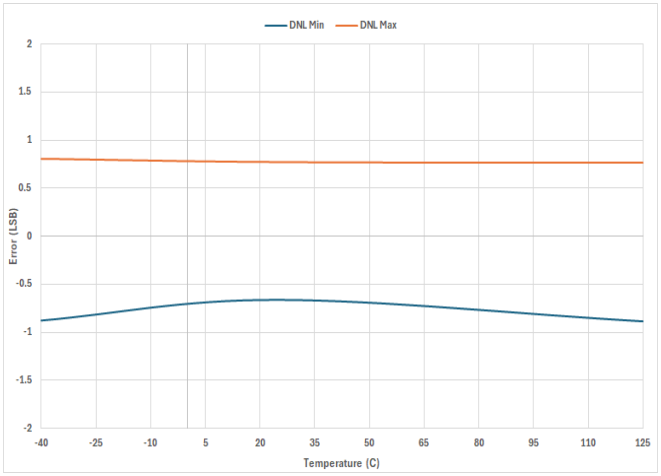


Figure 16. DAC DNL vs. Temperature (Negative Mode)

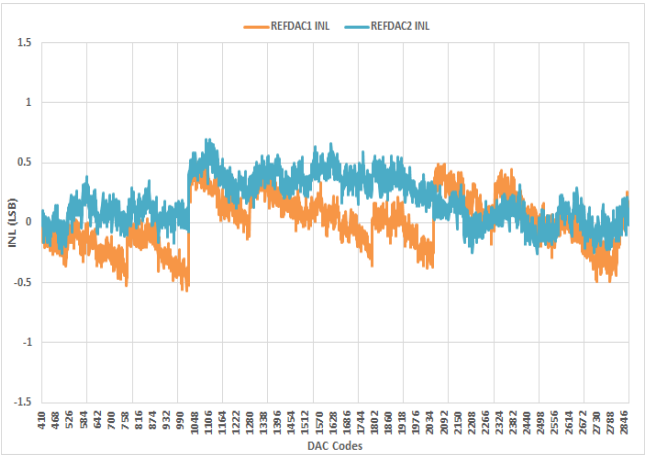


Figure 17. REFDAC INL, 25C (Positive Mode)

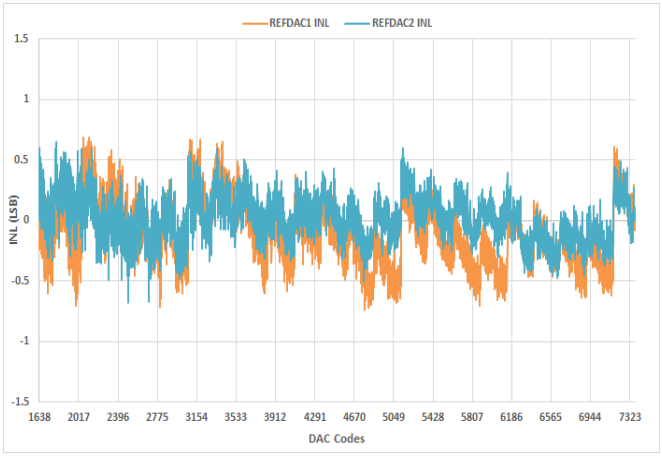


Figure 18. REFDAC INL, 25C (Negative Mode)

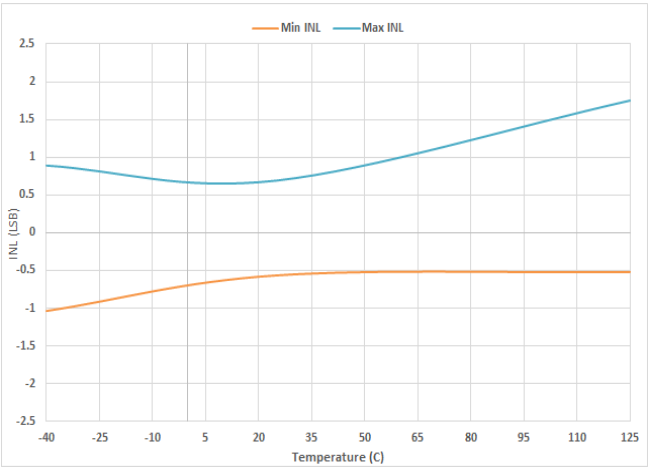


Figure 19. REFDAC INL vs. Temperature (Positive Mode)

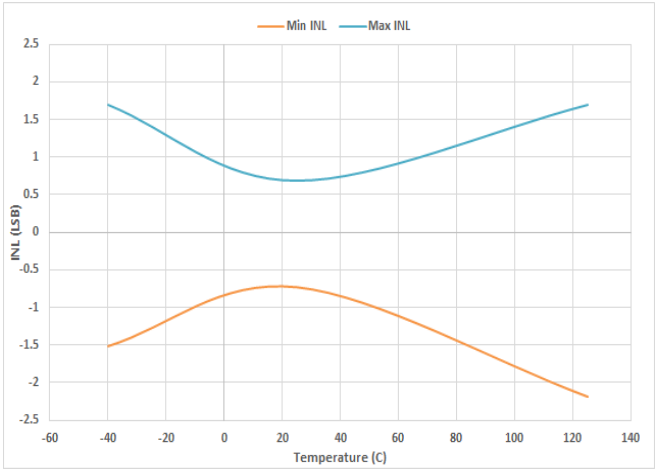


Figure 20. REFDAC INL vs. Temperature (Negative Mode)

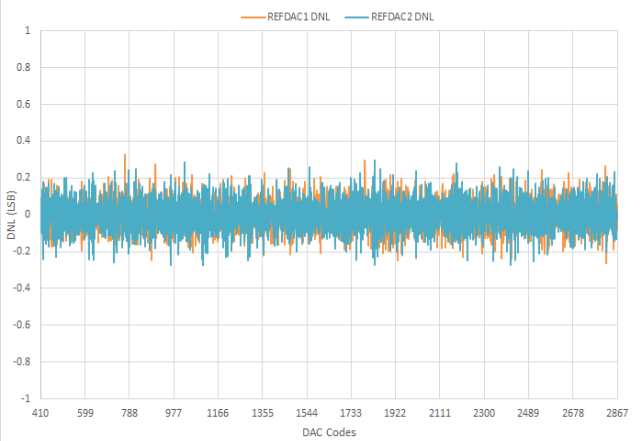


Figure 21. REFDAC DNL, 25C (Positive Mode)

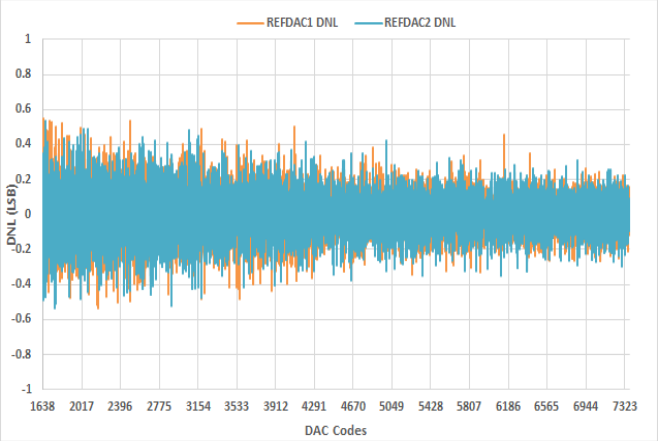


Figure 22. REFDAC DNL, 25C (Negative Mode)

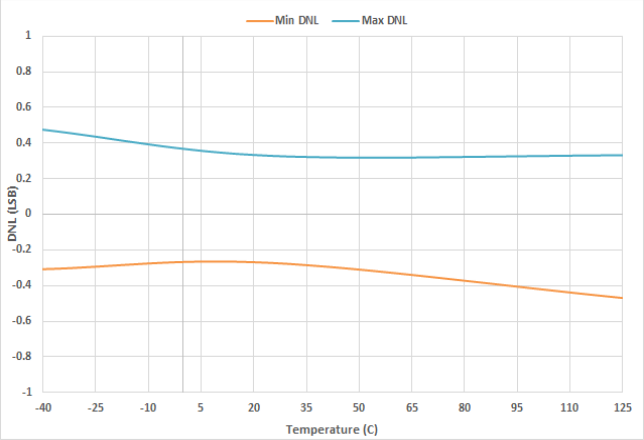


Figure 23. REFDAC DNL vs. Temperature (Positive Mode)

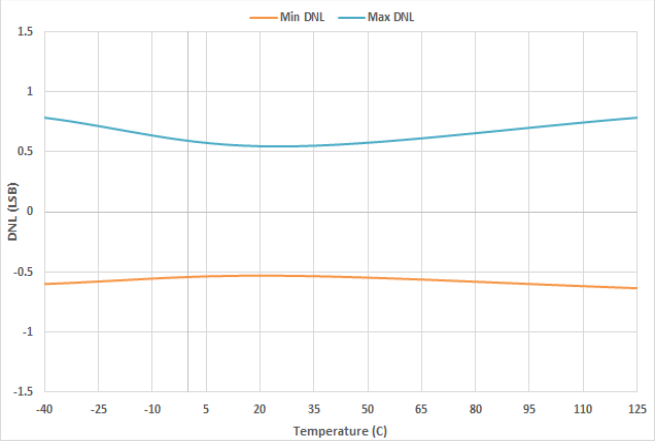


Figure 24. REFDAC DNL vs. Temperature (Negative Mode)

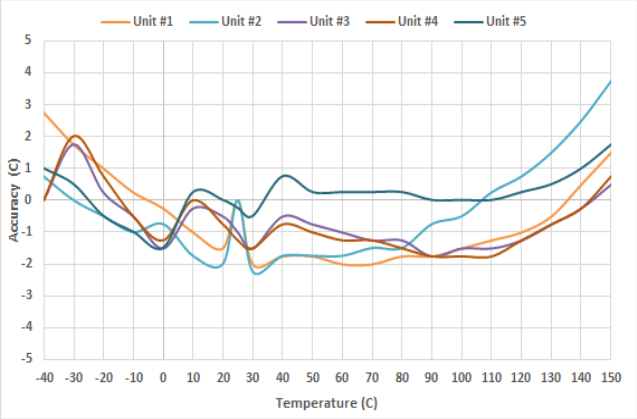


Figure 25. Local Temperature Sensor Accuracy (Positive Mode)

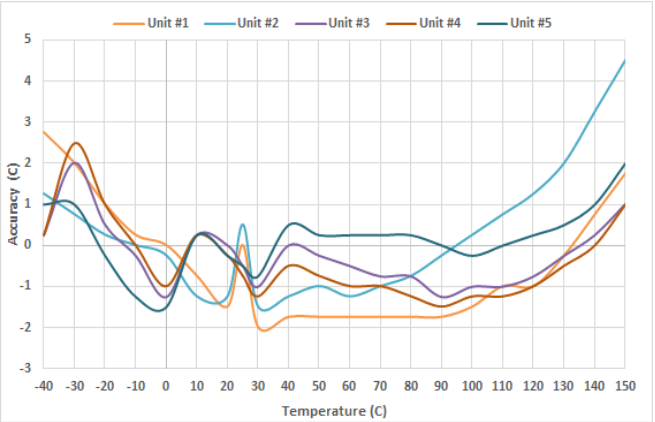


Figure 26. Local Temperature Sensor Accuracy (Negative Mode)

5. Functional Description

5.1 Overview

The F39510 is a precise, low-power, temperature stable, programmable, 6-channel bias controller for RF power amplifier (PA) applications. The F39510 features six monotonic 13-bit DACs (two DACs providing selectable clamp voltage), one 12-bit SAR ADC and an internal -40°C to 150°C temperature sensor.

The F39510 features two DAC output modes that support a wide programmable range. The first mode supports GaN PA applications with a range of -10V to 0V, while the second mode supports LDMOS PA applications with 0V to +5V. DAC-1 and DAC-2 feature output switching circuitry designed for rapid RF Power Amplifier response. Driving the gate of an RF PA through the OUT-1 (pin 11) and OUT-2 (pin 20) pins significantly reduces the PA biasing time.

The F39510 features a single ADC with a switchable input that can read between the internal temperature sensor, and a remote temperature-sensor diode driver.

5.2 Temperature Sensors (Local/Remote)

The F39510 supports local and remote temperature sensing. The onboard sensor stores the output in the local temperature data registers (address 0x00 and 0x01) and the remote temperature data output is stored in the remote temperature data registers (address 0x02 and 0x03).

Local/remote temperature data registers are initialized with 0s and will begin operation at the power-up after the supply voltage reaches its minimum operating level.

The local/remote temperature sensor result is converted by the device ADC. The local/remote temperature sensors can be disabled in the LUT Configuration Register. The acquisition time of the ADC can be increased to optimize the remote temperature measurements.

The temperature value is stored in the Local Temperature Data registers (address 0x0100 and 0x0101) and ADC Local Temperature (address 0x0124 and 0x0125). The temperature value is stored in the Remote Temperature Data registers (address 0x0102 and 0x0103) and ADC Remote Temperature (address 0x0126 and 0x0127). Three different Temperature formats can be selected:

1) Legacy Format (ADC_CFG.TEMP_RAL_FORMAT = 1)

2) Standard Format (ADC_CFG.TEMP_RAL_FORMAT = 0 and TEMP_CFG.RANGE = 0)

3) Extended Format (ADC_CFG.TEMP_RAL_FORMAT = 0 and TEMP_CFG.RANGE = 1)

Table 5. ADC Controller Temperature Data Legacy Format

Temperature (°C)	Legacy Digital Code
-40.00	1111 0110 0000
-25.00	1111 1001 1100
-10.00	1111 1101 1000
-0.25	1111 1111 1111
0	0000 0000 0000
0.25	0000 0000 0001
10.00	0000 0010 1000
25.00	0000 0110 0100
50.00	0000 1100 1000

Temperature (°C)	Legacy Digital Code
75.00	0001 0010 1100
100.00	0001 1001 0000
105.00	0001 1010 0100
125.00	0001 1111 0100
150.00	0010 0101 1000

In Legacy 12-bit two's complement format use the following equations to calculate the positive and negative temperature according to the polarity of the temperature data MSB (0 – positive, 1 – negative):

$$Positive\ Temperature\ (°C) = 'Legacy\ Digital\ Code'/4$$

$$Negative\ Temperature\ (°C) = ('Legacy\ Digital\ Code' - 4096)/4$$

This Legacy format temperature range is from -512˚C to 511.75˚C; however, the temperature sensor operates within the range of -40˚C to 150˚C.

The Legacy 12-bit two's complement format is stored right aligned in Temperature registers, in other words, upper nibble of Temperature High byte register is 4'b0000.

Table 6. ADC Controller Temperature Data Standard Format

Temperature (°C)	Legacy Digital Code
-40.00	1101 1000 0000
-25.00	1110 0111 0000
-10.00	1111 0110 0000
-0.25	1111 1111 1100
0	0000 0000 0000
0.25	0000 0000 0100
10.00	0000 1010 0000
25.00	0001 1001 0000
50.00	0011 0010 0000
75.00	0100 1011 0000
100.00	0110 0100 0000
105.00	0110 1001 0000
125.00	0111 1101 0000
150.00	0111 1111 1100

In Standard 12-bit two's complement format use the following equations to calculate the positive and negative temperature according to the polarity of the temperature data MSB (0 = positive, 1 = negative):

$$Positive\ Temperature\ (°C) = 'Standard\ Digital\ Code'/16$$

$$Negative\ Temperature\ (°C) = ('Standard\ Digital\ Code' - 4096)/16$$

This Standard format temperature range is from -128°C to 127.75°C; however, the temperature sensor operates within the range of -40°C to 150°C.

The Standard 12-bit two's complement format is stored left aligned in Temperature registers, that is the lower nibble of Temperature Low byte register is 4'b0000. The Temperature MSB data stores the temperature value with 1°C resolution and LSB data stores the decimal fractional value: since temperature sensor resolution is 0.25 only the bits <7:6> of the LSB are used. In the Extended Temperature format an offset of 64 is added to the standard binary value, as shown below.

Table 7. ADC Controller Temperature Data Extended Format

Temperature (°C)	Legacy Digital Code
-40.00	0001 1000 0000
-25.00	0010 0111 0000
-10.00	0011 0110 0000
-0.25	0011 1111 1100
0	0100 0000 0000
0.25	0100 0000 0100
10.00	0100 1010 0000
25.00	0101 1001 0000
50.00	0111 0010 0000
75.00	1000 1011 0000
100.00	1010 0100 0000
105.00	1010 1001 0000
125.00	1011 1101 0000
150.00	1011 0110 0000

In Extended 12-bit format use the following equations to calculate the positive and negative temperature:

$$Temperature\ (°C) = (\text{'}Extended\ Digital\ Code\text{'} - 1024)/16$$

This Extended format temperature range is from -64°C to 191.75°C; however, the temperature sensor operates within the range of -40°C to 150°C.

The Extended 12-bit format is stored left aligned in Temperature registers, in other words, lower nibble of Temperature Low byte register is 4'b0000. The Temperature MSB data stores the temperature value with 1°C resolution and LSB data stores the decimal fractional value: since temperature sensor resolution is 0.25 only the bits <7:6> of the LSB are used.

The selected format must be used for all temperature registers LT_DATA_H/L, ADC_LT_DATA, TEMP_OVRD_1/2 H/L, LT _UP _THR_H/L and LT _LO _THR_H/L; LT_THERM_THR trimming register uses only Legacy format, independently from the format settings.

When the full temperature value is needed, it assures that both bytes of the read operation are from the same ADC conversion the ADC_LT_DATA registers are synchronized with dac_in update command in REG_UPDATE register.

A different locking mechanism, that does not require an additional write operation, is used for LT_DATA registers: reading the MSB value first causes the LSB value to be locked until the LSB value is read. For proper operation, read the high byte of the temperature result first with ascending incremental address setting of the serial interface (default).

If a different read sequence is used, then an additional access to other register is required to unlock the LT_DATA registers and allow updates from ADC conversions.

This locking mechanism can be disabled clearing the ADC_CFG.TEMP_LOCK_EN bit stored in EEPROM: in this case it can happen that the high byte and low byte are not from same ADC conversion, so precision is lower (1°C for Standard and Extended formats)

5.3 Analog Signal Path

A simplified schematic of a single analog channel with the output switches is shown in Figure 27. The following subsections describe each of the individual blocks within a channel.

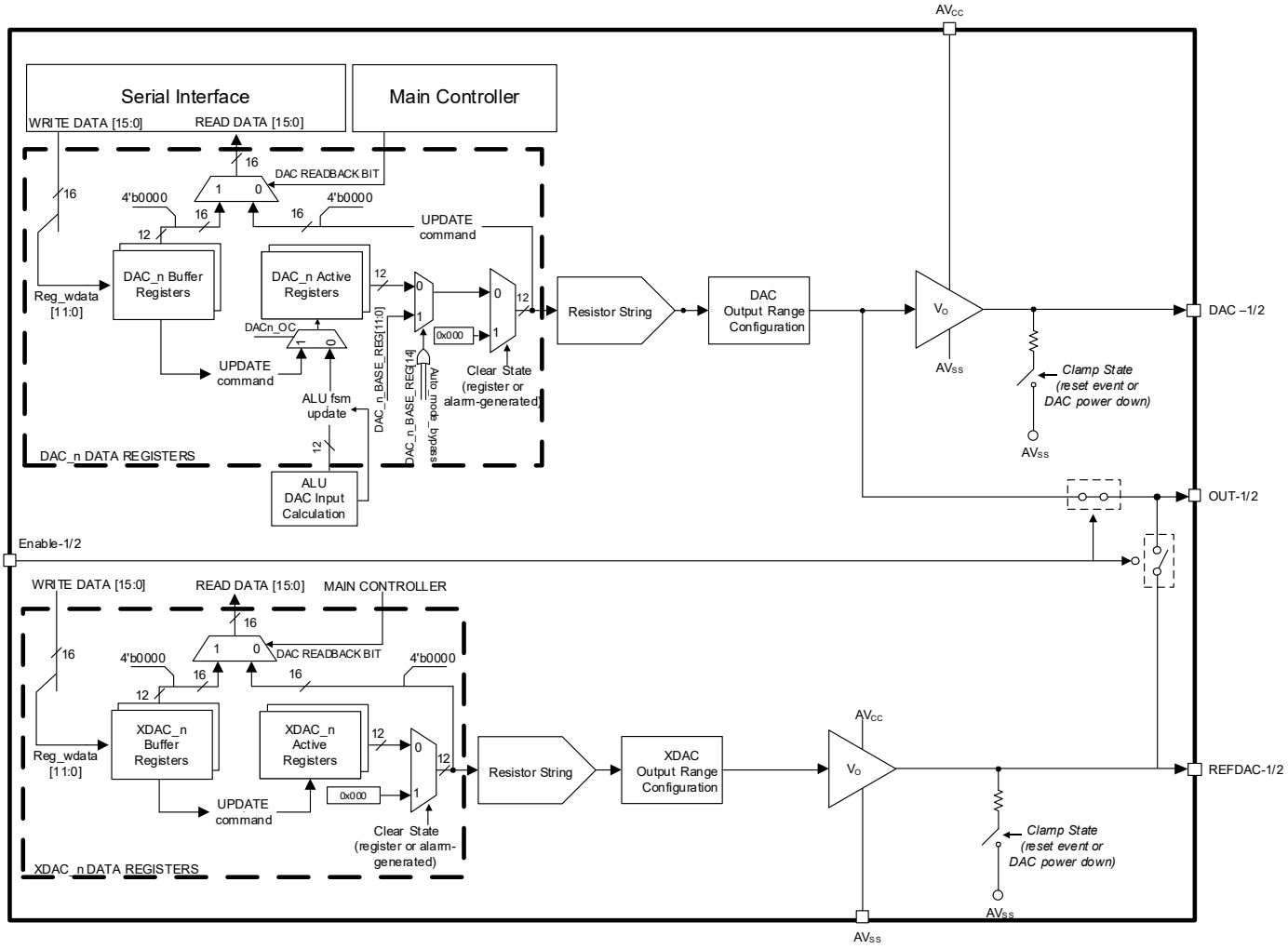


Figure 27. Single Channel Path

5.3.1. DAC

The F39510 consists of six 13-bit DACs that operate from an internal bandgap reference voltage. The auxiliary DAC (REFDAC) is used to program off voltages. The auxiliary DACS can also be used as independent DACs if required. Each DAC core consists of a resistor string DAC and an output-voltage buffer. The auxiliary DACs must always be set to a voltage lower than or equal to that of the main DACs. This does not apply to DAC0 and DAC3 as these DACs can be used independently.

5.3.1.1. DAC Differential Non-Linearity

The differential non-linearity (DNL) of the F39510 is specified as shown in Table 3.4 to be a maximum of ±2 LSB in Negative mode and a maximum of ±2 LSB in positive mode.

For the F39510, at certain DAC codes there are glitches in the DNL performance that are observed. This is limited to 1 glitch point per 512 codes only. The DNL at the points of these glitches can go up to 5 LSB however they do not affect the overall slope of the device DNL performance. The DNL for the codes above and below these points fall well within the limits shown in Table 3.4.

The error at these few select DAC codes are negligible (few mV) and are therefore not considered under the specifications for the DNL parameter in Table 3.4 as highlighted in footnote (1).

5.3.1.2. DAC Input Data

The input data of the DACs is written to the individual DAC Data registers in straight binary format for all output ranges as shown in Table 8. Ideal DAC positive and negative output voltages vs DAC Code are shown in Figure 28 and Figure 29.

Table 8. DAC Data Format

Digital Code	DAC Output Voltage (V)	
	0 to 5 V Range	-10 to 0 V Range
0 0000 0000 0000	0	-10
0 0000 0000 0001	0.00122	-9.99878
0 1111 1111 1111	4.99878	
1 0000 0000 0000	5	-5
1 111 1111 11110	5	-0.00244
1 111 1111 11111	5	-0.00122

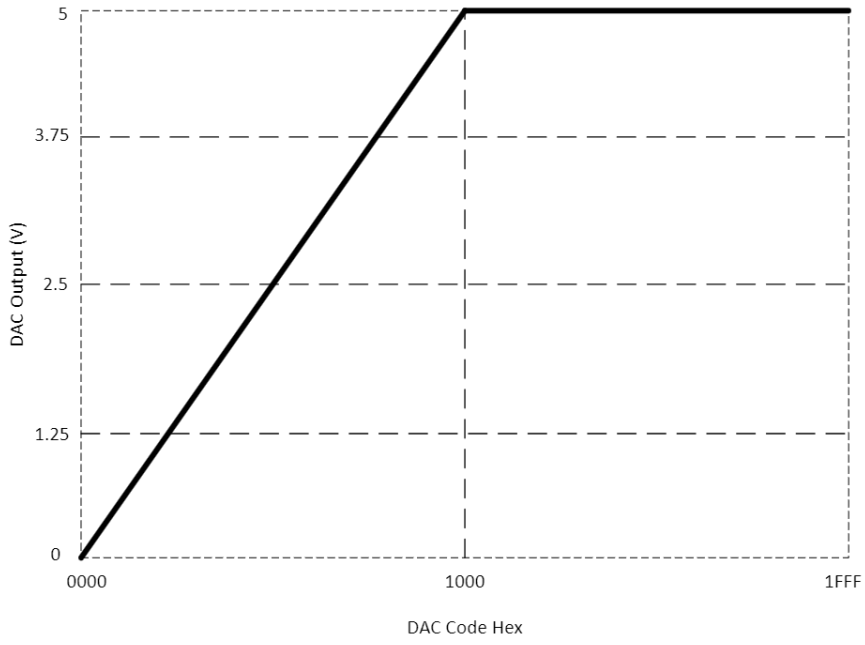


Figure 28. Ideal Positive Range DAC Output vs. DAC Code

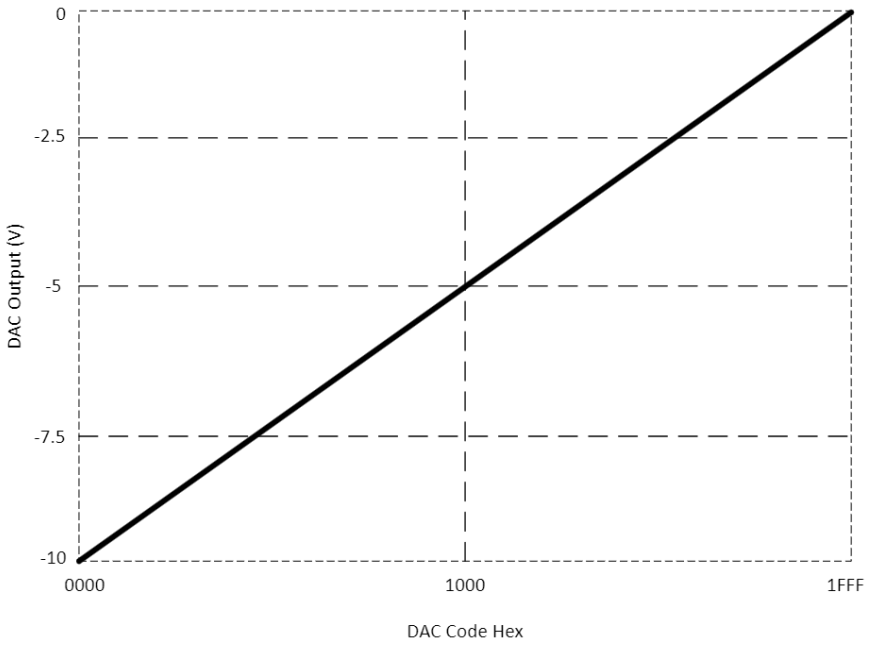


Figure 29. Ideal Negative Range DAC Output vs. DAC Code

The 13-bit input code of DAC0, DAC1, DAC2 and DAC3 is produced by the LUT/ALU and automatically stored in the Active Registers at the end of the calculation. The user can also insert the DAC input code via the DAC_x_OVRD registers (Address: 0x38 – 0x3F) by setting the correspondent bit in the OVRD_CTRL register (Address 0x15).

In this override operation mode, data written to the DAC Override Data registers is initially stored in the DAC Buffer registers. The transfer of data from the DAC Buffer registers to the DAC Active registers is initiated by an UPDATE command in the Register Update register. When the DAC Active registers are updated, the DAC outputs change to the new values.

A low clamping feature can be enabled with DAC_CLAMP_EN field of the MISC_CNTL register. When low clamping feature is enabled, if a DAC Buffer register contains a digital code that is less than the digital code of the correspondent XDAC Buffer, then the DAC Buffer code is clamped to the value of the XDAC code when it is transferred to the Active register.

The host has the option to read from either the DAC Buffer registers or the DAC Active registers when accessing the DAC Data registers. The DAC read back option is configured by the READBACK bit in the Interface Configuration 1 register. Read from DAC Active registers is synchronized with a DAC_IN update command.

In particular, in LUT/ALU mode the produced DAC input code can be read if the READBACK bit is set and an UPDATE command will update the DAC active register.

Auxiliary XDACs are used to program the off voltages of DAC-1/2. Data written to the REFDAC1 and REFDAC2 Data registers is initially stored in the DAC Buffer registers. The transfer of data from the XDAC Buffer registers to the XDAC Active registers is initiated by an UPDATE command in the Register Update register. When the XDAC Active registers are updated, the XDAC outputs change to the new values.

The host has the option to read from either the XDAC Buffer registers or the XDAC Active registers when accessing the XDAC Data registers. The DAC read back option is configured by the READBACK bit in the Interface Configuration 1 register. Read from XDAC Active registers is synchronized with a DAC_IN update command.

Since REFDAC1_DATA and REFDAC2_DATA are stored in the EEPROM, their values are automatically loaded to the operating memory at power up.

Refer to Figure 27 for a high-level block diagram of the DAC and XDAC Data register.

5.3.1.3. DAC Output Range and Clamp Configuration

The output range and clamp voltage value can be independently set for each DAC group. After power-on or a reset event, the DAC outputs are directed automatically to the corresponding clamp value (see Table 9). The auto-range detector sets the DAC group's output ranges, and all DAC data registers and data latches are set to their default values.

The DAC output ranges can also be manually configured by writing to DAC_RANGE [2:0] bits as shown in Table 9. Typical power supply configurations are listed in Table 10 and Table 11.

Table 9. DAC Output Range Selection

DAC_RANGE [2:0] (Page: 0x01, Addr: 0x6C)	DAC Output Voltage Range
0xx	Range set by auto-range detection circuit (default)
100	-10 to 0V
111	0 to 5V

Table 10. All-Positive DAC Range Mode Typical Configuration

Pin	Typical Connection
IOVDD	1.8V
AVDD	5V
AVCC	5V
AVSS	AGND
Thermal Pad	AGND

Table 11. All-Negative DAC Range Mode Typical Configuration

Pin	Typical Connection
IOVDD	1.8V
AVDD	5V
AVCC	0V
AVSS	-12V
Thermal Pad	AGND

5.3.1.4. Auto-Range Detection

After the power-on or reset event, the voltage present on the corresponding A_{VSS} pin determines the output range for each DAC group.

The output DAC group is configured to -10 to 0V when A_{VSS} voltage is lower than the threshold value AV_{SSTH}. The output DAC group is configured to 0 to 5V range when A_{VSS} voltage is higher than the threshold value AV_{SSTH}. The results of the auto-range detector are stored in the general status register address 0x40.

The auto-range detector is also enabled by a register write to the DAC power-down registers, 0x68 or the device configuration register, 0x06.

Although the auto-range detector determines each DAC group's initial output range setting, the output range can be modified afterward by writing to the DAC range register, 0x6C.

Similar to the A_{VSS} pin, the auto-range detector results for the positive analog supply A_{VCC} are captured in the General Status 1 Register. When the A_{VCC} voltage of a DAC group is lower than the threshold value, A_{VCCTH}, the signal goes LOW and the associated bit is set to 0. Conversely, if the DAC group A_{VCC} voltage is higher than v, the signal goes HIGH and the associated bit is set to 1.

The full-scale output range for each DAC group is limited by the corresponding A_{VCC} and A_{VSS} values. The maximum and minimum outputs cannot exceed the A_{VCC} voltage or be lower than the A_{VSS} voltage.

Table 12. Recommended DAC Group Configuration

DAC Group	DAC	AUTO-Range and Clamp Voltage Selection (AV_{SS})	Positive Output Range	Clamp Voltage Connection	Negative Output Range	Clamp Voltage Connection
1	DAC0	AVSS	0 to 5 V	AGND	-10 to 0 V	AVSS
	DAC1					
	REFDAC1					
	OUT-1	REFDAC1	0 to 5 V	REFDAC1	-10 to 0 V	REFDAC1
2	DAC2	AVSS	0 to 5 V	AGND	-10 to 0 V	AVSS
	DAC3					
	REFDAC2					
	OUT-2	REFDAC2	0 to 5 V	REFDAC2	-10 to 0 V	REFDAC2

5.3.1.5. DAC Clear Operation

Each DAC can be set to a CLEAR state using either hardware or software. When a DAC goes to CLEAR state, it is loaded with a zero-code input and the output voltage is set according to the auto-range detector output range.

The DAC Buffer or Active registers do not change when the DACs enter the CLEAR state which makes it possible to return to the same voltage output before the clear event was issued. Even though the contents of the DAC Active register do not change while a DAC is in CLEAR state, a data-register read operation from the DAC Active registers while in this state returns zero-code. This functionality enables the ability to determine the DAC output voltage regardless of the operating state (CLEAR or NORMAL).

Note that the DAC Buffer and Active registers can be updated while the DACs are in CLEAR state allowing the DACs to output new values upon return to normal operation. When the DACs exit the CLEAR state they are immediately loaded with the data in the DAC Active registers and the output is set back to the corresponding level to restore operation.

The DAC Clear registers enable independent control of each DAC CLEAR state through software.

The device has the capability to force the DACs into the CLEAR state as a response to an alarm event. To enable this function, the alarm events must first be enabled as DAC-clear alarm sources in the DAC Clear Source registers. The DAC outputs to be cleared by the selected alarm events must also be specified in the DAC Clear Enable registers.

When an alarm event is triggered, the corresponding alarm bit in the Alarm Status register is set and all the DACs set to clear in response to this alarm event in the DAC Clear Enable registers enter a CLEAR state. Once the alarm bit is cleared, and as long as no other CLEAR state controlling alarm events have been triggered, the DACs get reloaded with the contents of the DAC Active registers and the outputs update accordingly.

When DAC low clamping protection is enabled, setting the DAC-clear enable or the CLEAR state of a DAC will automatically set the clear enable or the CLEAR state of the correspondent XDAC.

5.3.2. DEVICE_READY Signal

The F39510 supports the generation of a DEVICE_READY signal. The DEVICE_READY pin is asserted if the output of all the enabled DACs and XDACs is settled when the timer wait time has elapsed. DAC output voltage is converted through the ADC and compared with the DAC code to determine if the DAC output voltage is settled. At the end of the timer wait time, if all DAC output voltages are settled, DEVICE_READY is set HIGH.

The timer wait time from when the first DAC is enabled to when the host can turn on the power amplifier is programmable in the DEVICE_READY Configuration Register (Address: 0xF4).

The DAC output voltage is measured via the bipolar internal ADC channels and then compared with the expected ADC Code. If the delta between the converted DAC output voltage and expected ADC Code is within the error limit of +/-m LSB defined in the ADCINT_n_ERR_LIMIT registers stored in the EEPROM then the DEVICE_READY pin is asserted HIGH.

All alarms can be set to deactivate the DEVICE_READY pin: the DEVICE_READY pin will be re-asserted when the alarm event is cleared and timer wait time elapses. The DEVICE_READY pin works as an interrupt to the host so that it can query the Alarm Status registers to determine the alarm source. Any alarm event can deactivate the pin as long as the alarm is not masked in the DAC Clear Source registers (address 0x1A through 0x1B). When an alarm event is masked, the occurrence of the event sets the corresponding status bit in the Alarm Status registers but does not deactivate the DEVICE_READY pin.

The DEVICE_READY signal is de-asserted when all DACs are disabled or if any AVDD_OK AVCC_OK IOVDD OK signal goes low.

The DEVICE_READY signal can be forced into an active state (driven high) by setting the ASSERT bit to 1’3 in the DEVICE_READY Configuration Register. The DEVICE_READY signal can be forced into an inactive state (driven low) by setting the DEASSERT bit to 1’3 in the DEVICE_READY Configuration Register.

5.3.3. DAC Enable Sequence

After power-up (power_sup_ok = 1) in autonomous mode (LUT_EN = 1) the enable signals EN_DAC_BA[7:0] of the DAC’s enabled in the PD_DAC Register are set in the following manner:

REFDAC1 →REFDAC2 →DAC_0→DAC_1 →DAC_2→DAC_3.

The delay time Tdac_en between two consecutive DAC enables is programmable by the AUTO_CFG.TIM_DAC_EN bits with the following values: 1ms/2ms/4ms/6ms. The time TDEVICE_READY for the assertion of the DEVICE_READY signal depends on the number of enabled DACs and it will be greater than the total DACs enable time of the sequence; TDEVICE_READY can be estimated with the following formula:

TDEVICE_READY (ms) = (#EN_DAC + 2 * #EN_XDAC - 1) * Tdac_en + 7

> where 6ms are estimated for the phase of the ADC monitoring of DAC output settling (ADC average = 16): refer to ADC Input Conditioning for a more accurate estimation of the ADC monitoring phase. The programmed timer wait time Ttimer must be greater than the estimated TDEVICE_READY time.

After power-up (power_sup_ok = 1) if autonomous mode is not enabled (LUT_EN = 0) the enable signals are set without delays.

5.3.4. Output Switch On and Off Control

The F39510 facilitates rapid turn-on and shutdown of the downstream devices through the OUT-1 and OUT-2 outputs. The Enable 1 and Enable 2 input can switch ON and OFF these outputs independent of the I3C/I^{2}C and SPI bus transactions. When Enable 1/2 input pin is asserted HIGH, then the corresponding OUT 1/2 is driven by the DAC. When Enable 1/2 input pin is asserted LOW, the OUT-1 or OUT-2 pin is driven by REFDAC1 or REFDAC2.

The control and switch design is optimized for the minimum delay between the Enable 1/2 input and the OUT-1/2 switching. The design also ensures that during the state transition, there exists an instance when both switches

at OUT-1/2 are open; that is, there is no possibility for the crowbar current to flow from the Buffer output to AVSS.

The switches are designed to default to the state where OUT-1/2 output is connected to REFDAC1/REFDAC2 at power-up, as long as Enable 1/2 input is programmed to logic 0.

If the DAC_SW_EN register (Addr: 0x0163) is used to toggle the DAC output switches, then the ENABLE_CFG register must be set to all zeroes (Addr: 0x0164). In this case, the ENABLE 1 and 2 pins will not be used. Similarly, if the Enable 1 and Enable 2 pins are being used to control the DAC output switches using the ENABLE_CFG register (Addr: 0x0164), then the DAC_SW_EN register (Addr: 0x0163) must be set to all zeroes (the last 4 bits). Only one of these registers can be used at a given time to control the DAC output switches and never both simultaneously.

5.4 Look-Up-Table (LUT) and Arithmetic-Logic Unit (ALU)

The Look-Up Table (LUT) is used to create an arbitrary transfer function that maps the temperature to the analog output of the device. The LUT is indexed in 4°C increments to minimize the storage requirements. Also, the stored values are only the increments or first derivatives (Δs) of the modeled transfer function. The internal Arithmetic-Logic-Unit reconstructs the original transfer function by integrating the coefficients (values) stored in the LUT. The errors due to the coarseness of the temperature quantization are significantly reduced using linear interpolation, which is also implemented in the Arithmetic-Logic-Unit.

Consider the example shown in Figure 30. The target output vs. temperature is shown in the top graph. V_{DACx} is a smooth, monotonic function with, ideally, infinite precision. The LUT stores only the increments, or the rise, within each 4°C intervals.

The series of increments must be summed together and added to the constant BASE value to recreate the original transfer function. The BASE represents the constant offset which is lost due to the differentiation - storage of the increments only. This process must also be referenced to the common temperature point. This reference temperature is called BASELINE in this document and is fixed at 24°C.

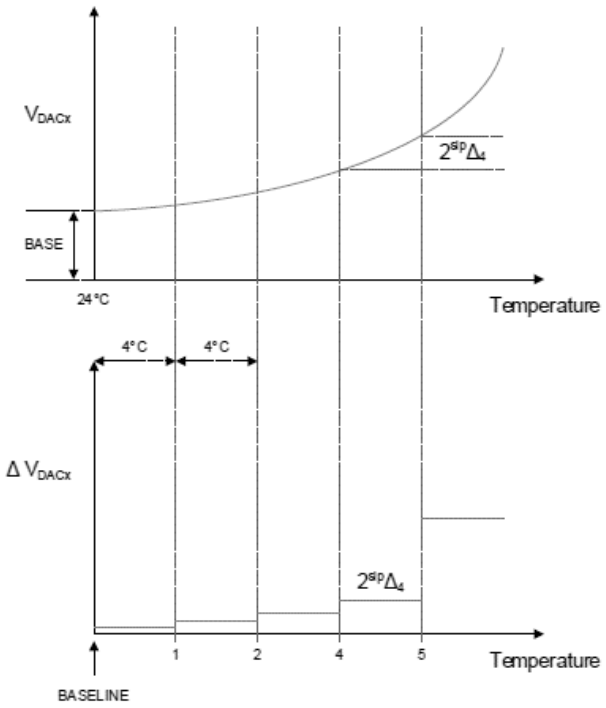


Figure 30. Original Transfer Function

Table 13. Look-Up-Table Organization

	Look-Up-Table		Register	
Temperature	**Index**	**Value**	**Name**	**Value [2]**
148°C	+31	Δ_{31}	DEL48	DEL(48)
144°C	+30	Δ_{30}	DEL47	DEL(47)
	K+1	Δ_{K+1}		
	K	Δ_{K}		
36°C	+3	Δ_{3}	DEL20	DEL(20)
32°C	+2	Δ_{2}	DEL19	DEL(19)
28°C	+1	Δ_{1}	DEL18	DEL(18)
24°C	BASELINE	BASE	DAC_n_BASE_[L/H]	BASE
20°C	-1	Δ_{-1}	DEL17	DEL(17)
	-(M-1)	$\Delta_{-(M-1)}$		
	-M	Δ_{-M}		
-44°C	-17	Δ_{-17}	DEL1	DEL(1)
-48°C	-18	Δ_{-18}	DEL0	DEL(0)

The increments stored in the LUT are 4-bit unsigned values. This limits the maximum slope of the transfer function stored in the LUT to:

$$SLOPE_{MAX} = 2^{\mathrm{slp}} \frac{16LSB}{4°C} = 2^{\mathrm{slp}} \frac{4\ LSB}{°C},\ \mathrm{slp} = 0,1,2,3$$

Where slp is the slope factor that can be configured for each DAC in the DAC_n_DEL48 register.

Given this slope limit imposed by the LUT structure, and the fact that the LUT input range is 196°C (from -48°C to 148°C), the maximum output range of the LUT due to the temperature sensor input is $(784*2^{slp})$ LSBs, for the given BASE value.

5.4.1. DAC Input Calculation

When the temperature is above 24°C, all increments (Δs) of the modelled transfer function are added to the BASE value to produce numeric equivalent of the analog output. When the temperature is below 24°C, all increments (Δs) are subtracted from the BASE value to produce the input data to the DACs.

Interpolation function is implemented in the ALU that follows the Look-Up-Table. The truncated lower bits of the temperature value, REM = TEMP[3:0], are used to interpolate between data points stored in the LUT. A portion of increment, αΔi, is added to from the final numeric input data to the DAC. The factor α is a fraction of 4°C temperature span, or equivalently it is a fraction of the 16-code temperature span.

$$\alpha = \frac{REM}{16}$$

A scaling factor 2^{slp} for the stored increments can be selected for each DAC to increase the maximum supported increment (Δs) of the modelled transfer function.

The process of calculating DACIN, including the interpolation, for a monotonically increasing transfer function is depicted in Figure 31. The DACIN is the final 13-bit value produced by the ALU, and forwarded to the DAC for conversion in the analog domain.

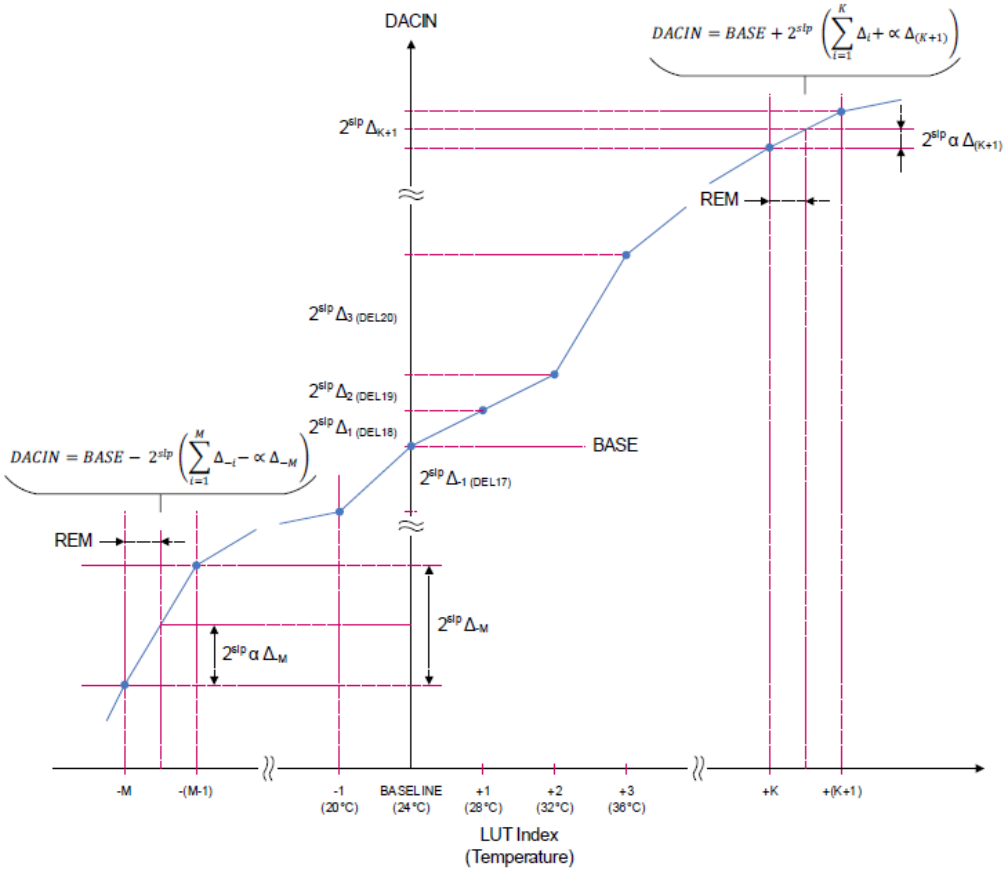


Figure 31. ALU DAC Input Data Calculation Monotonically Increasing Transfer Function

The device can also produce monotonically decreasing transfer function by setting the polarity bit DAC_n_POL in the DAC_n_BASE_H.POL register (n = 0, 1, 3, 2).

The effect of polarity reversal (POL = 1) on the overall transfer function is shown in Figure 32. The LUT content is unchanged from the original example above. Note that now the LUT values stored at locations above BASELINE address are subtracted from BASE value, and the LUT values stored at locations below BASELINE address are added to the BASE value.

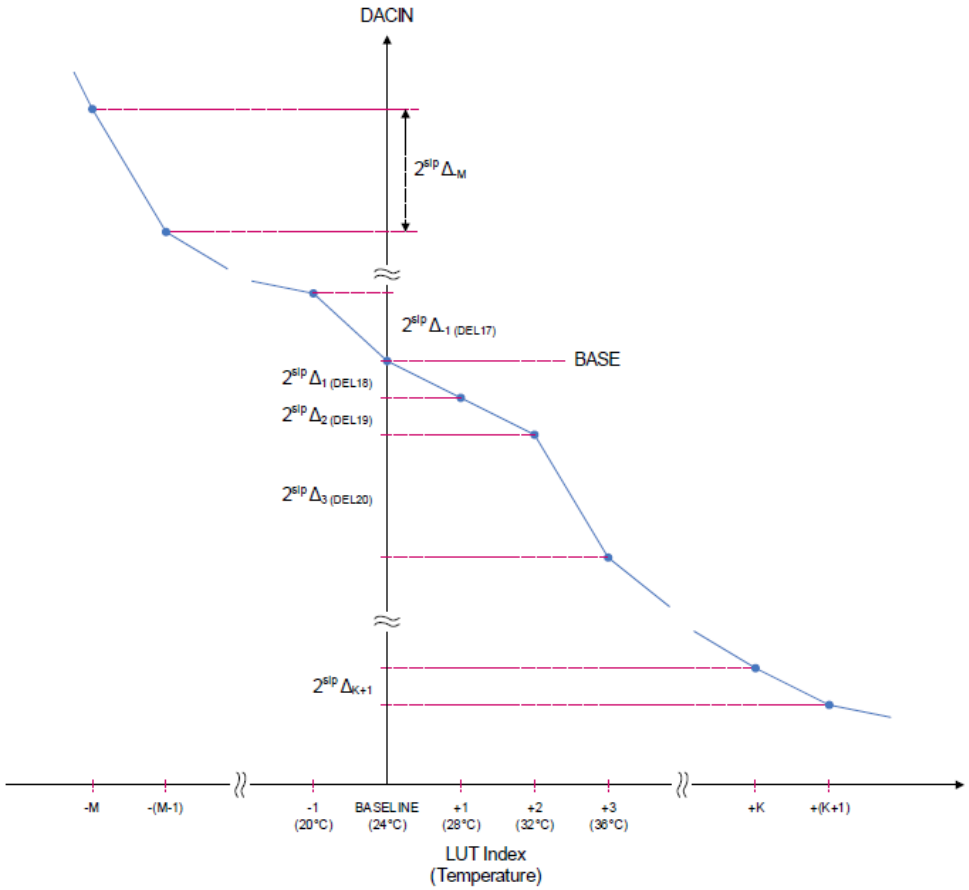


Figure 32. ALU DAC Input Data Calculation for Monotonically Decreasing Transfer Function

The expressions used in the calculation of the transfer function are summarized below:

LUT index = BASELINE:

$$\text{DACIN} = \text{BASE}$$

LUT index > BASELINE:

$$\text{DACIN} = \text{BASE} + (-1)^{POL} 2^{slp} \left(\sum_{i=1}^{K} \Delta_i + \alpha\Delta_{(K+1)} \right)$$

LUT index < BASELINE:

$$\text{DACIN} = \text{BASE} - (-1)^{POL} 2^{slp} \left(\sum_{i=1}^{M} \Delta_{-i} - \alpha\Delta_{-M} \right)$$

5.4.2. LUT Input and Output Ranges:

The programmable LUT input range spans temperatures -48°C to 148°C. For the temperatures below -48°C the LUT output is linearly extrapolated; that is, the increment Δ_{-18} (register DEL0) stored at the location corresponding to -48°C is used as the slope below -48°C. For the temperatures above 148°C the LUT output is linearly extrapolated; that is, the increment Δ_{31} (register DEL48) stored at the location corresponding to 148°C is used as the slope above 148°C.This is shown in (see Figure 33).

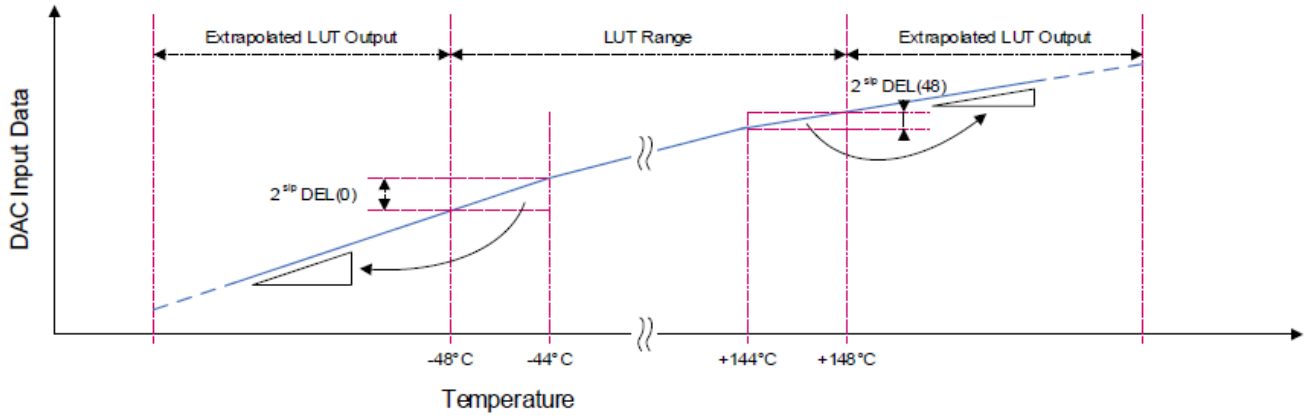


Figure 33. ALU DAC Input Data Below -28°C

5.4.3. DAC Input Override Mode

The DAC input data can be overridden by externally supplied data. The DAC Input Override Mode is facilitated in the ALU. In this mode the F39510 is a six user's programmable 13-bit DACs device. The multiplexer control signal is the DAC_n_OC bit (n = 0, 1, 2, 3) of the OVRD_CTL register.

5.4.4. ALU Bypass Mode

The F39510 can produce a predetermined constant output level as soon as it is powered up by bypassing the ALU. The ALU bypass mode is enabled by setting the DAC_n_BASE_H.BYP bit (n = 0, 1, 2, 3). Since DAC_n_BASE_H.BYP is stored in the EEPROM Controller, its value is automatically loaded into the DAC Controller at power up. If the stored value for DAC_n_BASE_H.BYP is 1, upon power up the corresponding DAC output immediately produces an analog output equivalent to the BASE value.

5.4.5. Temperature Sensor Override Mode

The Local Temperature Sensor Output Data can be overridden by externally supplied data.

This functionality is facilitated in the ALU by the multiplexer that precedes the DAC Input Calculation. The multiplexer control signal is the OVRD_CTRL.TEMP_OC bit, which is connected to the TEMP_OVRD_CNTL input pin.

Data written to the TEMP_OVRD Data registers is initially stored in the TEMP_OVRD Buffer registers. The transfer of data from the TEMP_OVRD Buffer registers to the TEMP_OVRD Active registers is initiated by a TEMP_UPDATE command in the Register Update register. When the TEMP_OVRD Active registers are updated, the TEMP_OVRD outputs change to the new values.

The host has the option to read from either the TEMP_OVRD Buffer registers or the TEMP_OVRD Active registers when accessing the TEMP_OVRD Data registers. The TEMP_OVRD read back option is configured by the READBACK bit in the Interface Configuration 1 register. Read from TEMP_OVRD Active registers is synchronized with a DAC_IN update command.

5.5 ADC

The F39510 uses a single 12 bit SAR ADC, 3 channel select multiplexer, and on-chip sample and hold circuitry. The F39510 has an internal analog temperature sensor.

The ADC in F39510 operates from an internal 2.5V reference voltage and has an input range from 0V to 2* V_{ref}. A 26MHz on-chip clock derives the ADC timing signals. The user can access the conversion results through the device serial interface.

Driving each analog input pin with a low impedance source is recommended to achieve specified performance, especially at higher input frequencies.

5.5.1. Internal Bipolar Analog Output Data

The F39510 can support up to 10 internal bipolar analog inputs. The analog input range for these channels is -12.5 to 12.5V. The bipolar signal is scaled internally through a resistor divider so that it maps to the native input range of the ADC (0V to 2 × Vref).

The bipolar analog input conversion values are stored in straight binary format in the ADC Data registers (address 0x20 through 0x2B). The LSB (least-significant bit) size for these channels is 10 × Vref / 4096. With the ADC reference voltage equal to 2.5V, the input voltage is calculated by:

$$Voltage = 5\,\mathrm{x}\left(\frac{'\ Digital\ Code'\ \ x\ 5}{4096} - 2.5\right)$$

Refer to Table 14 for some correlation between the analog input for these channels and the output value of the ADC data registers.

Table 14. ADC Bipolar Analog Output Data

Analog Input (V)	Digital Code
-12.5	0000 0000 0000
-9.9976	0001 1001 1010
-7.5012	0011 0011 0011
-4.9988	0100 1100 1101
-2.5024	0110 0110 0110
-0.0061	0111 1111 1111
0	1000 0000 0000
0.0061	1000 0000 0001
2.5024	1001 1001 1010
4.9988	1011 0011 0011
7.5012	1100 1100 1101
9.9915	1110 0110 0101
12.4939	1111 1111 1111

5.5.2. ADC Sequencing

The F39510 supports direct mode (default conversion method), auto mode and autonomous mode conversion. The conversion method can be selected through register 0x62 (ADC configuration register) and requires the ADC to be first configured using register address 0x0A (LUT CFG configuration register), register address 0x60 (DAC Monitor Configuration register) and register address 0x13 (ADC MUX FETDRV Monitor Configuration Register). The input channels to the ADC include the Local Temperature Sensor, the Remote Temperature Diode Driver and ten internal bipolar channels.

Direct mode conversion allows users to convert a single channel or sequence of channels on-demand by issuing an ADC trigger signal. After the last enabled channel is converted and the iterations for averaging are completed, the ADC enters IDLE state and waits for a new trigger.

Auto mode conversion allows users to convert selected ADC input channels continuously. Upon completion of the average iterations of the first sequence, another sequence automatically starts. The ADC trigger initiates the auto mode conversion. Issuing a second ADC trigger stops the auto mode conversion.

In autonomous mode, the selected ADC input channels are converted continuously without intervention from the system controller. When the power is applied the conversion cycle is initiated automatically: upon completion of the average iterations of the first conversion sequence another sequence is automatically started. Conversion of the selected channels occurs repeatedly until the autonomous conversion is stopped by clearing the LUT_EN bit in AUTO_CFG register.

The F39510 enables digital averaging of the channels measurements to improve their accuracy at the cost of a longer update time. The digital average is enabled by the ADC_AVG[2:0] bits in the ADC Average Count Register: averaging length can be set to 1, 2, 4, 8, 16, 32, 64, or 128. The number of average iterations is the same for all channels, and the average is performed running a complete conversion sequence of the selected channels at each average iteration.

Regardless of the selected conversion method, the following registers should only be updated while the ADC is in IDLE state:

- False Alarm Configuration Register
- ADC Average Count Register
- False Alarm Configuration register
- ADC MUX Configuration registers
- Threshold registers
- Hysteresis registers

After updating any of the registers listed above, a minimum wait time of 65 ADC clock (adc_clk) cycles should be implemented before issuing an ADC trigger. Figure 34 shows the ADC conversion sequence.

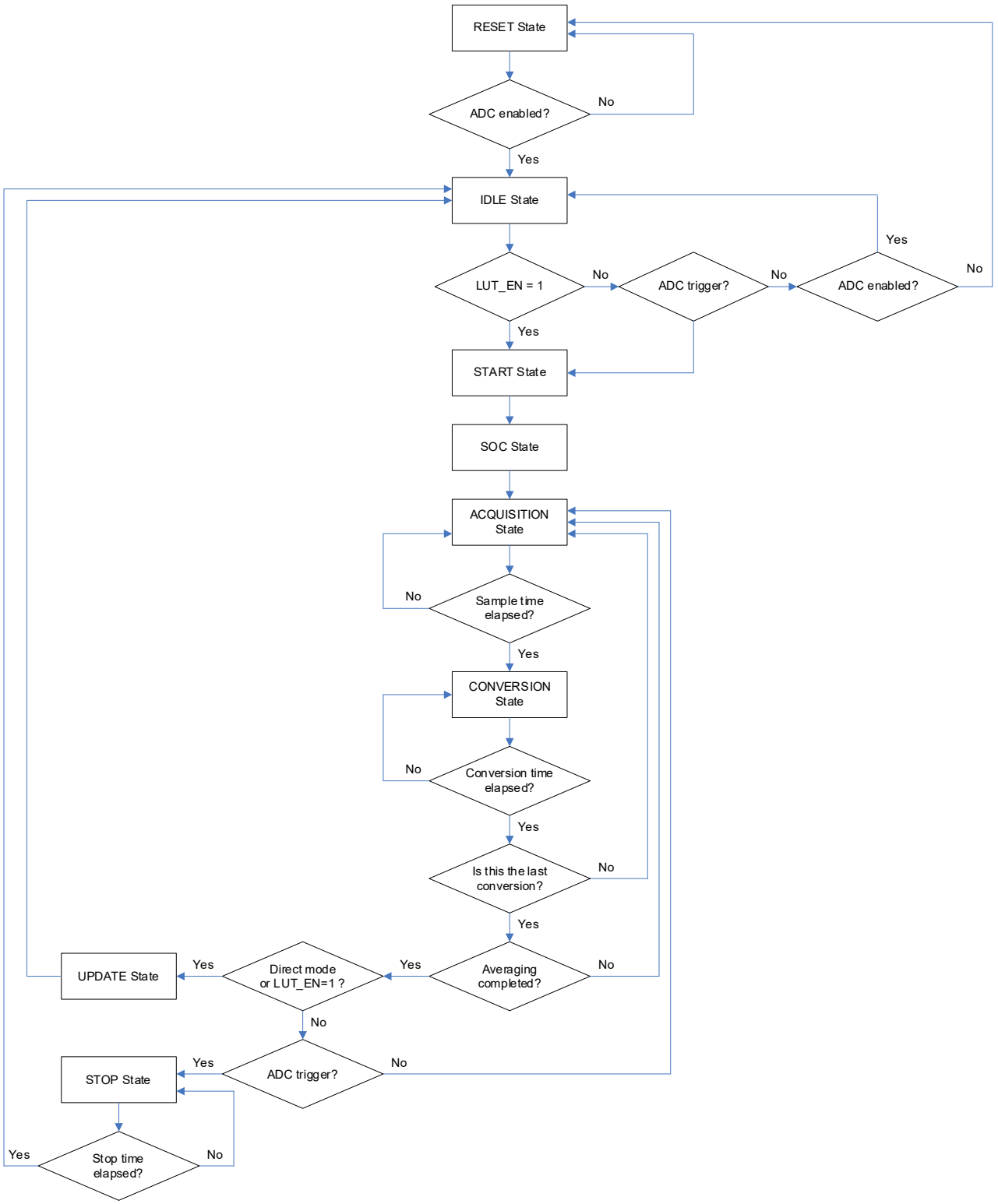


Figure 34. ADC Controller Conversion Sequence

5.5.3. ADC Synchronization

In direct-mode and automode, a trigger signal must occur for the ADC to enter and exit the IDLE state. The ADC trigger can be generated through software (ICONV bit in the ADC Trigger Register 0x5F). In Autonomous mode, at power-on the ADC does not require a trigger to exit IDLE state and start conversion; ADC enters IDLE state when Autonomous mode is disabled (LUT_EN = 0).

In auto mode, the Analog Input, and Temperature registers are accessed by first issuing an ADC UPDATE command in the Register Update register. The ADC UPDATE command ensures the latest available data for each input channel can be accessed without the need for complex synchronization schemes between the F39510 and the host controller. A single ADC UPDATE command updates all ADC and Temperature Data registers. Therefore, issuing multiple UPDATE commands is not necessary when reading more than one ADC Data register.

The ADC UPDATE command and accessing of the ADC and Temperature Data registers do not interfere with the conversion process, ensuring continuous ADC operation.

In direct mode, the Analog Input, and Temperature registers should only be accessed while the ADC is in the IDLE state (see Figure 35). Although the total update time can be easily calculated, the device provides a data-available indicator signal to track the ADC status. Failure to satisfy the synchronization requirements could lead to erroneous data reads.

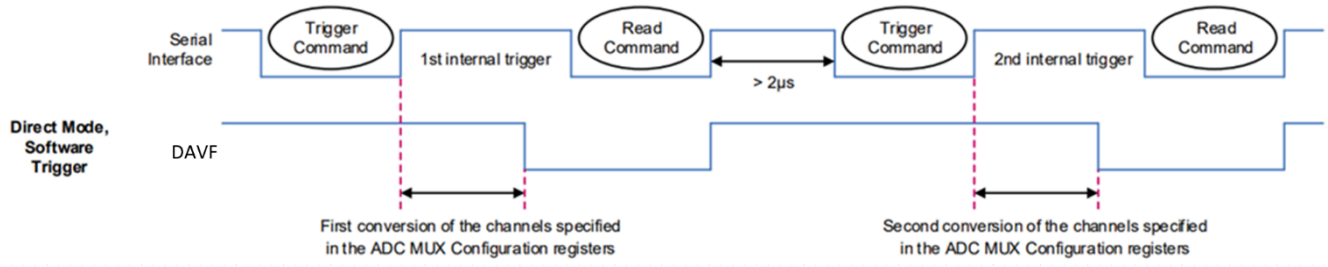


Figure 35. ADC Direct-Mode Trigger Synchronization: Software Trigger

The data-available indicator signal is output as a data-available flag that is accessible through the Serial Interface (DAVF bit in the General Status Register). After a direct-mode conversion is complete and the ADC returns to the IDLE state, the DAVF bit is immediately set to 1. The flag is cleared automatically when a new conversion begins or one of the ADC Data or Temperature Data registers is accessed.

In autonomous mode, then selected temperature sensor continuously updates reading with an update time that depends on the selected ADC channels and can be calculated using Table 15. For internal synchronization with ALU, the adc-done pulse, generated in the UPDATE state of the fsm, is used: each temperature sensor update triggers the ALU to re-calculate its output using the user defined coefficients stored in the LUT. The ALU output is passed on to the DACs and DAC output is updated: all functionality described here occurs automatically, without intervention from the system controller.

The DAC input calculated by the ALU can be read from registers DAC_x_OVRD (Readback from active registers) by first issuing a DAC_IN UPDATE command in the Register Update register.

5.5.4. ADC Conversion Rate and Update Time

The sampling frequency of the ADC is dynamic and dependent on the acquisition and conversion time of each channel. Table 15 provides the relationship between the total update time, ADC conversion rate, acquisition clocks, and conversion clocks for internal bipolar, and internal temperature sensor ADC input channels.

Table 15. ADC Conversion Rate and Total Clock Cycles

Conversion Rate [1]	Input Channel	Select Clocks		Acquisition Clocks		Conversion Clocks [3]		Number of Clocks		Update Time [µs] [2]
		adc_clk	osc_clk	adc_clk	osc_clk	adc_clk	osc_clk	adc_clk	osc_clk	
00	Unipolar Analog	1	4	30.5	122	14.5	58	46	184	7.0656
	Internal Bipolar	1	4	122.5	490	14.5	58	138	552	21.1968
	Local Temperature	1	4	1009.5	4038	14.5	58	1025	4100	157.44
	Remote Temperature [4]	1	4	1609.5	6438	14.5	58	1625	6500	250
01	Unipolar Analog	1	4	76.5	306	14.5	58	92	368	14.1312
	Internal Bipolar	1	4	122.5	490	14.5	58	138	552	21.1968
	Local Temperature	1	4	1009.5	4038	14.5	58	1025	4100	157.44
	Remote Temperature [4]	1	4	3234.5	12938	14.5	58	3250	13000	500
10	Unipolar Analog	1	4	122.5	490	14.5	58	138	552	21.1968
	Internal Bipolar	1	4	122.5	490	14.5	58	138	552	21.1968
	Local Temperature	1	4	1009.5	4038	14.5	58	1025	4100	157.44
	Remote Temperature [4]	1	4	6484.5	25938	14.5	58	6500	26000	1000
11	Unipolar Analog	1	4	260.5	1042	14.5	58	276	1104	42.3936
	Internal Bipolar	1	4	260.5	1042	14.5	58	276	1104	42.3936
	Local Temperature	1	4	1009.5	4038	14.5	58	1025	4100	157.44
	Remote Temperature [4]	1	4	12984.5	51938	14.5	58	13000	52000	2000

1. See the ADC conversion rate bit fields in the ADC Configuration Register to configure this setting for the Internal Bipolar Analog Inputs and the Local Temperature Sensor (ADC_CFG.ADC_CONV_RATE) as well as for the Remote Temperature Diode Driver (ADC_CFG.RT_CONV_RATE).
2. Based on a typical Oscillator frequency of 26MHz.
3. The number of Conversion clocks cycles can be extended from 58 to 70 in step of 4 with ADC_CAL_CNTL.ADC_SAMPLE_DLY[1:0] bits: for each conversion, the update time increases by n*0,0384µs, where n is the number of additional clock cycles.
4. Listed timing values are for a single ADC measurement: RT sensor is a differential measurement, so it requires 2 measurements.

The user can use Table 15 with the minimum and maximum oscillator frequency and the following equation to calculate the total ADC update time range.

$$T_S = \#AVG \times \frac{(Bclk \times \#Bch + Uclk * \#Uch + LTclk * \#LTch + 2 * RTclk * \#RTch)}{F_{osc}}$$

where:

- Ts is the total update time
- #AVG is the number of averaging cycles, either 128, 64, 32, 16, 8, 4, 2 or 1
- Bclk is the total number of bipolar clock cycles
- #Bch is the number of active Internal Bipolar Channels, either 10, 9, 8, 7, 6, 5, 4, 3, 2, 1 or 0
- Uclk is the total number of Unipolar Channels clock cycles.
- #Uch is the number of active Unipolar Channels inputs, either 2, 1 or 0.
- LTclk is the total number of Local Temperature Sensor clock cycles
- #LTch the number of active Local Temperature Sensor channels; either 1 or 0
- 2*RTclk is the total number of Remote Temperature Diode Driver clock cycles
- #RTch the number of active Remote Temperature Diode Driver channels; either 1 or 0
- fosc is the Oscillator frequency

The following is an example of a complete calculation of the total update time range. In this example, the ADC conversion rate is set to 2'b00 (ADC_CFG.ADC_CONV_RATE) and the number of averaging cycles is set to 3'b100 (ADC_AVG.ADC_AVG_ADC) and the following ADC input channels are used:

- Internal Bipolar channels: ADCINT_DAC[3:0], ADCINT_REFDAC_[2:1] (6 active channels)
- Unipolar channels: TEMP+/TEMP- (1 active unipolar channels)
- Local Temperature Sensor: Yes (1 active temperature channel)
- Remote Temperature Diode Driver: No (no active remote temperature channel)

Table 15 provides the total number of clocks required for each ADC input under the example conditions.

For the minimum specified oscillator frequency of 22.5MHz, the ADC conversion rates set to 2'b00 (ADC_CFG.ADC_CONV_RATE), respectively, use the following equation to calculate the total maximum update time for this example.

$$T_{SMAX} = 16 \times \frac{(552 * 6 + 184 * 1 + 2 * 4100 * 1)}{22.5\text{MHz}} = 8317.2\ \mu s$$

For the maximum specified oscillator frequency of 27.5MHz the minimum update time for this example is:

$$T_{SMIN} = 16 \times \frac{(552 * 6 + 184 * 1 * 4100 * 1)}{27.5\text{MHz}} = 6805\ \mu s$$

During the conversion, the input current per channel varies with the total update time which is determined by the number and type of channels and the conversion rate setting in the ADC Configuration Register.

5.6 Alarms

5.6.1. Programmable Out-of-Range Alarms

Refer to sections 8.23 to 8.26 for details regarding the programmable out of range alarms in the F39510.

5.6.2. False-Alarm Protection

The false alarm configuration register (address 0x6E) determines the number of consecutive samples N (alarm factor) before an alarm event is issued. The alarm event is not issued if the monitored alarm signal returns to the normal range before N consecutive conversions. Only when this condition is violated, an alarm event is registered.

5.6.3. Alarm Latch Disable

The Alarm Latch Disable bit in the ALR_CFG_2 register (address 0x16) sets the latching behavior for all alarms. When the ALARM_LATCH_DIS bit is cleared to 0 the alarm bits in the Alarm Status registers are latched. The alarm bits are referred to as being latched because they remain set until cleared by software. This design ensures that out-of-limit events cannot be missed if the software is polling the device periodically. All bits are cleared when reading the Alarm Status registers, and all bits are reasserted if the out-of limit condition still exists on the next monitoring cycle.

When the ALARM_LATCH_DIS bit is set to 1, the alarm bits are not latched. The alarm bits in the Alarm Status registers are set to 0 when the error condition subsides, regardless of whether the bit is cleared or not. I3C alarm error bits (s0s1_err_alr, par_err_alr) and ADC data available bit (dav_alr) are always latched.

5.6.4. GALR Alarm

When any of the monitored inputs is out of the specified range, an alarm event is registered and the global alarm bit, GALR in the General Status Register, is set. Use the Alarm Status registers to determine the source and reason of the alarm event.

TBD.

Figure 36. Global Alarm Generation

5.7 Hysteresis

The Hysteresis registers (address 0x7A through 0x7B) store the hysteresis value for the Internal Bipolar Monitoring channels, Local Temperature Sensor, and Remote Temperature Sensor programmable alarms. The hysteresis is a programmable value between 0°C to 31°C for temperature sensor alarms. The die thermal alarm hysteresis is fixed at 8°C. Figure 20 shows how the alarm condition is cleared when the conversion result returns a value below the high threshold or above the low threshold by the number of codes specified in the hysteresis settings.

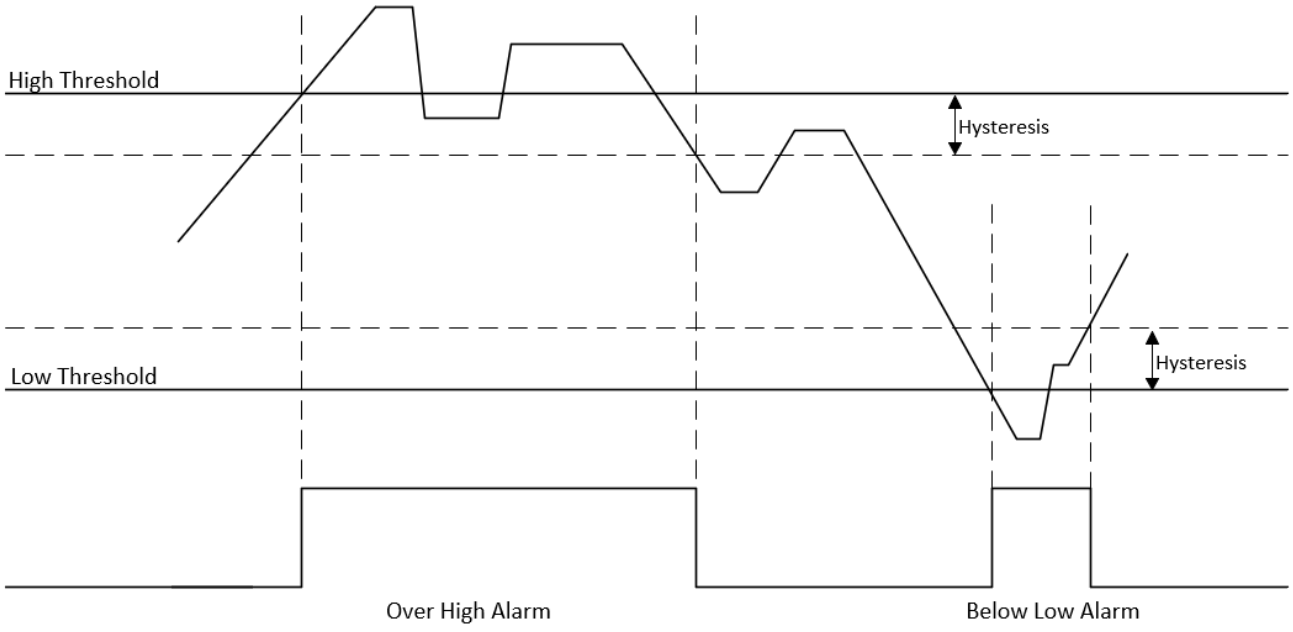


Figure 37. Device Hysteresis

6. EEPROM

The memory of the EEPROM Controller consists of 2 distinct areas: the register area (operating memory) and the EEPROM (non-volatile memory).

The registers provide control over the EEPROM and store the trimming data of almost all components in the Analog Subsystem and User data, including Look-up-table and autonomous mode configuration data. All register locations are directly accessible via the Serial Interface.

The EEPROM is not directly accessible via the Serial Interface. It acquires its data via the transfer from the EEPROM Controller, upon user issued command.

The EEPROM Controller offers integrated Error Correction Code (ECC) functionality to increase reliability against soft errors from random noise. For each 64 bits of data, 8 check (or protection) bits are generated and used for Single Error Correction and Double Error Detection (SEC-DED).

6.1 User Data Storage

The User data for the Look-Up-Tables (100 bytes), Autonomous mode configuration (18 bytes) and the NotePad (9 bytes) are stored in the EEPROM Controller spanning addresses 0x80 through 0xFF. This space is directly accessible (READ and WRITE) via the Serial Interface.

There is an option to store the User Data in the non-volatile memory, EEPROM. This is shown in Figure 50. The move of data from the EEPROM Controller to EEPROM (BURN) is initiated by writing a command byte to the LUT EEPROM Control register

The EEPROM Controller supports in total 128 registers to store the User data.

Upon power up the device automatically copies the User data of the EEPROM to the EEPROM Controller (TRANSFER), after the transfer of the Trimming data. The user can also issue a command via the Serial Interface by writing a command byte to the LUT_E2P_CNTL register to force the transfer of data from the EEPROM to the EEPROM Controller. This is shown in Table 16.

Table 16. EEPROM Controller to EEPROM Transfer Control (user data)

Operation	Address	Data	EEPROM Controller Operation	Description
WRITE	0x0A	0x5E	TRANSFER	Transfer of User data from EEPROM to EEPROM Controller.
WRITE	0x0A	0xE5	BURN	Transfer of User data from EEPROM Controller to EEPROM.

The User data that are read from the EEPROM are not applied at once, but sequentially.

The READ of the LUT EEPROM Control register returns the status of the data transfer. This is shown in Table 17.

Table 17. EEPROM Controller to EEPROM Transfer Status (user data)

Operation	Address	Bit Field	Description
READ	0x0A	RDYB	0 = The TRANSFER or BURN has completed 1 = The TRANSFER or BURN is in progress.
		COR	1 = A bit error was detected during the transfer of user data from EEPROM to EEPROM Controller. The error has been corrected and the data is valid.
		UCOR	1 = A bit error was detected during the transfer of user data from EEPROM to EEPROM Controller. The error was not corrected and data is compromised.

Note that the UCOR and COR bits are updated only by the TRANSFER command and report error information for the user data.

6.2 NotePad Data

20 bytes of memory for arbitrary data storage in Page 15 (0x0F). This data does not affect the operation of the device. This data is transferred to the EEPROM when BURN command sequence is issued. Upon power up the device automatically copies the data of the EEPROM to the EEPROM Controller (TRANSFER).

7. Programming

7.1 SPI Interface Programming

The F39510 provides a four-wire SPI interface that offers all registers read and write (R/W) access. To configure the device in SPI operation the SDA pin needs to be set to 0V (grounded). The SPI interface access cycle is (N + 2) bytes long, where N is the number of data bytes. Asserting the CSB pin low initiates a frame and de-asserting the CSB pin high ends the frame. In MSB-first mode, the first bit transferred is the R/W bit followed by 7 or 15 register address bits (1-Byte or 2-Byte addressing mode) and 8 data bits. For all writes, data is committed in bytes as the eighth data bit of a data field that is clocked in on the rising edge of SCLK. If the write access is not an even multiple of 8 clocks, the trailing data bits are not committed. On a read access, data is clocked out on the falling edge of the serial interface clock, SCLK, on the SDO pin.

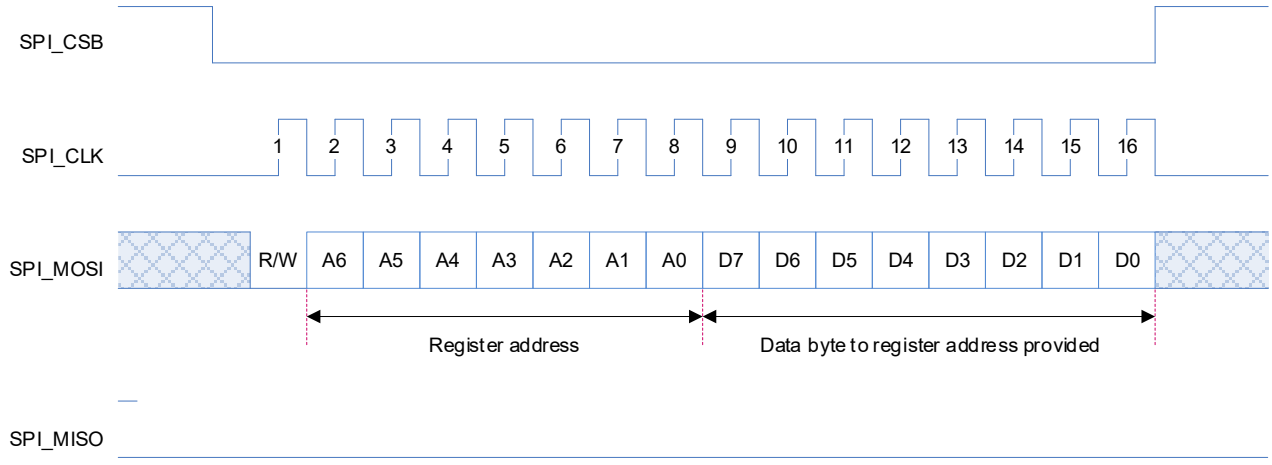


Figure 38. SPI Interface Write Bus Cycle (1 Byte of Register Address)

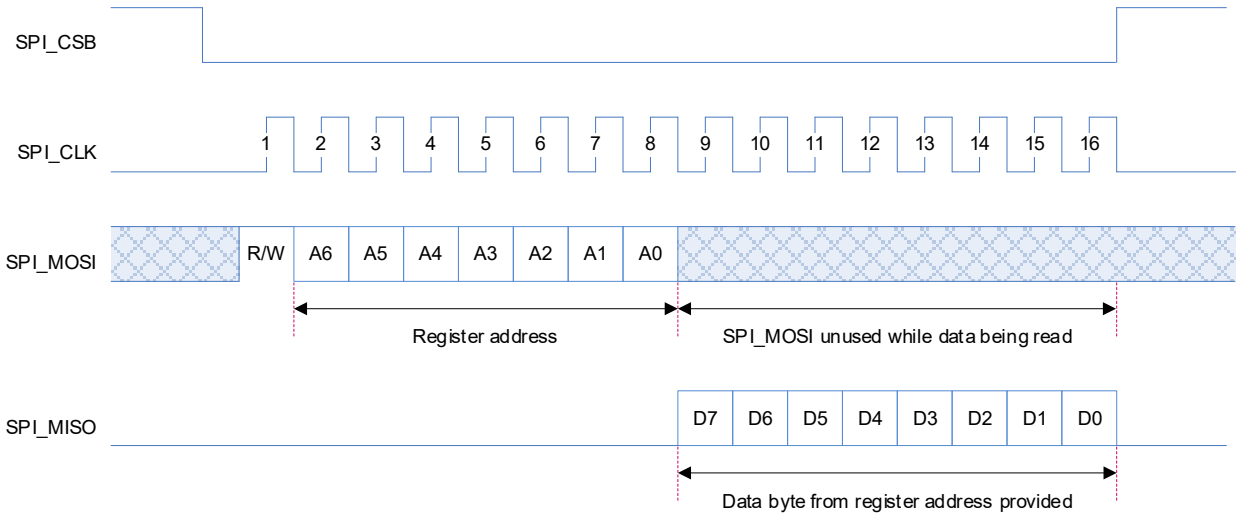


Figure 39. SPI Interface Read Bus Cycle (1 Byte of Register Address)

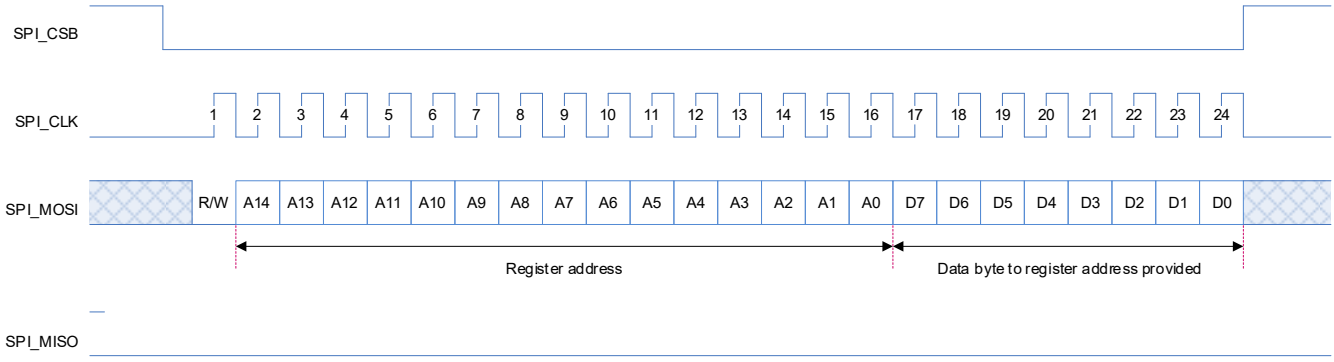


Figure 40. SPI Interface Write Bus Cycle (2 Bytes of Register Address)

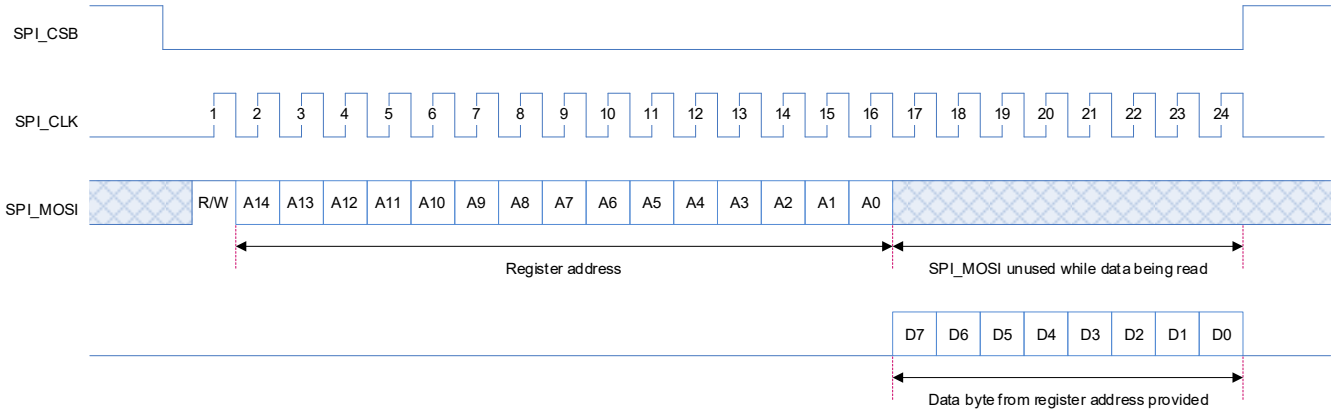


Figure 41. SPI Interface Read Bus Cycle (2 Bytes of Register Address)

The F39510 also supports a streaming mode that allows the user to read and write multiple bytes of data without specifically providing instructions for each byte. To activate the streaming mode, the CSB pin is continuously kept active as new data is shifted in and old data is shifted out of the device.

In streaming mode, the first instruction includes the starting address. The F39510 starts reading or writing to this address as long as the CSB pin is kept active, and the single byte write functionality has been disabled in the interface configuration register (address 0x0104). The F39510 automatically increments or decrements the address depending on the address ascend bit in register 0x0104.

If the address is decrementing and page offset 0x00 is reached, the next page offset used is 0x7D in both 1 byte and 2 bytes addressing mode. If the address is incrementing and page offset 0x7D is reached, the next page offset used is 0x00 in both 1 byte and 2 bytes addressing mode. Care should be taken when writing to address 0x0104 as writing to this address may change the configuration of the SPI Interface.

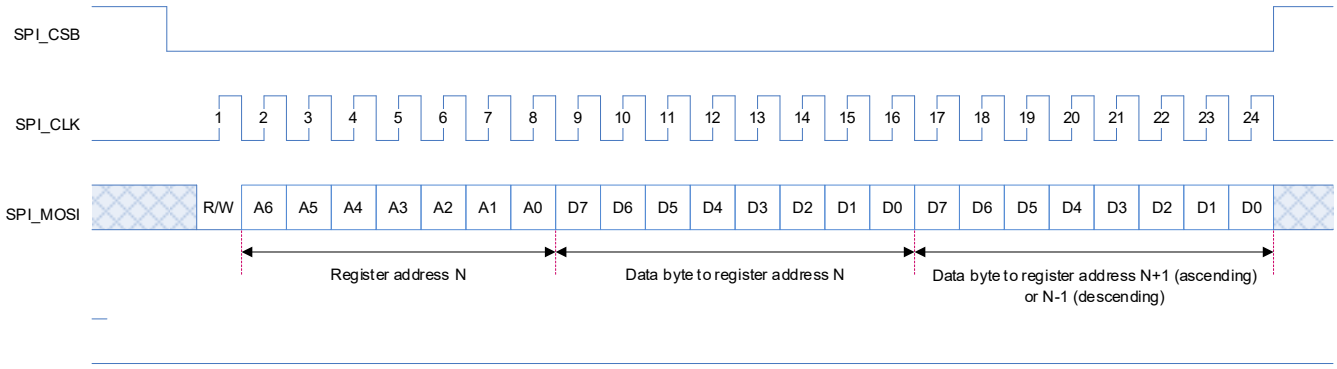


Figure 42. Serial Interface Streaming Write Example (1 Byte of Register Address)

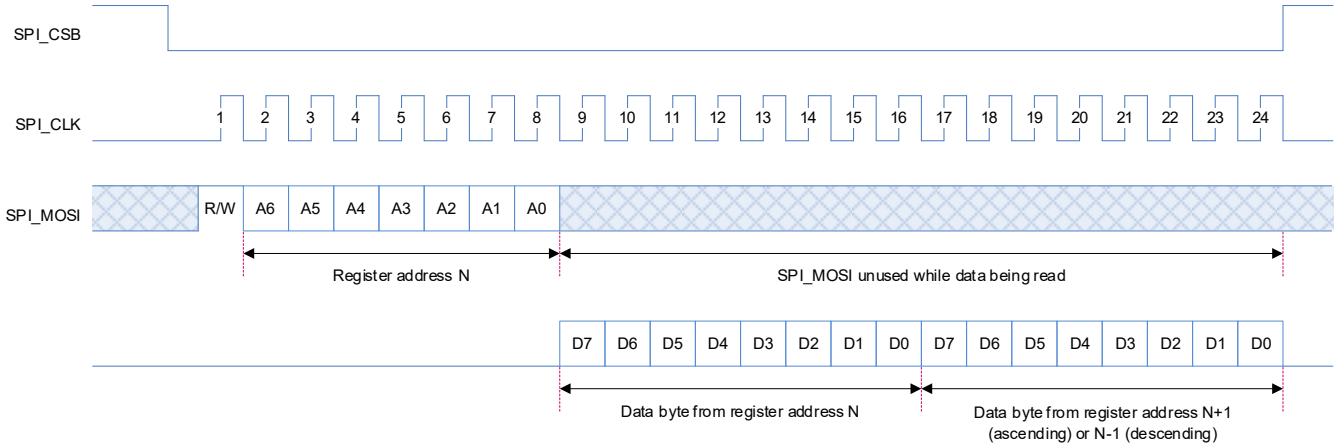


Figure 43. Serial interface Streaming Read Example (1 Byte of Register Address)

7.2 I3C Basic and I²C Programming

The F39510 supports a two-wire I3C basic serial interface that is backward compatible with many legacy I²C devices. In I3C basic mode the device can read/write speeds up to 12.5MHz. In I²C mode the device can read/write speeds up to 1MHz. The F39510 in I3C basic mode supports an SDR-only slave interface and In-Band interrupts. Programming the F39510 using the I3C/I²C bus requires using the SDA (Serial Data, Pin 10, bi-directional data) and SCL (Serial clock, Pin 11) pins. This device turns on in I²C mode by default. To configure the device in I3C/I²C operation the SDA pin must not be grounded.

7.2.1. Device Static Address

The F39510 supports 3-pin and 2-pin addressing mode for the slave static address selection based on the polarity of the A0, A1 and A2 pins (see Table 18 and Table 19).

Table 18. I3C Interface Two Address Pins Slave Address Space (default base value 0x8)

Device Pins			Static Address	
A2	**A1**	**A0**	**LID**	**HID**
N.C	Low	Low	011	1111
N.C	Low	N.C.	100	0000
N.C	Low	High	100	0001
N.C	N.C	Low	100	0010
N.C	N.C	N.C.	100	0011
N.C	N.C	High	100	0100
N.C	High	Low	100	0101
N.C	High	N.C.	100	0110
N.C	High	High	100	0111

Table 19. I3C Interface Three Address Pins Slave Address Space (default base value 0x8)

Device Pin			Static Address	
A2	**A1**	**A0**	**LID**	**HID**
Low	Low	Low.	100	0000
Low	Low	High	100	0001
Low	High	Low	100	0010
Low	High	High	100	0011
High	Low	Low	100	0100
High	Low	High	100	0101
High	High	Low	100	0110
High	High	High	100	0111

7.2.2. Device Dynamic Address

During the Initialization of the I3C bus, the master performs a "Dynamic Address Assignment" (DAA) to assign addresses to slave devices. DAA process can be achieved via the ENTDAA (Enter Dynamic Address Assignment), SETAASA (Set All Addresses to Static Address), or SETDASA (Set Dynamic Address from Static Address) command codes.

DAA process via ENTDAA command capitalizes on the unique provisional ID (6 bytes) + BCR (1 byte) + DCR (1 byte) content of all I3C devices on the bus (see Table 20 through Table 22). The F39510 static address (section 7.2.1) is part of the unique provisional ID, allowing ENTDAA “Dynamic Address Assignment” to support up to nine F39510 devices on the same I3C bus. If the master uses the ENTDAA command in a network with multiple slaves responding with the same provisional ID+BCR+DCR information, the master will fail to assign dedicated dynamic addresses correctly.

Table 20. I3C 48-bit Provisional ID Definition

Bits	Value (hex)	Register	Description
47:40	04	MIPI_MAN_ID_H	MIPI Manufacturer ID (high byte)

Bits	Value (hex)	Register	Description
39:32	CC	MIPI_MAN_ID_L	MIPI Manufacturer ID (low 7 bits) + PID type selector bit
31:24	0C	CHIP_ID_H	Vendor Part ID (high byte)
23:16	39	CHIP_ID_L	Vendor Part ID (low byte)
15:12	HID	-	Vendor Instance ID
12:8	8	CHIP_TYPE	Vendor Device Characteristics (high 4 bits)
7:0	00	CHIP_VERSION	Vendor Device Characteristics (low byte)

Table 21. I3C Bus Characteristics Register (BCR)

Bits	Value (hex)	Register	Description
7:0	0x03 at 1.8V 0x02 at 3.3V	-	IBI Request Capable, no payload

Table 22. I3C Device Characteristics Register (DCR)

Bits	Value (hex)	Register	Description
7:0	C7		PMIC MIPI Device ID. https://mipi.org/MIPI_I3C_device_characteristics_register

The provisional ID is not used when the SETAASA and SETDASA command codes are used to assign the Dynamic Address.

7.2.3. Switch from I²C Mode to I3C Basic Mode

The F39510 powers on in I²C mode by default until it is put into I3C mode by issuing one of the three DAA CCCs (ENTDAA, SETDASA, SETAASA). The first time the interface receives a START with I3C broadcast address 0x7E, the I²C spike filters are disabled so that subsequent I3C messages can be received. To ensure that the interface can detect the first START with address 0x7E when I²C spike filters are present and enabled, the I3C bus controller must send the first START with address 0x7E at Fm/Fm+ open-drain timing.

7.2.4. Switch from I3C Basic Mode to I²C Mode

The host can put the F39510 back in I²C mode from I3C Basic mode at any time by issuing RSTDAA (Reset Dynamic Address Assignment) CCC. When the interface registers RSTDAA CCC, it updates the I3C_MODE bit to 0 in the general status register (address 0x42).

7.2.5. I²C Slave Protocol

The I²C mode of operation is the primary mode of operation when the device is powered up. If the device is in I3C mode of operation, then issuing a “Reset Dynamic Address Assignment” RSTDAA CCC also reverts the mode of operation back to I²C. In I²C mode, the maximum bus speed supported is 1.0 MHz, and IBI and Parity Error Check features are not supported.

In the I²C mode of operation, the device supports ENTDAA, SETDASA, SETAASA CCCs and data transfer packets. Additionally, a Start or Repeated Start followed by 7'h7E with W = 0 is only allowed for the purpose of issuing the supported CCCs.

For I²C write operation, the host controller sends the device address with R/W bit as 0, after a Start or Repeated Start as shown in Table 23 and Table 24. This is followed by the 1 byte (ADDR_MODE = 0) or 2 bytes (ADDR_MODE = 1) register address and then the data.

The interface writes the data to the register address specified. The internal write register address pointer is incremented or decremented after every data byte is written.

Table 23. I²C Write Command Data Packet (1 Byte of Register Address)

Write Operation with 1 Byte of Register Address										
Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	W = 0	A	
	A7	A6	A5	A4	A3	A2	A1	A0	A	
	D7	D6	D5	D4	D3	D2	D1	D0	A	
	D7	D6	D5	D4	D3	D2	D1	D0	A	
	…….								A	
	D7	D6	D5	D4	D3	D2	D1	D0	A	Sr or P

Byte Description
Static Address[6:0] + W
Register Address[7:0]
Data Write Reg#0
Data Write Reg#1
…….
Data Write Reg#n

Table 24. I²C Write Command Data Packet (2 Bytes of Register Address)

Write Operation with 2 Bytes of Register Address										
Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	W = 0	A	
	A7	A6	A5	A4	A3	A2	A1	A0	A	
	X	A14	A13	A12	A11	A10	A9	A8	A	
	D7	D6	D5	D4	D3	D2	D1	D0	A	
	D7	D6	D5	D4	D3	D2	D1	D0	A	
	…….								A	
	D7	D6	D5	D4	D3	D2	D1	D0	A	Sr or P

Byte Description
Static Address[6:0] + W
Register Address[7:0]
Register Address[14:0]
Data Write Reg#0
Data Write Reg#1
…….
Data Write Reg#n

For an I²C read operation, the host controller sends the device address with R/W bit as 0, after a Start or repeated start as shown in Table 25 and Table 26. This is followed by the 1 byte (ADDR_MODE = 0) or 2 bytes (ADDR_MODE = 1) register address. Once the register address is available to the device, the host issues a Repeated Start and sends the device address with R/W bit as 1. At this point, the device shall send the data from the register address incrementally until the host sends a NACK.

Table 25. I²C Read Command Data Packet (1 Byte of Register Address)

Read Operation with 1 Byte of Register Address										
Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	W = 0	A	
	A7	A6	A5	A4	A3	A2	A1	A0	A	
Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	R = 1	A	
	D7	D6	D5	D4	D3	D2	D1	D0	A	
	D7	D6	D5	D4	D3	D2	D1	D0	A	
	…….								A	
	D7	D6	D5	D4	D3	D2	D1	D0	N	Sr or P

Table 26. I²C Read Command Data Packet (2 Bytes of Register Address)

Read Operation with 2 Bytes of Register Address										
Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	W = 0	A	
	A7	A6	A5	A4	A3	A2	A1	A0	A	
	X	A14	A13	A12	A11	A10	A9	A8	A	
Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	R = 1	A	
	D7	D6	D5	D4	D3	D2	D1	D0	A	
	D7	D6	D5	D4	D3	D2	D1	D0	A	
	…….....								A	
	D7	D6	D5	D4	D3	D2	D1	D0	N	Sr or P

Byte Description
Static Address[6:0] + W
Register Address[7:0]
Register Address[14:0]
Slave Address[6:0] + R
Data Read Reg#0
Data Read Reg#1
…….....
Data Read Reg#n

7.2.6. I3C Slave Protocol

The F39510 must always be set to the I3C basic mode of operation from the I²C mode of operation. In the I3C basic mode, the device can support data transfer rates of up to 12.5MHz (V_{DD} 3.3V) with a push-pull SDA driver. In addition, IBI (disabled by default in I²C mode) can now be enabled. Parity check is always enabled.

As shown in Table 27,

Table 2828, Table 29, and Table 30, an I3C basic write operation is the same as an I²C write operation. For all bytes after the device address field, the 9th bit is the parity bit sent by the host. When the host enables the IBI, it must send the IBI header byte, which consists of 7'h7E+R/W=0 before it sends the device address. This allows the participating devices on the bus to arbitrate between themselves if more than one device has an interrupt condition that needs to be communicated to the host.

If there is a parity error during the data transfer, the device shall discard all the bytes, including the byte for which parity error was detected and set the parity error condition. If the host attempts to start a new transaction with a Repeated Start to the same device, the slave shall NACK the device address to indicate an error condition. The host must first clear the parity error condition before performing any new transfer to the F39510. When IBI is enabled, the device can communicate the error conditions seen to the host using IBI. However, when IBI is not enabled, it is strongly recommended that the host check the error status register to ensure that no parity error was detected on the bus.

Table 27. I3C Write Command Data Packet (1 Byte of Register Address)

Write Operation with 1 Byte of Register Address										
Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	W = 0	A	
	A7	A6	A5	A4	A3	A2	A1	A0	T	
	D7	D6	D5	D4	D3	D2	D1	D0	T	
	D7	D6	D5	D4	D3	D2	D1	D0	T	
	…….								T	
	D7	D6	D5	D4	D3	D2	D1	D0	T	Sr or P

Byte Description
Dynamic Address[6:0] + W
Register Address[7:0]
Data Write Reg#0
Data Write Reg#1
…….
Data Write Reg#n

Table 28. I3C Write Command Data Packet with IBI Header (1 Byte of Register Address)

Write Operation with 1 Byte of Register Address and IBI Header										
Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A	
Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	W = 0	A	
	A7	A6	A5	A4	A3	A2	A1	A0	T	
	D7	D6	D5	D4	D3	D2	D1	D0	T	
	D7	D6	D5	D4	D3	D2	D1	D0	T	
	…….								T	
	D7	D6	D5	D4	D3	D2	D1	D0	T	Sr or P

Byte Description
7'h7E + W
Dynamic Address[6:0] + W
Register Address[7:0]
Data Write Reg#0
Data Write Reg#1
…….
Data Write Reg#n

Table 29. I3C Write Command Data Packet (2 Bytes of Register Address)

Write Operation with 2 Bytes of Register Address										
Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	W = 0	A	
	A7	A6	A5	A4	A3	A2	A1	A0	T	
	X	A14	A13	A12	A11	A10	A9	A8	T	
	D7	D6	D5	D4	D3	D2	D1	D0	T	
	D7	D6	D5	D4	D3	D2	D1	D0	T	
	…….								T	
	D7	D6	D5	D4	D3	D2	D1	D0	T	Sr or P

Byte Description
Dynamic Address[6:0] + W
Register Address[7:0]
Register Address[14:0]
Data Write Reg#0
Data Write Reg#1
…….
Data Write Reg#n

Table 30. I3C Write Command Data Packet with IBI Header (2 Bytes of Register Address)

Write Command Data Packet with IBI Header with 2 Bytes of Register Address										
Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A	
S or Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	W = 0	A	
	A7	A6	A5	A4	A3	A2	A1	A0	T	
	X	A14	A13	A12	A11	A10	A9	A8	T	
	D7	D6	D5	D4	D3	D2	D1	D0	T	
	D7	D6	D5	D4	D3	D2	D1	D0	T	
	…….								T	
	D7	D6	D5	D4	D3	D2	D1	D0	T	Sr or P

Byte Description
7'h7E + W
Dynamic Address[6:0] + W
Register Address[7:0]
Register Address[14:0]
Data Write Reg#0
Data Write Reg#1
…….
Data Write Reg#n

As shown in Table 31, Table 32, Table 33 and Table 34, an I3C basic mode read is the same as I^2C read operation. For all bytes sent by the device, the 9th bit is the T-bit, which the device and host use to negotiate the continuation of the read transfer. During the read phase, the device drives the T-bit as 1, before the rising edge to tell the host that it can send more bytes or drives the T-bit as 0, to indicate to the host that the device wants to terminate the transfer and the host shall respond with either a Stop or Repeated Start on the bus. The host may also terminate the transfer by driving the T-bit as 0, only when the device sends the T-bit as 1, which creates a repeated start condition on the bus. Additionally, the host may send a Stop on the bus. When the host enables the IBI, it must send the IBI header byte, which consists of 7'h7E+R/W = 0, before it sends the device address. This allows the participating devices on the bus, to arbitrate between themselves if more than one device has an interrupt condition that needs to be communicated to the host.

Table 31. I3C Read Command Data Packet (1 byte of Register Address)

Read Operation with 1 byte of Register Address									
Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	W = 0	A	
	A7	A6	A5	A4	A3	A2	A1	A0	T	
Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	R = 1	A	
	D7	D6	D5	D4	D3	D2	D1	D0	T=1	
	D7	D6	D5	D4	D3	D2	D1	D0	T=1	
	…….								T=1	
	D7	D6	D5	D4	D3	D2	D1	D0	T	Sr or P

Byte Description
Dynamic Address[6:0] + W
Register Address[7:0]
Dynamic Address[6:0] + R
Data Read Reg#0
Data Read Reg#1
…….
Data Read Reg#n

Table 32. I3C Read Command Data Packet with IBI Header (1 byte of Register Address)

Read Operation with 1 byte of Register Address and IBI Header									
Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A	
Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	W = 0	A	
	A7	A6	A5	A4	A3	A2	A1	A0	T	
Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	R = 1	A	
	D7	D6	D5	D4	D3	D2	D1	D0	T=1	
	D7	D6	D5	D4	D3	D2	D1	D0	T=1	
	…….								T=1	
	D7	D6	D5	D4	D3	D2	D1	D0	T	Sr or P

Byte Description
7'h7E + W
Dynamic Address[6:0] + W
Register Address[7:0]
Dynamic Address[6:0] + R
Data Read Reg#0
Data Read Reg#1
…….
Data Read Reg#n

Table 33. I3C Read Command Data Packet (2 bytes of Register Address)

Read Operation with 2 bytes of Register Address										
Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	W = 0	A	
	A7	A6	A5	A4	A3	A2	A1	A0	T	
	X	A14	A13	A12	A11	A10	A9	A8	T	
Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	R = 1	A	
	D7	D6	D5	D4	D3	D2	D1	D0	T=1	
	D7	D6	D5	D4	D3	D2	D1	D0	T=1	
	…….....								T=1	
	D7	D6	D5	D4	D3	D2	D1	D0	T	Sr or P

Byte Description
Dynamic Address[6:0] + W
Register Address[7:0]
Register Address[14:0]
Dynamic Address[6:0] + R
Data Read Reg#0
Data Read Reg#1
…….....
Data Read Reg#n

Table 34. I3C Read Command Data Packet with IBI Header (2 bytes of Register Address)

Read Operation with 2 bytes of Register Address and IBI Header										
Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A	
Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	W = 0	A	
	A7	A6	A5	A4	A3	A2	A1	A0	T	
Sr	X	A14	A13	A12	A11	A10	A9	A8	T	
Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	R = 1	A	
	D7	D6	D5	D4	D3	D2	D1	D0	T=1	
	D7	D6	D5	D4	D3	D2	D1	D0	T=1	
	…….....								T=1	
	D7	D6	D5	D4	D3	D2	D1	D0	T	Sr or P

Byte Description
7'h7E + W
Dynamic Address[6:0] + W
Register Address[7:0]
Register Address[14:0]
Dynamic Address[6:0] + R
Data Read Reg#0
Data Read Reg#1
…….....
Data Read Reg#n

7.2.7. I3C Basic Common Command Codes (CCC)

The F1594 device supports the I3C CCC commands listed in Table 35.

Table 35. I3C Interface CCC Supported Commands

Command	Mode	Code	Default	Description	Applicable Mode
ENEC	Broadcast	0x00	On	Enable Event Interrupts	I3C
	Direct	0x80			
DISEC	Broadcast	0x01	Off	Disable Event Interrupts	I3C
	Direct	0x81			
RSTDAA	Broadcast	0x06	-	Disable Event Interrupts (Direct CCC deprecated in V1.1)	I3C
	Direct	0x86			
GETPID	Direct	0x8D	0x04 0xCC 0x0C 0x39 0x(4'bHID)8 0x00	Get Provisional ID	I3C
GETBCR	Direct	0x8E	3.3V: 0x02 1.8V: 0x03 Refer to Table 36	Get Bus Characteristics Register	I3C
GETDCR	Direct	0x8F	0xC7	Get Device Characteristics Register	I3C
GETSTATUS	Direct	0x90		Get Device Status	I3C
GETMXDS	Direct	0x94	3.3V: 0x00, 0x20 1.8V: 0x02, 0x3A(default) Refer to Table 36	Get max. RD/WR data speeds	I3C
ENTDAA	Broadcast	0x07	-	Enter Dynamic Address Assignment	I^2C
SETDASA	Direct	0x87	-	Set Dynamic Address from Static Address	I^2C
SETNEWDA	Direct	0x88	-	Set New Dynamic Address	I3C
SETAASA	Broadcast	0x29	-	Set All Addresses to Static Addresses	I^2C

Table 36: I3C GETMXDS CCC maxWr and maxRd byte configuration at 1.8V IOVDD

I3C_MAX_DS[2:0]	Max Rd and Wr Data Rate	Clock to Data Turnaround Time (t_{SCO})	GETMXDS {maxWr, maxRd}	GETBCR
0xx	12.5MHz	≤ 12 ns	0x00, 0x20	0x02
100	8 MHz	> 12 ns	0x01, 0x39	0x03
101	6 MHz	> 12 ns	0x02, 0x3A	0x03
110	4 MHz	> 12 ns	0x03, 0x3B	0x03
111	2 MHz	> 12 ns	0x04, 0x3C	0x03

7.2.8. IO Operation

At power-on, by default, the device comes up in the I²C mode of operation with Open-Drain IO for the serial interface. The maximum speed is limited to 400kHz, and supported IO voltage levels are from 1.8V to 3.3V.

After power-on, the host can put the device's serial interface in the I3C Basic mode of operation. In I3C Basic mode of operation, the maximum speed is limited to 12.5MHz, at an IO voltage level of 3.3V.

In I3C Basic mode, the host can drive the SCL clock input of the device using either Push-Pull output driver or using the open-drain output driver. It is expected that for F39510 use cases, the host can always drive the SCL clock input using a Push-Pull output driver.

The device supports dynamic switching between Open-Drain mode and Push-Pull mode on its SDA bus for various events. Table 37 describes the different mode of operation by the device for each cycle in I3C Basic mode.

Table 37. I3C Interface Dynamic IO Operation Mode Switching

Bus Event	SDA Mode
START + Device Select Code	Open-Drain
START + 7'h7E IBI Header Byte	Open-Drain
REPEAT START + Device Select Code	Push-Pull
REPEAT START + 7'h7E Header Byte	Push-Pull
CCC Byte (in other words, after 7'h7E+W = 0+ACK)	Push-Pull
STOP	Push-Pull
ACK/NACK Responses	Open-Drain
Command, Block Address, Address Operation	Push-Pull
Interrupt Request by Slave	Open-Drain
Write Data, T-bit Sequence	Push-Pull
Read Data, T-bit Sequence	Push-Pull

The F39510 supports spike filters (~50ns) on its SCL and SDA inputs per definition in I²C specifications. Immediately after reset, the spike filters are enabled because it is unknown whether the device is attached to an I²C or I3C bus. The first time the F39510 receives a START with I3C broadcast address 0x7E, I²C spike filters are disabled so that subsequent I3C messages can be received.

To ensure that the interface can detect the first START with address 0x7E when I²C spike filters are present and enabled, the I3C bus controller must send the first START with address 0x7E at Fm open-drain SCL timing.

7.3 Paging

In 1-byte addressing mode the address space is wider than what can be addressed with the size of the address field of the serial interface therefore paging is required. In 2-byte addressing mode up to 32768 registers can be addressed so paging is not implemented. Figure 44 shows how page register and offset bytes from each serial transaction interact to address a register within the serial interface.

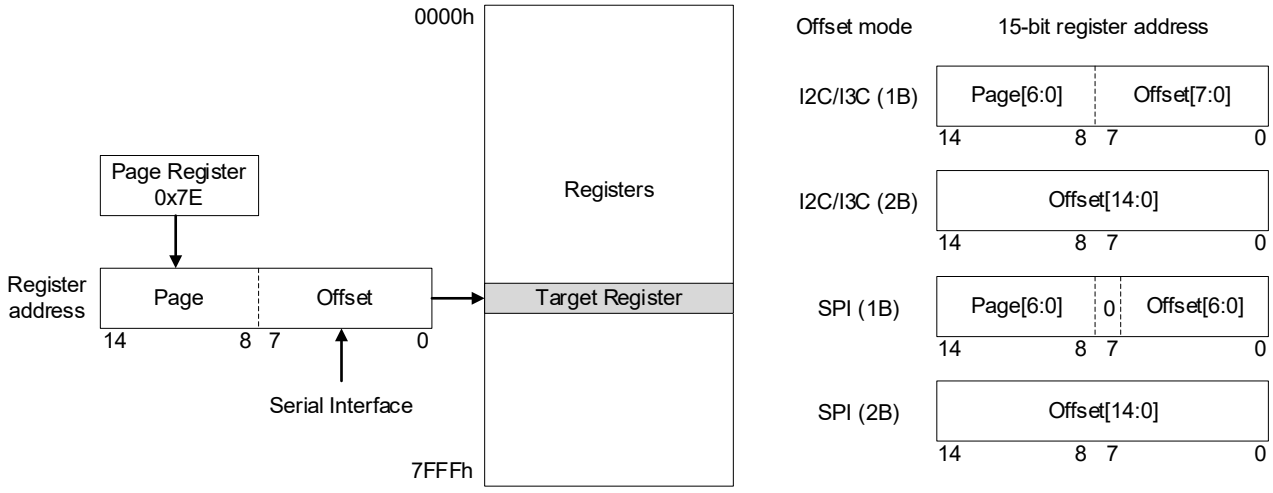


Figure 44: Register Addressing Mode via Serial Interface

I²C/I3C and SPI 1-byte (1B) or 2-byte (2B) offset addressing is selected with IF_CFG.ADDR_MODE bit.

In 1B mode, the 15-bit register address is formed by using the 8 bits of address supplied in the I2C/I3C access and taking the upper 7 bits from the page register. In case of SPI access, the lower 7 bits are supplied and bit[7] of the register address is set to 0. The page register is accessed using an Offset Address of 0x7E from any page

In 2B mode, the 15-bit register address is formed by using the 15 bits of address supplied in the I2C/I3C/SPI access (page register is not used).

Address 0x7E is used to address different pages. Within each page the user can access each individual register field starting from 0x00. The page register holds the current page settings until the register is programmed with a new value. Examples of a write to the Page register in I²C and SPI mode are shown in Table 38 and Figure 44 respectively.

Table 38: I²C Write Command to Page Register

Write Operation with 1 byte of Register Address										
Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	W = 0	A	
	0	1	1	1	1	1	1	0	A	
	D7	D6	D5	D4	D3	D2	D1	D0	A	Sr or P

Byte Description
Static Address[6:0] + W
Page Register Address
Page Number

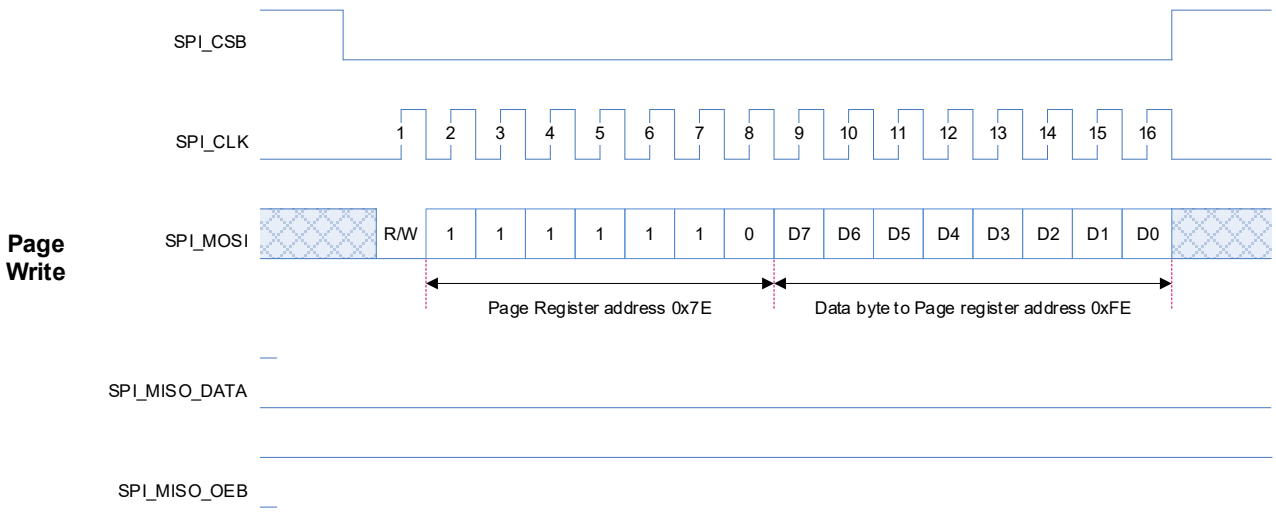


Figure 45: SPI Write to Page Register

The F39510 uses the page system to group and organize the user registers by their functionalities, as shown in Table 39.

Table 39: Page Organization of Address Space

Page number	Size (bytes)	Description
0	-	Reserved
1 (default)	114	Main configuration registers
2	108	LUTs and temperature sensors trimming data
3	14	Alarms Configuration registers
15	21	Notepad area

8. Quick Start Guide

This section provides instructions on how to bring up the F39510 in I3C mode.

8.1 Power Supply Sequencing

To ensure proper device operation, adhere to the following power supply sequencing steps:

N10 Mode:

1. AVSS is first powered up to -8V.
2. AVDD (5V) and IOVDD (1.8V min) are then powered up together.
3. AVCC is set to 0V under the N10 mode.
4. The PA power supply is to be done following these sequences.

P10 Mode:

1. AVSS is set to 0V.
2. AVDD (5V) and AVCC (5V) are ramped up together.
3. IOVDD (1.8V min) is then powered up.
4. The PA power supply is to be done following these sequences.

Note: The power supply sequence shown is the recommended sequence for proper product bring up. For any deviation from the above-mentioned power-up sequence, please contact your local Axiro Sales representative.

8.2 DAC Load Capacitor Select

The F39510 supports a range of DAC load capacitors that are configurable in the register area. The two DAC load capacitor ranges are from 0uF to 0.1uF and from 0.1uF to 15uF. This is also highlighted in the description section of the register map. The user can choose the DAC load capacitance range as per their needs using register (0x016C). By default, the DAC load capacitance range is configured to the 0uF to 0.1uF range.

- Configure the DAC load capacitor range to 0uF – 0.1uF (Reg Addr: 0x016C = 0x00) – This is the default range.
- Configure the DAC load capacitor range to 0.1uF – 15uF (Reg Addr: 0x016C = 0xFF)

For more information on the configurability of register 0x016C, see the “Register Map”.

8.3 I3C Interface Initialization

The F39510 will wake up in I²C mode and can be set to operate in I3C Basic mode by setting the dynamic address using any of the three methods below:

Method	Command	Mode	Code	Description
1	ENTDAA	Broadcast	0x07	Enter Dynamic Address Assignment. Command issued by master is received by all slave devices.
2	SETDASA	Direct	0x87	Set Dynamic Address from Static Address Command issued by master is for a specific slave device.
3	SETAASA	Broadcast	0x29	Set all Addresses to Static Addresses. Command issued by master is received by all slave devices.

After the master assigns the F39510 its dynamic address, it can send I3C write and read commands to communicate with the device. User registers are from address 0x00 – 0x7D and 1 byte header mode is recommended.

8.3.1. I3C BUS Initialization Command Examples

Note: All examples assume that the LID is set to 000 and HID to 1111 with A1 (pin 6) and A0 (pin 7) pin set to GND.

- F39510 I3C PID is 0x04CC0C39F800
- F39510 I3C Bus Characteristics Register (BCR) value is hex 0x02
- F39510 I3C Device Characteristics Register (DCR) value is hex 0xC7

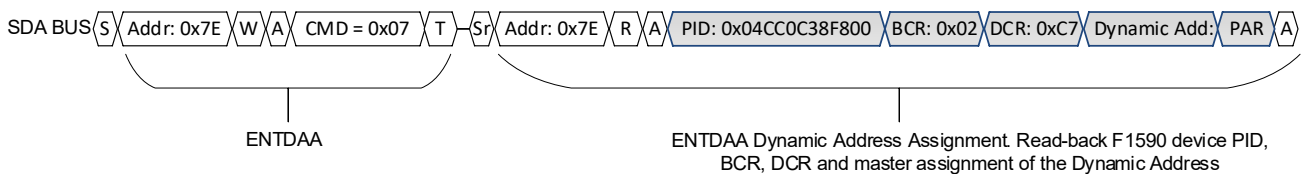
All F39510 static address configurations are shown in the following table.

Device Pins			Static Address	
A2	**A1**	**A0**	**LID**	**HID**
N.C	Low	Low	011	1111
N.C	Low	N.C.	100	0000
N.C	Low	High	100	0001
N.C	N.C	Low	100	0010
N.C	N.C	N.C.	100	0011
N.C	N.C	High	100	0100
N.C	High	Low	100	0101
N.C	High	N.C.	100	0110
N.C	High	High	100	0111

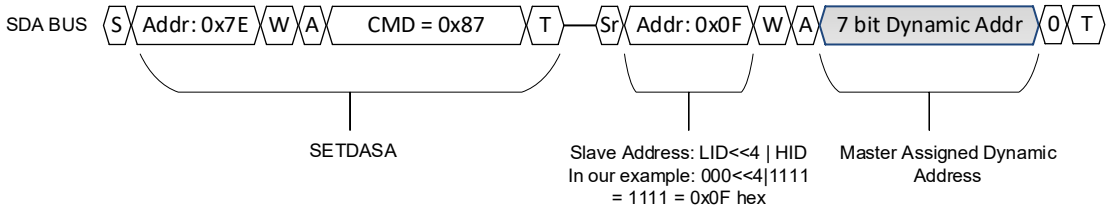
The F39510 I3C provisional ID is defined according to the following table. All examples assume HID 1111.

Bits	Value (hex)	Register	Description
47:40	04	MIPI_MAN_ID_H	MIPI Manufacturer ID (high byte)
39:32	CC	MIPI_MAN_ID_L	MIPI Manufacturer ID (low 7 bits) + PID type selector bit
31:24	0C	CHIP_ID_H	Vendor Part ID (high byte)
23:16	39	CHIP_ID_L	Vendor Part ID (low byte)
15:12	HID	-	Vendor Instance ID (HID, Set to 1111 for all examples)
12:8	8	CHIP_TYPE	Vendor Device Characteristics (high 4 bits)
7:0	00	CHIP_VERSION	Vendor Device Characteristics (low byte)

Example 1: ENTDAA sequence

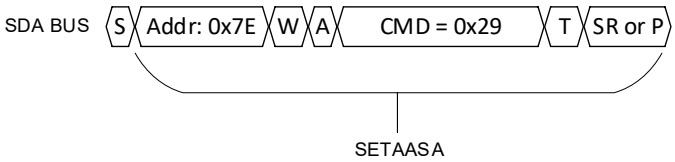


Example 2: SETDASA sequence



SETDASA command should be used before the ENTDAA command is used; all slaves without assigned Dynamic Address will respond to the ENTDAA command.

Example 3: SETAASA sequence



Fastest method to assign I3C Dynamic address to all slaves with Static Addresses.

8.4 ADC Initialization Procedure (ADC_0)

For proper ADC_0 initialization, complete the steps in the following order:

1. Enable ADC (Reg Addr: 0x0166 = 0x01)
2. Configure ADC to direct mode (Reg Addr: 0x0162 = 0x10)
3. Select ADC channel 0 (ADC_0) (Reg Addr: 0x0113 = 0x01)
4. Start ADC conversion (Reg Addr: 0x015F = 0x01)
5. Wait 1ms
6. Read back the content of the 8-bit Low Byte ADC_0 data register (Reg Addr: 0x0120)
7. Read back the content of the 4-bit High Byte ADC_0 data register (Reg Addr: 0x0121)
8. Disable ADC (Reg Addr: 0x0166 = 0x00)

8.5 DAC Initialization Procedure

To ensure proper DAC initialization, complete the steps in the following order:

1. The DACs are configured using the lower capacitive load range by default.
2. To change this to the high capacitive load range in other words, between 0.1µF to 15µF
   (Reg Addr: 0x016C = 0xFF)
   Note: The REFDACs must always be maintained at a voltage lower than or equal to that of the main DACs. (This condition does not apply to DAC0 and DAC3)
3. To control OUT-1 with ENABLE-1 pin and OUT-2 with ENABLE-2 pin, Perform the following register writes:
   - Enabling DAC0 and DAC3 switches (Reg Addr: 0x0163 = 0x09)
   - To Control OUT-1 with ENABLE-1 and to control OUT-2 with ENABLE-2 (Reg Addr: 0x0164 = 0x42)
4. Enable All DACs (Reg Addr: 0x0165 = 0xFF).
5. Wait 5ms.
6. Bypass the LUT for manual DAC control (Reg Addr: 0x011A = 0xEE)
7. Load DAC data registers. All the DAC codes can be loaded simultaneously. An example of this is indicated below for setting the DACs to their mid value:
   a. Update all DAC registers from address 0x0140 to 0x014B with the desired codes:

Example: Setting DAC 0 to 2.5V (Positive Mode) or -7.5V (Negative Mode)

Reg Addr: 0x0140 = 0x00 (Low Byte 8 LSB)
Reg Addr: 0x0141 = 0x08 (High Byte 4 MSB)

Example: Setting DAC 1 to 2.5V (Positive Mode) or -7.5V (Negative Mode)

Reg Addr: 0x0142 = 0x00 (Low Byte 8 LSB)
Reg Addr: 0x0143 = 0x08 (High Byte 4 MSB)

Example: Setting REFDAC 1 to 2.5V (Positive Mode) or -7.5V (Negative Mode)

Reg Addr: 0x0144 = 0x00 (Low Byte 8 LSB)
Reg Addr: 0x0145 = 0x08 (High Byte 4 MSB)

Writing 0x00 to the Low Byte and 0x08 to the High Byte registers for DAC 2, DAC 3 and REFDAC 2 will also set the output voltage of 2.5V (Positive Mode) or -7.5V (Negative Mode) respectively.

8. Set register 0x0112 = 0x01 this will load all the DACs simultaneously

8.6 LUT Voltage-to-Temperature Transfer Function Initialization Procedure

To properly initialize the LUT, registers from Page 02, Address 0x00 to 0x6B must be accessed. The descriptions for these registers are in the “Register Map”.

- DAC baseline registers (LUT control): 0x0200 to 0x0207
- DAC data registers (LUT coefficients): 0x0208 to 0x026B
- LUT slope control registers: 2-bit control in registers 0x0220 (for DAC0), 0x0239 (for DAC1), 0x0252 (for DAC2), and 0x026B (for DAC3)

After the DAC baseline registers are configured, the slope for each DAC is defined and the LUT values are burned to the DAC data registers as per the user’s requirement. The following steps are to be followed:

1. Enable the ADC (Reg Addr: 0x0166 = 0x01).
2. Configure the ADC to direct mode with the reference buffer enabled (Reg Addr: 0x0162 = 0x10).
3. Apply averaging to the ADC (Reg Addr: 0x0161 = 0x04).
   a. Set the LUT to autonomous mode (Reg Addr: 0x0167 = 0x88)
   b. Enable all the DACs (Reg Addr: 0x0165 = 0xEE)

      Note: The DACs must be configured as per the user’s requirements.
   c. Provide a wait time after the DACs are enabled (Reg Addr: 0x0168 = 0x3F).

      Note: The timer for the device-ready signal is set to ~158ms. This can be reduced as per the application requirements of the user (for more information, see the “Register Map”).
   d. Burn the EEPROM registers (Reg Addr: 0x0111 = 0xE5) and power cycle the device to enable the device to power up with the LUT in Autonomous mode, ADC enabled, and the DACs configured as per the requirement.
      Note: If this EEPROM burn and reset has been done previously for these configurations, this step can be skipped
   e. Check the burn status using the LSB of the LUT_E2P_CNTL register (Reg Addr: 0x0111) and only reset the device once the burn transfer has been completed.
   f. Set the temperature input to the LUT to be generated by the Local temperature sensor (Reg Addr: 0x011A = 0x00).
      Note: To manually enter the temperature inputs, the TEMP override registers can be used (Reg Addr: 0x011A = 0x01). For more information, see the “Register Map”.
   g. Enable readback from the DAC_OVRD registers using the REG_UPDATE register (Reg Addr: 0x0112 = 0x20)

h. Read the DAC codes from the DAC_OVRD registers (Reg Addr: 0x0140 – 0x014B).

8.7 Remote Temperature Sensor Initialization Procedure

For proper RT initialization, follow the steps in the order shown below:

1. Enable ADC (Reg Addr: 0x0166 = 0x01)
2. Configure ADC to direct mode (Reg Addr: 0x0162 = 0x10)
3. Select RT ADC channel (Reg Addr: 0x010A = 0x02)
4. Start ADC conversion (Reg Addr: 0x015F = 0x01)
5. Read back content of Reg Addr: 0x0150: If 0x0150<0> = 1 ADC conversion is complete
6. Read back the content of the 8-bit High Byte D1- data register (Reg Addr: 0x0102)
7. Read back the content of the 4-bit Low Byte D1- data register (Reg Addr: 0x0103)
8. Disable ADC (Reg Addr 0x0166 = 0x00)

8.8 Local Temperature Sensor Initialization Procedure

For proper LT initialization, complete the following steps:

1. Select Temp sensor measurement (Reg Addr: 0x010A = 0x01)
2. Enable ADC (Reg Addr: 0x0166 = 0x01)
3. Configure ADC to direct mode (Reg Addr: 0x0162 = 0x10)
4. Start ADC conversion (Reg Addr: 0x015F = 0x01)
5. Wait for 2ms
6. Read back the content of the 8-bit High Byte LT_DATA_H data register (Reg Addr: 0x0100)
7. Read back the content of the 4-bit Low Byte LT_DATA_L data register (Reg Addr: 0x0101)
8. Disable ADC (Reg Addr 0x0166 = 0x00)

8.9 EEPROM Fast-mode

The EEPROM contains a list of registers that can be programmed and burned as and when required. The EEPROM burn process approximately requires 8s of time for the full and proper completion of the burn. The burn status can be checked in register 0x0111 (Page 01).

The EEPROM can also be put into a “Fast-mode” state. When the EEPROM is configured to the fast-mode state, the burn time reduces by almost 50% to only 4.5s. This can be done using the register write shown below. Please note that this register write will be wiped out during a RESET. Therefore, the user must perform the following register write each time the device is reset if they require the fast-mode functionality of the EEPROM.

1. Configure EEPROM to fast-mode (Reg Addr: 0x1101 = 0x02)

9. Register Map

Table 40. Register Map

Page/Offset	Address	Type	Default	Register Name
0x00	0x7E	R/W	0x01	MEM_PAGE
0x01	0x00	R	0x40	LT_DATA_H
0x01	0x01	R	0x00	LT_DATA_L
0x01	0x02	R	0x40	RT_DATA_H
0x01	0x03	R	0x00	RT_DATA_L
0x01	0x04	R/W	0x40	IF_CFG
0x01	0x05	-	-	RSVD_0X0105
0x01	0x06	-	-	RSVD_0X0106
0x01	0x07	R/W	0x00	SOFT_RESET
0x01	0x08	R/W	0x04	TEMP_CFG
0x01	0x09	-	-	RSVD_0X0109
0x01	0x0A	R/W	0x03	LUT_CFG
0x01	0x0B	R	0x08	CHIP_TYPE
0x01	0x0C	R	0x49	CHIP_ID_L
0x01	0x0D	R	0x0C	CHIP_ID_H
0x01	0x0E	R	0x01	CHIP_VERSION
0x01	0x0F	R	0xCC	MIPI_MAN_ID_L
0x01	0x10	R	0x04	MIPI_MAN_ID_H
0x01	0x11	R/W	0x00	LUT_E2P_CNTL
0x01	0x12	R/W	0x00	REG_UPDATE
0x01	0x13	R/W	0x00	ADC_MUX_CFG
0x01	0x14	R/W	0x00	ADC_MUX_CFG_1
0x01	0x15	-	-	RSVD_0X0115
0x01	0x16	-	-	RSVD_0X0116
0x01	0x17	R	0x00	ALR_STAT_0
0x01	0x18	R	0x00	ALR_STAT_1
0x01	0x19	R/W	0x00	DAC_CLR
0x01	0x1A	R/W	0x00	OVRD_CTRL
0x01	0x1B	R/W	0x00	TEMP_OVRD_1_L
0x01	0x1C	R/W	0x00	TEMP_OVRD_1_H

Page/Offset	Address	Type	Default	Register Name
0x01	0x1D	R/W	0x00	TEMP_OVRD_2_L
0x01	0x1E	R/W	0x00	TEMP_OVRD_2_H
0x01	0x1F	R	0xB3	VENDOR_ID
0x01	0x20	R	0x00	ADC_IN0_DATA_L
0x01	0x21	R	0x00	ADC_IN0_DATA_H
0x01	0x22	R	0x00	ADC_IN1_DATA_L
0x01	0x23	R	0x00	ADC_IN1_DATA_H
0x01	0x24	R	0x00	ADC_LT_DATA_L
0x01	0x25	R	0x40	ADC_LT_DATA_H
0x01	0x26	R	0x00	ADC_RT_DATA_L
0x01	0x27	R	0x40	ADC_RT_DATA_H
0x01	0x28	R	0x00	ADCINT_DAC_0_DATA_L
0x01	0x29	R	0x00	ADCINT_DAC_0_DATA_H
0x01	0x2A	R	0x00	ADCINT_DAC_1_DATA_L
0x01	0x2B	R	0x00	ADCINT_DAC_1_DATA_H
0x01	0x2C	R	0x00	ADCINT_REFDAC_1_DATA_L
0x01	0x2D	R	0x00	ADCINT_REFDAC_1_DATA_H
0x01	0x2E	R	0x00	ADCINT_DAC_2_DATA_L
0x01	0x2F	R	0x00	ADCINT_DAC_2_DATA_H
0x01	0x30	R	0x00	ADCINT_DAC_3_DATA_L
0x01	0x31	R	0x00	ADCINT_DAC_3_DATA_H
0x01	0x32	R	0x00	ADCINT_REFDAC_2_DATA_L
0x01	0x33	R	0x00	ADCINT_REFDAC_2_DATA_H
0x01	0x34	R	0x00	ADCINT_SW_0_DATA_L
0x01	0x35	R	0x00	ADCINT_SW_0_DATA_H
0x01	0x36	R	0x00	ADCINT_SW_1_DATA_L
0x01	0x37	R	0x00	ADCINT_SW_1_DATA_H
0x01	0x38	R	0x00	ADCINT_SW_2_DATA_L
0x01	0x39	R	0x00	ADCINT_SW_2_DATA_H
0x01	0x3A	R	0x00	ADCINT_SW_3_DATA_L
0x01	0x3B	R	0x00	ADCINT_SW_3_DATA_H
0x01	0x3C	-	-	RSVD_0X013C

Page/Offset	Address	Type	Default	Register Name
0x01	0x3D	-	-	RSVD_0X013D
0x01	0x3E	-	-	RSVD_0X013E
0x01	0x3F	-	-	RSVD_0X013F
0x01	0x40	R/W	0x00	DAC_0_OVRD_L
0x01	0x41	R/W	0x00	DAC_0_OVRD_H
0x01	0x42	R/W	0x00	DAC_1_OVRD_L
0x01	0x43	R/W	0x00	DAC_1_OVRD_H
0x01	0x44	R/W	0x00	REFDAC_1_OVRD_L
0x01	0x45	R/W	0x00	REFDAC_1_OVRD_H
0x01	0x46	R/W	0x00	DAC_2_OVRD_L
0x01	0x47	R/W	0x00	DAC_2_OVRD_H
0x01	0x48	R/W	0x00	DAC_3_OVRD_L
0x01	0x49	R/W	0x00	DAC_3_OVRD_H
0x01	0x4A	R/W	0x00	REFDAC_2_OVRD_L
0x01	0x4B	R/W	0x00	REFDAC_2_OVRD_H
0x01	0x4C	-	-	RSVD_0X014C
0x01	0x4D	-	-	RSVD_0X014D
0x01	0x4E	-	-	RSVD_0X014E
0x01	0x4F	-	-	RSVD_0X014F
0x01	0x50	R	0x48	GEN_STAT
0x01	0x51	R	0x00	GEN_STAT_1
0x01	0x52	R	0x3D	GEN_STAT_2
0x01	0x53	-	-	RSVD_0X0153
0x01	0x54	-	-	RSVD_0X0154
0x01	0x55	-	-	RSVD_0X0155
0x01	0x56	-	-	RSVD_0X0156
0x01	0x57	-	-	RSVD_0X0157
0x01	0x58	-	-	RSVD_0X0158
0x01	0x59	-	-	RSVD_0X0159
0x01	0x5A	-	-	RSVD_0X015A
0x01	0x5B	-	-	RSVD_0X015B
0x01	0x5C	-	-	RSVD_0X015C

Page/Offset	Address	Type	Default	Register Name
0x01	0x5D	-	-	RSVD_0X015D
0x01	0x5E	-	-	RSVD_0X015E
0x01	0x5F	R/W	0x00	ADC_TRIG
0x01	0x60	R/W	0x00	ADC_MUX_CFG_0
0x01	0x61	R/W	0x00	ADC_AVG
0x01	0x62	R/W	0x00	ADC_CFG
0x01	0x63	R/W	0x09	DAC_SW_EN
0x01	0x64	R/W	0x42	ENABLE_CFG
0x01	0x65	R/W	0x00	PD_DAC
0x01	0x66	R/W	0x00	PD_ADC
0x01	0x67	R/W	0x08	AUTO_CFG
0x01	0x68	R/W	0x01	DEVICE_READY_CFG
0x01	0x69	R/W	0x00	DAC_CFG
0x01	0x6A	R/W	0x00	DAC_CLR_EN
0x01	0x6B	R/W	0x00	DAC_CLR_SRC
0x01	0x6C	R/W	0x00	DAC_LOAD_CAP_SEL
0x02	0x00	R/W	0x00	DAC_0_BASE_L
0x02	0x01	R/W	0x00	DAC_0_BASE_H
0x02	0x02	R/W	0x00	DAC_1_BASE_L
0x02	0x03	R/W	0x00	DAC_1_BASE_H
0x02	0x04	R/W	0x00	DAC_2_BASE_L
0x02	0x05	R/W	0x00	DAC_2_BASE_H
0x02	0x06	R/W	0x00	DAC_3_BASE_L
0x02	0x07	R/W	0x00	DAC_3_BASE_H
0x02	0x08	R/W	0x00	DAC_0_DEL1_0
0x02	0x09	R/W	0x00	DAC_0_DEL3_2
0x02	0x0A	R/W	0x00	DAC_0_DEL5_4
0x02	0x0B	R/W	0x00	DAC_0_DEL7_6
0x02	0x0C	R/W	0x00	DAC_0_DEL9_8
0x02	0x0D	R/W	0x00	DAC_0_DEL11_10
0x02	0x0E	R/W	0x00	DAC_0_DEL13_12
0x02	0x0F	R/W	0x00	DAC_0_DEL15_14

Page/Offset	Address	Type	Default	Register Name
0x02	0x10	R/W	0x00	DAC_0_DEL17_16
0x02	0x11	R/W	0x00	DAC_0_DEL19_18
0x02	0x12	R/W	0x00	DAC_0_DEL21_20
0x02	0x13	R/W	0x00	DAC_0_DEL23_22
0x02	0x14	R/W	0x00	DAC_0_DEL25_24
0x02	0x15	R/W	0x00	DAC_0_DEL27_26
0x02	0x16	R/W	0x00	DAC_0_DEL29_28
0x02	0x17	R/W	0x00	DAC_0_DEL31_30
0x02	0x18	R/W	0x00	DAC_0_DEL33_32
0x02	0x19	R/W	0x00	DAC_0_DEL35_34
0x02	0x1A	R/W	0x00	DAC_0_DEL37_36
0x02	0x1B	R/W	0x00	DAC_0_DEL39_38
0x02	0x1C	R/W	0x00	DAC_0_DEL41_40
0x02	0x1D	R/W	0x00	DAC_0_DEL43_42
0x02	0x1E	R/W	0x00	DAC_0_DEL45_44
0x02	0x1F	R/W	0x00	DAC_0_DEL47_46
0x02	0x20	R/W	0x00	DAC_0_DEL48
0x02	0x21	R/W	0x00	DAC_1_DEL1_0
0x02	0x22	R/W	0x00	DAC_1_DEL3_2
0x02	0x23	R/W	0x00	DAC_1_DEL5_4
0x02	0x24	R/W	0x00	DAC_1_DEL7_6
0x02	0x25	R/W	0x00	DAC_1_DEL9_8
0x02	0x26	R/W	0x00	DAC_1_DEL11_10
0x02	0x27	R/W	0x00	DAC_1_DEL13_12
0x02	0x28	R/W	0x00	DAC_1_DEL15_14
0x02	0x29	R/W	0x00	DAC_1_DEL17_16
0x02	0x2A	R/W	0x00	DAC_1_DEL19_18
0x02	0x2B	R/W	0x00	DAC_1_DEL21_20
0x02	0x2C	R/W	0x00	DAC_1_DEL23_22
0x02	0x2D	R/W	0x00	DAC_1_DEL25_24
0x02	0x2E	R/W	0x00	DAC_1_DEL27_26
0x02	0x2F	R/W	0x00	DAC_1_DEL29_28

Page/Offset	Address	Type	Default	Register Name
0x02	0x30	R/W	0x00	DAC_1_DEL31_30
0x02	0x31	R/W	0x00	DAC_1_DEL33_32
0x02	0x32	R/W	0x00	DAC_1_DEL35_34
0x02	0x33	R/W	0x00	DAC_1_DEL37_36
0x02	0x34	R/W	0x00	DAC_1_DEL39_38
0x02	0x35	R/W	0x00	DAC_1_DEL41_40
0x02	0x36	R/W	0x00	DAC_1_DEL43_42
0x02	0x37	R/W	0x00	DAC_1_DEL45_44
0x02	0x38	R/W	0x00	DAC_1_DEL47_46
0x02	0x39	R/W	0x00	DAC_1_DEL48
0x02	0x3A	R/W	0x00	DAC_2_DEL1_0
0x02	0x3B	R/W	0x00	DAC_2_DEL3_2
0x02	0x3C	R/W	0x00	DAC_2_DEL5_4
0x02	0x3D	R/W	0x00	DAC_2_DEL7_6
0x02	0x3E	R/W	0x00	DAC_2_DEL9_8
0x02	0x3F	R/W	0x00	DAC_2_DEL11_10
0x02	0x40	R/W	0x00	DAC_2_DEL13_12
0x02	0x41	R/W	0x00	DAC_2_DEL15_14
0x02	0x42	R/W	0x00	DAC_2_DEL17_16
0x02	0x43	R/W	0x00	DAC_2_DEL19_18
0x02	0x44	R/W	0x00	DAC_2_DEL21_20
0x02	0x45	R/W	0x00	DAC_2_DEL23_22
0x02	0x46	R/W	0x00	DAC_2_DEL25_24
0x02	0x47	R/W	0x00	DAC_2_DEL27_26
0x02	0x48	R/W	0x00	DAC_2_DEL29_28
0x02	0x49	R/W	0x00	DAC_2_DEL31_30
0x02	0x4A	R/W	0x00	DAC_2_DEL33_32
0x02	0x4B	R/W	0x00	DAC_2_DEL35_34
0x02	0x4C	R/W	0x00	DAC_2_DEL37_36
0x02	0x4D	R/W	0x00	DAC_2_DEL39_38
0x02	0x4E	R/W	0x00	DAC_2_DEL41_40
0x02	0x4F	R/W	0x00	DAC_2_DEL43_42

Page/Offset	Address	Type	Default	Register Name
0x02	0x50	R/W	0x00	DAC_2_DEL45_44
0x02	0x51	R/W	0x00	DAC_2_DEL47_46
0x02	0x52	R/W	0x00	DAC_2_DEL48
0x02	0x53	R/W	0x00	DAC_3_DEL1_0
0x02	0x54	R/W	0x00	DAC_3_DEL3_2
0x02	0x55	R/W	0x00	DAC_3_DEL5_4
0x02	0x56	R/W	0x00	DAC_3_DEL7_6
0x02	0x57	R/W	0x00	DAC_3_DEL9_8
0x02	0x58	R/W	0x00	DAC_3_DEL11_10
0x02	0x59	R/W	0x00	DAC_3_DEL13_12
0x02	0x5A	R/W	0x00	DAC_3_DEL15_14
0x02	0x5B	R/W	0x00	DAC_3_DEL17_16
0x02	0x5C	R/W	0x00	DAC_3_DEL19_18
0x02	0x5D	R/W	0x00	DAC_3_DEL21_20
0x02	0x5E	R/W	0x00	DAC_3_DEL23_22
0x02	0x5F	R/W	0x00	DAC_3_DEL25_24
0x02	0x60	R/W	0x00	DAC_3_DEL27_26
0x02	0x61	R/W	0x00	DAC_3_DEL29_28
0x02	0x62	R/W	0x00	DAC_3_DEL31_30
0x02	0x63	R/W	0x00	DAC_3_DEL33_32
0x02	0x64	R/W	0x00	DAC_3_DEL35_34
0x02	0x65	R/W	0x00	DAC_3_DEL37_36
0x02	0x66	R/W	0x00	DAC_3_DEL39_38
0x02	0x67	R/W	0x00	DAC_3_DEL41_40
0x02	0x68	R/W	0x00	DAC_3_DEL43_42
0x02	0x69	R/W	0x00	DAC_3_DEL45_44
0x02	0x6A	R/W	0x00	DAC_3_DEL47_46
0x02	0x6B	R/W	0x00	DAC_3_DEL48
0x02	0x6C	R/W	0x00	REFDAC_1_DATA_L
0x02	0x6D	R/W	0x00	REFDAC_1_DATA_H
0x02	0x6E	R/W	0x00	REFDAC_2_DATA_L
0x02	0x6F	R/W	0x00	REFDAC_2_DATA_H

Page/Offset	Address	Type	Default	Register Name
0x02	0x70	R/W	0x00	ADC_OFFSET_RT_CAL
0x02	0x71	R/W	0x2A	ADC_RT_CAL
0x03	0x00	R/W	0x00	ALR_CFG_0
0x03	0x01	R/W	0x00	ALR_CFG_1
0x03	0x02	-	-	RSVD_0X0302
0x03	0x03	R/W	0x15	FALSE_ALR_CFG
0x03	0x04	R/W	0xC0	LT_UP_THR_L
0x03	0x05	R/W	0xFF	LT_UP_THR_H
0x03	0x06	R/W	0x00	LT_LO_THR_L
0x03	0x07	R/W	0x00	LT_LO_THR_H
0x03	0x08	R/W	0xC0	RT_UP_THR_L
0x03	0x09	R/W	0xFF	RT_UP_THR_H
0x03	0x0A	R/W	0x00	RT_LO_THR_L
0x03	0x0B	R/W	0x00	RT_LO_THR_H
0x03	0x0C	R/W	0x08	LT_HYST
0x03	0x0D	R/W	0x08	RT_HYST
0x0F	0x00	R/W	0x00	NOTE_PAD0
0x0F	0x01	R/W	0x00	NOTE_PAD1
0x0F	0x02	R/W	0x00	NOTE_PAD2
0x0F	0x03	R/W	0x00	NOTE_PAD3
0x0F	0x04	R/W	0x00	NOTE_PAD4
0x0F	0x05	R/W	0x00	NOTE_PAD5
0x0F	0x06	R/W	0x00	NOTE_PAD6
0x0F	0x07	R/W	0x00	NOTE_PAD7
0x0F	0x08	R/W	0x00	NOTE_PAD8
0x0F	0x09	R/W	0x00	NOTE_PAD9
0x0F	0x0A	R/W	0x00	NOTE_PAD10
0x0F	0x0B	R/W	0x00	NOTE_PAD11
0x0F	0x0C	R/W	0x00	NOTE_PAD12
0x0F	0x0D	R/W	0x00	NOTE_PAD13
0x0F	0x0E	R/W	0x00	NOTE_PAD14
0x0F	0x0F	R/W	0x00	NOTE_PAD15

Page/Offset	Address	Type	Default	Register Name
0x0F	0x10	R/W	0x00	NOTE_PAD16
0x0F	0x11	R/W	0x00	NOTE_PAD17
0x0F	0x12	R/W	0x00	NOTE_PAD18
0x0F	0x13	R/W	0x00	NOTE_PAD19
0x11	0x01	R/W	0x00	EEPROM_CFG

9.1 Temperature Sensor Conversion Results Registers: Page 0x01, Address 0x00 – 0x03

9.1.1. Local Temperature Sensor Data (High Byte) Register

Address = 0x00, Default value = 0x40

Table 41. Local Temperature Sensor Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LT_DATA_H	R	All zeros	8-bit MSB nibble of the 12-bit local temperature sensor conversion result.

9.1.2. Local Temperature Sensor Data (Low Byte) Register

Address = 0x01, Default value = 0x00

Table 42. Local Temperature Sensor Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LT_DATA_L	R	All zeros	8-bit LSB byte of the 12-bit local temperature sensor conversion result.

9.1.3. Remote Temperature Sensor Data (High Byte) Register

Address = 0x02, Default value = 0x40

Table 43. Remote Temperature Sensor Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RT_DATA_H	R	All zeros	8-bit LSB byte of the 12-bit remote temperature sensor conversion result.

9.1.4. Remote Temperature Sensor Data (Low Byte) Register

Address = 0x03, Default value = 0x00

Table 44. IS_B Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	All zeros	Reserved bit.
3:0	RT_DATA_L	R	All zeros	4-bit MSB nibble of the 12-bit remote temperature sensor conversion result.

9.2 Interface Configuration: Page 0x01, Address 0x04

9.2.1. Interface Configuration 0 Register

Address 0x04, Default value = 0x40

Table 45. Interface Config 0 Register Field Descriptions (R/W)

Bit	Field	Type	Default	Description
7	SINGLE_INSTR	R/W	-	Single instruction enable (SPI only) 0 = streaming mode (default) 1 = single instruction
6	ADDR_ASCEND	R/W	-	Address Ascend 0 = Descend – decrements address while streaming (offset wrap from 0x00 to 0x7D in the same page in both 2B and 1B addressing mode) 1 = Ascend – increments address while streaming (offset wrap from 0x7D to 0x00 in the same page in both 2B and 1B addressing mode)
5	ADDR_MODE	R/W	-	Addressing mode 0 = 1 byte addressing (default) 1 = 2 bytes addressing
4	RSVD_4	R	-	Reserved for factory use.
3	READBACK	R/W	-	Read back 0 = DAC read back from active registers (default) 1 = DAC read back from buffer registers
2:0	RSVD_2_0	R	-	Reserved for factory use.

9.2.2. Soft Reset Register

Address 0x07, Default value = 0x00

Table 46. Device Config Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SOFT_RESET	W	All zeros	Soft reset (self-clearing) 0x05: software reset

9.2.3. Temperature Configuration Register

Address 0x08, Default value = 0x04

Table 47. Temperature Config Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	Reserved	R/W	All zeros	Reserved for factory use.
2	Range	R/W	1	Temperature data format: 0 = Normal range. 1 = Extended range.
1:0	Reserved	R/W	00	Reserved for factory use.

9.2.4. LUT Configuration Register

Address 0x0A, Default value = 0x03

Table 48. LUT Config Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	Reserved	R	0	Reserved for factory use.
5	LUTSTAT	R	0	Reports the status of the LUT: 0 = LUT is disabled. 1 = LUT is enabled.
4	LUTDIS	R/W	0	Disable the LUT from calculating new DAC values: 0 = LUT is enabled. 1 = LUT is disabled. This bit cannot be burned to EEPROM.
3	LUTSEL2	R/W	0	Select temperature sensor used for LUT 2/3: 0 = LT sensor. 1 = RT sensor.
2	LUTSEL1	R/W	0	Select temperature sensor used for LUT 0/1: 0 = LT sensor 1 = RT sensor
1	RT_EN	R/W	1	Remote temperature sensor enable: 0 = disable conversion of RT 1 = enable conversion of RT
0	LT_EN	R/W	1	Local temperature sensor enable: 0 = disable conversion of LT 1 = enable conversion of LT

9.3 Device Identification: Page 0x01, Address 0x0B – 0x10

9.3.1. Chip Type Register

Address 0x0B, Default value = 0x08

Table 49. Chip Type Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	CHIP-VARIANT	R	0x0	Identifies which variant of the device has been implemented.
3:0	CHIP-TYPE	R	0x8	Identifies the device as a precision analog monitor and control

9.3.2. Chip ID Low Byte Register

Address 0x0C, Default value = 0x49

Table 50. Chip ID Low Byte Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CHIPID-LOW	R	0x49	Chip ID. Low byte.

9.3.3. Chip ID High Byte Register

Address 0x0D, Default value = 0x0C

Table 51. Chip ID High Byte Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CHIPID-HIGH	R	0x0C	Chip ID. High byte.

9.3.4. Chip Version

Address = 0x0E, Default value = 0x00

Table 52. Version ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VERSIONID	R	0x00	F39510 version ID. Subject to change.

9.3.5. Manufacturer ID Low Byte Register

Address = 0x0F, Default value = 0xCC

Table 53. Manufacturer ID Low Byte Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	MAN_ID-LOW	R	0xCC	Manufacturer ID. Low byte.
0	Reserved	R	0x0	Reserved for factory use.

9.3.6. Manufacturer ID High Byte Register

Address = 0x10, Default value = 0x04

Table 54. Manufacturer ID High Byte Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MAN_ID-HIGH	R	0x04	Manufacturer ID. High byte.

9.4 LUT EEPROM Control Register: Page 0x01, Address 0x11

9.4.1. LUT EEPROM Control Register

Address = 0x11, Default value = 0x00

Table 55. Register Update Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CMD STATUS	R/W	All zeros	This register has multiple functions depending on the selected operation mode as described in the following list: ▪ Write operation: 7:0 COMMAND. Instruction to BURN EEPROM or TRANSFER EEPROM content to EEPROM Controller. 0x5E: TRANSFER data from EEPROM to EEROM Controller. 0xE5: BURN EEPROM. ▪ Read operation: 7:3 Reserved. 2 UCOR. 1 = More than one bit error was detected during the TRANSFER, and correction was not possible. 0 = No uncorrected errors were detected during the TRANSFER. [1] COR. 1 = A bit error was detected and corrected during the TRANSFER. 0 = No errors detected during the TRANSFER. 0 RDBY. 1 = BURN or TRANSFER in progress. 0 = BURN or TRANSFER completed.

9.5 Register Update: Page 0x01, Address 0x012

9.5.1. Register Update Register

Address = 0x012, Default value = 0x00

Table 56. Register Update Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	Reserved	R	00	Reserved bit.
5	DAC_IN_UPDATE	W	0	When set transfers the latest DACIN data from ALU to the DAC_OVRD Data registers and the latest Temperature value (sensor or register) to the TEMP_OVRD Data register.
4	ADC_UPDATE	W	0	When set transfers the latest ADC and temperature conversion data to the ADC and Temperature Data registers. This function is needed when operating the ADC in auto-mode.
3:2	Reserved	R	00	Reserved bit.
1	TEMP_UPDATE	W	0	Temperature Override register update (self-clearing). 0 = disabled. 1 = enabled – transfers data from buffer to active register (Temperature Override registers only).
0	DAC_UPDATE	W	0	DAC update (self-clearing). 0 = disabled. 1 = enabled – transfers data from buffers to active registers (DAC registers only).

9.6 ADC MUX Configuration: Page 0x01, Address 0x13 – 0x14

9.6.1. ADC MUX Configuration Register

Address = 0x13, Default value = 0x00

Table 57. ADC Mux Configuration Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RSVD_7_2	R	-	Reserved bit.
1	ADC_IN1	R/W	-	When set to 1 the corresponding analog input channel ADC_IN1 is accessed during an ADC conversion cycle. When cleared to 0 the corresponding input channel ADC_IN1 is ignored during an ADC conversion cycle.
0	ADC_IN0	R/W	-	When set to 1 the corresponding analog input channel ADC_IN0 is accessed during an ADC conversion cycle. When cleared to 0 the corresponding input channel ADC_IN0 is ignored during an ADC conversion cycle.

9.6.2. ADC MUX FETDRV Monitor Configuration Register

Address = 0x14, Default value = 0x00

Table 58. ADC Mux Configuration 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD_7	R	0	Reserved bit.
6	ADCINT_SW_3	R/W	0	When set to 1, the corresponding internal bipolar channel OUT_2 is accessed during an ADC conversion cycle. When cleared to 0, the corresponding internal bipolar channel OUT_2 is ignored during an ADC conversion cycle.
5	ADCINT_SW_2	R/W	-	When set to 1 the corresponding internal bipolar channel DAC_3 is accessed during an ADC conversion cycle. When cleared to 0 the corresponding internal bipolar channel DAC_3 is ignored during an ADC conversion cycle.
4:3	RSVD_4_3	R	00	Reserved bit.
2	ADCINT_SW_1	R/W	0	When set to 1, the corresponding internal bipolar channel OUT_1 is accessed during an ADC conversion cycle. When cleared to 0, the corresponding internal bipolar channel OUT_1 is ignored during an ADC conversion cycle.
1	ADCINT_SW_0	R/W	0	When set to 1, the corresponding internal bipolar channel DAC_0 is accessed during an ADC conversion cycle. When cleared to 0, the corresponding internal bipolar channel DAC_0 is ignored during an ADC conversion cycle.
0	RSVD_0	R	0	Reserved bit.

9.7 Alarm Status Registers: Page 0x01, Address 0x17 – 0x18

9.7.1. Alarm Status 0 Register

Address = 0x17, Default value = 0x00

Table 59. Alarm Status 0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	S0S1_ERR_ALR	R	0	S0/S1 error types status bit.
6	PAR_ERR_ALR	R	0	Parity check error status bit.
5	RT_HIGH_ALR	R	0	RT-HIGH-ALR = 1 when the remote temperature sensor is out of the range defined by the upper threshold.
4	RT_LOW_ALR	R	0	RT-LOW-ALR = 1 when the remote temperature sensor is out of the range defined by the lower threshold.
3:0	RSVD_3_0	R	-	Reserved bit.

9.7.2. Alarm Status 1 Register

Address = 0x18, Default value = 0x00

Table 60. Alarm Status 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	DAV_ALR	R	0	ADC Data available status bit.
6:3	RSVD_6_3	R	0	Reserved bit.
2	THERM_ALR	R	0	Thermal alarm flag. When the die temperature is equal to or greater than +150°C, the bit is set (1) and the THERM-ALR flag activates. The on-chip temperature sensor (LT) monitors the die temperature. If LT is disabled, the THERM-ALR bit is always 0. The hysteresis of this alarm is 8°C.
1	LT_HIGH_ALR	R	0	LT-HIGH-ALR = 1 when the local temperature sensor is out of the range defined by the upper threshold.
0	LT_LOW_ALR	R	0	LT-LOW-ALR = 1 when the local temperature sensor is out of the range defined by the lower threshold.

9.8 DAC Clear Register: Page 0x01

Address = 0x19, Default value = 0x00

Table 61. DAC Clear Register Field Descriptions

Bit	Field	Type	Default	Description
7	CLR_REFDAC2	R/W	0	If CLR_REFDAC2 = 1, DAC_REFDAC2 is forced into a clear state. If CLR_REFDAC2 = 0, DAC_REFDAC2 is restored to normal operation.
6	CLR_DAC_3	R/W	0	If CLR_3 = 1, DAC_3 is forced into a clear state. If CLR_3 = 0, DAC_3 is restored to normal operation.
5	CLR_DAC_2	R/W	0	If CLR_2 = 1, DAC_2 is forced into a clear state. If CLR_2 = 0, DAC_2 is restored to normal operation.
4	RSVD_4	R	0	Reserved bit.
3	CLR_REFDAC1	R/W	0	If CLR_REFDAC1 = 1, DAC_REFDAC1 is forced into a clear state. If CLR_REFDAC1 = 0, DAC_REFDAC1 is restored to normal operation.
2	CLR_DAC_1	R/W	0	If CLR_1 = 1, DAC_1 is forced into a clear state. If CLR_1 = 0, DAC_1 is restored to normal operation.
1	CLR_DAC_0	R/W	0	If CLR_0 = 1, DAC_0 is forced into a clear state. If CLR_0 = 0, DAC_0 is restored to normal operation.
0	RSVD_0	R	0	Reserved bit.

9.9 Override Control Register: Page 0x01

Address = 0x1A, Default value = 0x00

Table 62. Override Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	REFDAC_2_OC	R/W	0	REFDAC_2 override enable bit: 0 = REFDAC_2 input generated by LUT 1 = REFDAC_2 input is supplied from user accessible registers REFDAC_2_OVRD_L/M.
6	DAC_3_OC	R/W	0	DAC_3 override enable bit: 0 = DAC_3 input generated by LUT 1 = DAC_3 input is supplied from user accessible registers DAC_3_OVRD_L/M.
5	DAC_2_OC	R/W	0	DAC_2 override enable bit: 0 = DAC_2 input generated by LUT 1 = DAC_2 input is supplied from user accessible registers DAC_2_OVRD_L/M.
4	RSVD_4	R		Reserved bit.
3	REFDAC_1_OC	R/W	0	REFDAC_1 override enable bit: 0 = REFDAC_1 input generated by LUT 1 = REFDAC_1 input is supplied from user accessible registers REFDAC_1_OVRD_L/M.
2	DAC_1_OC	R/W	0	DAC_1 override enable bit: 0 = DAC_1 input generated by LUT 1 = DAC_1 input is supplied from user accessible registers DAC_1_OVRD_L/M.
1	DAC_0_OC	R/W	0	DAC_0 override enable bit: 0 = DAC_0 input generated by LUT 1 = DAC_0 input is supplied from user accessible registers DAC_0_OVRD_L/M.
0	TEMP_OC	R/W	0	TEMP override enable bit: 0 = TEMP input generated by Temperature Sensor 1 = TEMP input is supplied from user accessible registers TEMP_OVRD.

9.10 Temperature Sensor 1 Override Data (Low Byte): Page 0x01

Address = 0x1B, Default value = 0x00

Table 63. Temperature Sensor Override Low Byte Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TEMP_OVRD_1_L	R/W	All Zeros	8-bit LSB byte (right aligned format) or trailing zeros padded nibble (left aligned format) of the 12-bit Temperature Sensor 1 override input word.

9.11 Temperature Sensor 1 Override Data (High Byte): Page 0x01

Address = 0x1C, Default value = 0x00

Table 64. Temperature Sensor Override High Byte Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TEMP_OVRD_1_H	R	All Zeros	8-bit MSB byte (left aligned format) or leading zeros padded nibble (right aligned format) of the 12-bit Temperature Sensor 1 override input word.

9.12 Temperature Sensor 2 Override Data (Low Byte): Page 0x01

Address = 0x1D, Default value = 0x00

Table 65. Temperature Sensor Override Low Byte Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TEMP_OVRD_2_L	R/W	All Zeros	8-bit LSB byte (right aligned format) or trailing zeros padded nibble (left aligned format) of the 12-bit Temperature Sensor 2 override input word.

9.13 Temperature Sensor 2 Override Data (High Byte): Page 0x01

Address = 0x1E, Default value = 0x00

Table 66. Temperature Sensor Override High Byte Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TEMP_OVRD_2_H	R	All Zeros	8-bit MSB byte (left aligned format) or leading zeros padded nibble (right aligned format) of the 12-bit Temperature Sensor 2 override input word.

9.14 Vendor ID Register: Page 0x01

Address = 0x1F, Default value = 0xB3

Table 67. Vendor ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VENDOR_ID	R	00001011	F39510 Vendor ID.

9.15 ADC_IN0 Data (Low Byte) Register: Page 0x01, Address 0x20

Address = 0x20, Default value = 0x00

Table 68. ADC_IN0 Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADC_IN0_DATA_L	R	All zeros	8-bit LSB byte of the 12-bit ADC_IN0 conversion result.

9.16 ADC_IN0 Data (High Byte) Register: Page 0x01, Address 0x21

Address = 0x21, Default value = 0x00

Table 69. ADC_IN1 Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	-	Reserved bit.
3:0	ADC_IN0_DATA_H	R	All zeros	8-bit LSB byte of the 12-bit ADC_IN0 conversion result.

9.17 ADC_IN1 Data (Low Byte) Register: Page 0x01, Address 0x22

Address = 0x22, Default value = 0x00

Table 70. ADC_IN1 Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADC_IN1_DATA_L	R	All zeros	8-bit LSB byte of the 12-bit ADC_IN1 conversion result.

9.18 ADC_IN1 Data (High Byte) Register: Page 0x01, Address 0x23

Address = 0x23, Default value = 0x00

Table 71. ADC_IN1 Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	-	Reserved bit.
3:0	ADC_IN1_DATA_H	R	All zeros	8-bit LSB byte of the 12-bit ADC_IN1 conversion result.

9.19 Local Temperature Data (Low Byte) Register: Page 0x01, Address 0x24

Address = 0x24, Default value = 0x00

Table 72. Local Temperature (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADC_LT_DATA_L	R	-	8-bit MSB byte (left aligned format) or leading zeros padded nibble (right aligned format) of the 12-bit local temperature sensor conversion result. Reading first this byte causes the lock of low byte register (recommended for proper operation).

9.20 Local Temperature Data (High Byte) Register: Page 0x01, Address 0x25

Address = 0x25, Default value = 0x40

Table 73. Local Temperature (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADC_LT_DATA_H	R	-	8-bit LSB byte (right aligned format) or trailing zeros padded nibble (left aligned format) of the 12-bit local temperature sensor conversion result. Reading first this byte causes the lock of high byte register.

9.21 Remote Temperature Data (Low Byte) Register: Page 0x01, Address 0x26

Address = 0x26, Default value = 0x00

Table 74. Local Temperature (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADC_RT_DATA_L	R	-	8-bit MSB byte (left aligned format) or leading zeros padded nibble (right aligned format) of the 12-bit remote temperature sensor conversion result. Reading this byte causes the lock of low byte register (recommended for proper operation).

9.22 Remote Temperature Data (High Byte) Register: Page 0x01, Address 0x27

Address = 0x27, Default value = 0x40

Table 75. Local Temperature (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADC_RT_DATA_H	R	-	8-bit LSB byte (right aligned format) or trailing zeros padded nibble (left aligned format) of the 12-bit remote temperature sensor conversion result. Reading first this byte causes the lock of high byte register.

9.23 ADC Internal Conversion Results Registers: Page 0x01, Address 0x28 – 0x33

9.23.1. ADCINT_0 Data (Low Byte) Register

Address = 0x28, Default value = 0x00

Table 76. ADCINT_0 Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADCINT_DAC_0_DATA_L	R	All zeros	8-bit LSB byte of the 12-bit ADCINT_0 conversion result.

9.23.2. ADCINT_0 Data (High Byte) Register

Address = 0x29, Default value = 0x00

Table 77. ADCINT_0 Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	All zeros	Reserved bit.
3:0	ADCINT_DAC_0_DATA_H	R	All zeros	4-bit MSB nibble of the 12-bit ADCINT_0 conversion result.

9.23.3. ADCINT_1 Data (Low Byte) Register

Address = 0x2A, Default value = 0x00

Table 78. ADCINT_1 Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADCINT_DAC_1_DATA_L	R	All zeros	8-bit LSB byte of the 12-bit ADCINT_1 conversion result.

9.23.4. ADCINT_1 Data (High Byte) Register

Address = 0x2B, Default value = 0x00

Table 79. ADCINT_1 Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	All zeros	Reserved bit.
3:0	ADCINT_DAC_1_DATA_H	R	All zeros	4-bit MSB nibble of the 12-bit ADCINT_1 conversion result.

9.23.5. ADCINT_REFDAC1 Data (Low Byte) Register

Address = 0x2C, Default value = 0x00

Table 80. ADCINT_REFDAC1 Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADCINT_REFDAC1_DATA_L	R	All zeros	8-bit LSB byte of the 12-bit ADCINT_REFDAC1 conversion result.

9.23.6. ADCINT_REFDAC1 Data (High Byte) Register

Address = 0x2D, Default value = 0x00

Table 81. ADCINT_REFDAC1 Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	All zeros	Reserved bit.
3:0	ADCINT_REFDAC1_DATA_H	R	All zeros	4-bit MSB nibble of the 12-bit ADCINT_REFDAC1 conversion result.

9.23.7. ADCINT_2 Data (Low Byte) Register

Address = 0x2E, Default value = 0x00

Table 82. ADCINT_2 Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADCINT_DAC_2_DATA_L	R	All zeros	8-bit LSB byte of the 12-bit ADCINT_2 conversion result.

9.23.8. ADCINT_2 Data (High Byte) Register

Address = 0x2F, Default value = 0x00

Table 83. ADCINT_2 Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	All zeros	Reserved bit.
3:0	ADCINT_DAC_2_DATA_H	R	All zeros	4-bit MSB nibble of the 12-bit ADCINT_2 conversion result.

9.23.9. ADCINT_3 Data (Low Byte) Register

Address = 0x30, Default value = 0x00

Table 84. ADCINT_3 Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADCINT_DAC_3_DATA_L	R	All zeros	8-bit LSB byte of the 12-bit ADCINT_3 conversion result.

9.23.10. ADCINT_3 Data (High Byte) Register

Address = 0x31, Default value = 0x00

Table 85. ADCINT_3 Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	All zeros	Reserved bit.
3:0	ADCINT_DAC_3_DATA_H	R	All zeros	4-bit MSB nibble of the 12-bit ADCINT_3 conversion result.

9.23.11. ADCINT_REFDAC2 Data (Low Byte) Register

Address = 0x32, Default value = 0x00

Table 86. ADCINT_REFDAC2 Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADCINT_REFDAC2_DATA_L	R	All zeros	8-bit LSB byte of the 12-bit ADCINT_REFDAC2 conversion result.

9.23.12. ADCINT_REFDAC2 Data (High Byte) Register

Address = 0x33, Default value = 0x00

Table 87. ADCINT_REFDAC2 Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	All zeros	Reserved bit.
3:0	ADCINT_REFDAC2_DATA_H	R	All zeros	4-bit MSB nibble of the 12-bit ADCINT_REFDAC2 conversion result.

9.24 ADC Internal SW Monitoring Registers: Page 0x01, Address 0x34 – 0x3B

9.24.1. ADC Internal SW 0 Monitoring Data (Low Byte) Register

Address = 0x34, Default value = 0x00

Table 88. ADC Internal SW 0 Monitoring Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADCINT_SW_0_DATA_L	R	All zeros	8-bit LSB byte of the 12-bit ADCINT_SW_0 conversion result.

9.24.2. ADC Internal SW 0 Monitoring Data (High Byte) Register

Address = 0x35, Default value = 0x00

Table 89. ADC Internal SW 0 Lower-Threshold (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	All zeros	Reserved bit.
3:0	ADCINT_SW_0_DATA_H	R	All zeros	4-bit MSB nibble of the 12-bit ADCINT_SW_0 conversion result.

9.24.3. ADC Internal SW 1 Monitoring Data (Low Byte) Register

Address = 0x36, Default value = 0x00

Table 90. ADC Internal SW 1 Monitoring Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADCINT_SW_1_DATA_L	R	All zeros	8-bit LSB byte of the 12-bit ADCINT_SW_1 conversion result.

9.24.4. ADC Internal SW 1 Monitoring Data (High Byte) Register

Address = 0x37, Default value = 0x00

Table 91. ADC Internal SW 1 Lower-Threshold (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	All zeros	Reserved bit.
3:0	ADCINT_SW_1_DATA_H	R	All zeros	4-bit MSB nibble of the 12-bit ADCINT_SW_1 conversion result.

9.24.5. ADC Internal SW 2 Monitoring Data (Low Byte) Register

Address = 0x38, Default value = 0x00

Table 92. ADC Internal SW 2 Monitoring Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADCINT_SW_2_DATA_L	R	All zeros	8-bit LSB byte of the 12-bit ADCINT_SW_2 conversion result.

9.24.6. ADC Internal SW 1 Monitoring Data (High Byte) Register

Address = 0x39, Default value = 0x00

Table 93. ADC Internal SW 2 Lower-Threshold (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	All zeros	Reserved bit.
3:0	ADCINT_SW_2_DATA_H	R	All zeros	4-bit MSB nibble of the 12-bit ADCINT_SW_2 conversion result.

9.24.7. ADC Internal SW 3 Monitoring Data (Low Byte) Register

Address = 0x3A, Default value = 0x00

Table 94. ADC Internal SW 3 Monitoring Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADCINT_SW_3_DATA_L	R	All zeros	8-bit LSB byte of the 12-bit ADCINT_SW_3 conversion result.

9.24.8. ADC Internal SW 3 Monitoring Data (High Byte) Register

Address = 0x3B, Default value = 0x00

Table 95. ADC Internal SW 3 Lower-Threshold (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	All zeros	Reserved bit.
3:0	ADCINT_SW_3_DATA_H	R	All zeros	4-bit MSB nibble of the 12-bit ADCINT_SW_3 conversion result.

9.25 DAC Input Override Registers: Page 0x01, Address 0x40 – 0x4B

9.25.1. DAC_0_OVRD_L Data (Low Byte) Register

Address = 0x40, Default value = 0x00

Table 96. DAC_0_OVRD_L Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DAC_0_OVRD_L	R/W	All zeros	8-bit LSB byte to be loaded to the DAC_0.

9.25.2. DAC_0_OVRD_H (High Byte) Register

Address = 0x41, Default value = 0x00

Table 97. DAC_0_OVRD_H Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	All zeros	Reserved bit.
3:0	DAC_0_OVRD_H	R/W	All zeros	4-bit MSB nibble to be loaded to the DAC_0.

9.25.3. DAC_1_OVRD_L Data (Low Byte) Register

Address = 0x42, Default value = 0x00

Table 98. DAC_1_OVRD_L Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DAC_1_OVRD_L	R/W	All zeros	8-bit LSB byte to be loaded to the DAC_1.

9.25.4. DAC_1_OVRD_H (High Byte) Register

Address = 0x43, Default value = 0x00

Table 99. DAC_1_OVRD_H Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	All zeros	Reserved bit.
3:0	DAC_1_OVRD_H	R/W	All zeros	4-bit MSB nibble to be loaded to the DAC_1.

9.25.5. REFDAC_1_OVRD_L Data (Low Byte) Register

Address = 0x44, Default value = 0x00

Table 100. REFDAC_1_OVRD_L Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	REFDAC_1_OVRD_L	R/W	All zeros	8-bit LSB byte to be loaded to the REFDAC_1.

9.25.6. REFDAC_1_OVRD_H (High Byte) Register

Address = 0x45, Default value = 0x00

Table 101. REFDAC_1_OVRD_H Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	All zeros	Reserved bit.
3:0	REFDAC_1_OVRD_H	R/W	All zeros	4-bit MSB nibble to be loaded to the REFDAC_1.

9.25.7. DAC_2_OVRD_L Data (Low Byte) Register

Address = 0x46, Default value = 0x00

Table 102. DAC_2_OVRD_L Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DAC_2_OVRD_L	R/W	All zeros	8-bit LSB byte to be loaded to the DAC_2.

9.25.8. DAC_2_OVRD_H (High Byte) Register

Address = 0x47, Default value = 0x00

Table 103. DAC_2_OVRD_H Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	All zeros	Reserved bit.
3:0	DAC_2_OVRD_H	R/W	All zeros	4-bit MSB nibble to be loaded to the DAC_2.

9.25.9. DAC_3_OVRD_L Data (Low Byte) Register

Address = 0x48, Default value = 0x00

Table 104. DAC_3_OVRD_L Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DAC_3_OVRD_L	R/W	All zeros	8-bit LSB byte to be loaded to the DAC_3.

9.25.10. DAC_3_OVRD_H (High Byte) Register

Address = 0x49, Default value = 0x00

Table 105. DAC_3_OVRD_H Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	All zeros	Reserved bit.
3:0	DAC_3_OVRD_H	R/W	All zeros	4-bit MSB nibble to be loaded to the DAC_3.

9.25.11. REFDAC_2_OVRD_L Data (Low Byte) Register

Address = 0x4A, Default value = 0x00

Table 106. REFDAC_2_OVRD_L Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	REFDAC_2_OVRD_L	R/W	All zeros	8-bit LSB byte to be loaded to the REFDAC_1.

9.25.12. REFDAC_2_OVRD_H (High Byte) Register

Address = 0x4B, Default value = 0x00

Table 107. DAC_1_OVRD_H Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R	All zeros	Reserved bit.
3:0	REFDAC_2_OVRD_H	R/W	All zeros	4-bit MSB nibble to be loaded to the REFDAC_1.

9.26 General Status Registers: Page 0x01, Address 0x50 – 0x52

9.26.1. General Status Register

Address = 0x50, Default value = 0x48

Table 108. General Status Register Field Descriptions

Bit	Field	Type	Default	Description
7	IBI_PEND	R	0	Device event In Band Interrupt (IBI) status. 0 = No pending IBI. 1 = Pending IBI.
6	IBI_ENABLE	R	1	In Band Interrupt Enable (Applicable only in I3C mode) 0 = Disable. 1 = Enable.
5	RSVD_5	R	0	Reserved bit.
4	AVSS	R	0	This bit is the auto-range detection output for the DACs. This bit is set to 1 when AVSS < AVSSTH (-10 to 0V output range), and 0 when AVSS > AVSSTH (0 to 5V output range).
3	ADC_IDLE	R	1	ADC Idle indicator. Auto mode: 1 by default; goes to 0 once the ADC is triggered and is running. Remains 0 until ADC is stopped, then ADC_IDLE returns to 1. Direct mode: 1 by default; goes to 0 once the ADC is triggered and direct conversions are running and returns to 1 when direct mode conversions are completed.
2	I3C_MODE	R	0	Interface selection. 0 = I^2C protocol (maximum speed of 1MHz). 1 = I3C basic protocol.
1	GALR	R	0	Global alarm bit. This bit is the OR function or all individual alarm bits of the status register. This bit is set to 1 when any alarm condition occurs and remains set until the status register is read. This bit is cleared after reading the Status Register.
0	DAVF	R	0	ADC Data available flag bit. Direct mode only. Always cleared in Auto mode. 0 = ADC conversion is in progress or ADC is in Auto mode. 1 = ADC conversions are complete and new data is available.

9.26.2. General Status 1 Register

Address = 0x51, Default value = 0x00

Table 109. General Status 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	DEVICE_READY	R	0	Status of DEVICE_READY.
6:1	RSVD_6_2	R	All zeros	Reserved bit.
0	AVCC	R	0	Auto-range detection output of the positive analog power for the DACs. This bit is set to 1 when AVCC > AVCCTH (10V), and 0 when AVCC < AVCCTH (5V).

9.26.3. General Status 2 Register

Address = 0x52, Default value = 0x3D

Table 110. General Status 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RSVD_7_5	R	All zeros	Reserved bit.
4	AVSS_OK	R	1	Status of AVSS. This bit is set to 1 when AVSS < AVSSTH and 0 when AVSS > AVSSTH.
3	AVCC_OK	R	1	Status of AVCC. This bit is set to 1 when AVSS > AVCCTH, and 0 when AVSS < AVCCTH.
2	IOVDD_OK	R	1	Status of IOVDD. This bit is set to 1 when IOVDD > IOVDDTH, and 0 when IOVDD < IOVDDTH.
1	RSVD_1	R	0	Reserved bit.
0	AVDD_OK	R	1	Status of AVDD. This bit is set to 1 when AVDD > AVDDTH and 0 when AVDD < AVDDTH.

9.27 ADC Trigger: Page 0x01

Address = 0x5F, Default value = 0x00

Table 111. ADC Trigger Hysteresis Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	RSVD_7_1	R	All zeros	Reserved bit.
0	ICONV	R/W	0	Internal ADC conversion bit. Set this bit to 1 to start the ADC conversion internally. The bit is automatically cleared to 0 after the ADC conversion starts.

9.28 ADC MUX DAC Monitor Configuration Register: Page = 0x01

Address = 0x60, Default value = 0x00

Table 112. ADC Mux Configuration Register Field Descriptions

Bit	Field	Type	Default	Description
7	ADCINT_REFDAC2	R/W	0	When set to 1, the corresponding internal bipolar channel DAC_REFDAC2 is accessed during an ADC conversion cycle. When cleared to 0, the corresponding internal bipolar channel DAC_REFDAC2 is ignored during an ADC conversion cycle.
6	ADCINT_DAC3	R/W	0	When set to 1, the corresponding internal bipolar channel DAC_3 is accessed during an ADC conversion cycle. When cleared to 0, the corresponding internal bipolar channel DAC_3 is ignored during an ADC conversion cycle.
5	ADCINT_DAC2	R/W	0	When set to 1, the corresponding internal bipolar channel DAC_2 is accessed during an ADC conversion cycle. When cleared to 0, the corresponding internal bipolar channel DAC_2 is ignored during an ADC conversion cycle.
4	RSVD_4	R/W	0	Reserved bit.

Bit	Field	Type	Default	Description
3	ADCINT_REFDAC1	R/W	0	When set to 1, the corresponding internal bipolar channel DAC_REFDAC1 is accessed during an ADC conversion cycle. When cleared to 0, the corresponding internal bipolar channel DAC_REFDAC1 is ignored during an ADC conversion cycle.
2	ADCINT_DAC1	R/W	0	When set to 1, the corresponding internal bipolar channel DAC_1 is accessed during an ADC conversion cycle. When cleared to 0, the corresponding internal bipolar channel DAC_1 is ignored during an ADC conversion cycle.
1	ADCINT_DAC0	R/W	0	When set to 1, the corresponding internal bipolar channel DAC_0 is accessed during an ADC conversion cycle. When cleared to 0, the corresponding internal bipolar channel DAC_0 is ignored during an ADC conversion cycle.
0	RSVD_0	R/W	0	Reserved bit.

9.29 ADC Average Count Register: Page = 0x01

Address = 0x61, Default value = 0x00

Table 113. ADC Average Count Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RSVD_7_3	R/W	All zeros	Reserved bit.
2:0	ADC_AVG_ADC	R/W	All zeros	Average length in 2^n format (1, 2, 4, 8, 16, 32, 64, 128).

9.30 ADC Configuration Register: Page = 0x01

Address = 0x62, Default value = 0x00

Table 114. ADC Configuration Register Field Descriptions

Bit	Field	Type	Default	Description
7	CMODE	R/W	0	ADC Conversion Mode Bit. This bit selects the ADC conversion mode. 0 = Direct mode. The analog inputs specified in the ADC channel registers are converted sequentially one time. When one set of conversions is complete, the ADC is idle and waits for a new trigger. 1 = Auto mode. The analog inputs specified in the ADC channel registers are converted sequentially and repeatedly. When one set of conversions is complete, the ADC multiplexer returns to the first channel and repeats the process. The ADC-UPDATE bit in register 0x0F must be used to initiate the transfer of the latest conversion data to the ADC Data registers.
6:5	ADC_CONV_RATE	R/W	All zeros	ADC Conversion rate. Bipolar channel update time (µs): 00 = 21.2 01 = 21.2 10 = 21.2 11 = 42.5

Bit	Field	Type	Default	Description
4	ADC_REF_BUFF	R/W	0	ADC Reference Buffer bit. This bit must be set to 1 after device power-up to enable the internal reference buffer driving the ADC. 0 = ADC reference buffer is disabled 1 = ADC reference buffer is enabled
3:2	RSVD_3_2	R/W	00	Reserved bits.
1:0	RT_CONV_RATE	R/W	00	ADC Conversion rate. Remote Temperature Sensor channel update time (µs): 00 = 250 01 = 500 10 = 1000 11 = 2000

9.31 Switch Control Register: Page = 0x01

Address = 0x63, Default value = 0x09

This register is used in to control the DAC switches bypassing the Enable1/Enable2 pins.
Reset by: Power-on, Hardware Reset

Table 115. Switch Control Register Field Descriptions

Bit	Field	Type	Default	Description
6:4	RSVD_7_4	R/W	0000	Reserved bits.
3	DAC_3_SW_EN	R/W	1	DAC_3 Switch enable bit. 0 = REFDAC_2 output 1 = DAC_3 output
2	DAC_2_SW_EN	R/W	0	DAC_2 Switch enable bit. 0 = REFDAC2 output 1 = OUT_2 output
1	DAC_1_SW_EN	R/W	0	DAC_1 Switch enable bit. 0 = REFDAC_1 output 1 = OUT_1 output
0	DAC_0_SW_EN	R/W	1	DAC_0 Switch enable bit. 0 = REFDAC_1 output 1 = DAC_0 output

9.32 Enable Configuration: Page = 0x01

Address = 0x64, Default value = 0x42

Table 116. Enable1/ Enable 2 Configuration Register Field Descriptions

Bit	Field	Type	Default	Description
7	DAC_3_SW_EN2	R/W	0	When set DAC_3_SW switch is controlled by ENABLE_2.
6	DAC_2_SW_EN2	R/W	1	When set DAC_2_SW switch is controlled by ENABLE_2.
5	DAC_1_SW_EN2	R/W	0	When set DAC_1_SW switch is controlled by ENABLE_2.
4	DAC_0_SW_EN2	R/W	0	When set DAC_0_SW switch is controlled by ENABLE_2.
3	DAC_3_SW_EN1	R/W	0	When set DAC_3_SW switch is controlled by ENABLE_1.
2	DAC_2_SW_EN1	R/W	0	When set DAC_2_SW switch is controlled by ENABLE_1.
1	DAC_1_SW_EN1	R/W	1	When set DAC_1_SW switch is controlled by ENABLE_1.
0	DAC_0_SW_EN1	R/W	0	When set DAC_0_SW switch is controlled by ENABLE_1.

9.33 DAC Power-Down Register: Page = 0x01

Address = 0x65, Default value = 0x00

Table 117. DAC Power-Down Register Field Descriptions

Bit	Field	Type	Default	Description
7	PDAC_REFDAC2	R/W	0	If PDAC_REFDAC2 = 0, REFDAC_2 is put into clamp mode. If PDAC_REFDAC2 = 1, REFDAC_2 is restored to normal operation.
6	PDAC_3	R/W	0	If PDAC_3 = 0, DAC_3 is put into clamp mode. If PDAC_3 = 1, DAC_3 is restored to normal operation.
5	PDAC_2	R/W	0	If PDAC_2 = 0, DAC_2 is put into clamp mode. If PDAC_2 = 1, DAC_2 is restored to normal operation.
4	RSVD_4	R/W	0	Reserved bit.
3	PDAC_REFDAC1	R/W	0	If PDAC_REFDAC1 = 0, REFDAC_1 is put into clamp mode. If PDAC_REFDAC1 = 1, REFDAC_1 is restored to normal operation.
2	PDAC_1	R/W	0	If PDAC_1 = 0, DAC_1 is put into clamp mode. If PDAC_1 = 1, DAC_1 is restored to normal operation.
1	PDAC_0	R/W	0	If PDAC_0 = 0, DAC_0 is put into clamp mode. If PDAC_0 = 1, DAC_0 is restored to normal operation.
0	RSVD_0	R/W	0	Reserved bit.

9.34 ADC Power-Down Register: Page = 0x01

Address = 0x66, Default value = 0x00

Table 118. ADC Power-Down Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	RSVD_7_1	R/W	All zeros	Reserved bit.
0	PADC	R/W	0	If PADC = 0, ADC is put into an inactive low-power mode. If PADC = 1, ADC is restored to normal operation.

9.35 Autonomous Mode Configuration Register: Page = 0x01

Address = 0x67, Default value = 0x08

Table 119. Autonomous Mode Configuration Register Field Descriptions

Bit	Field	Type	Default	Description
7	LUT_EN	R/W	0	If LUT_EN = 1 Autonomous mode is enabled at power on. If LUT_EN = 0 Autonomous mode is disabled at power on.
6	DEVICE_READY_ADC_COMP_EN	R/W	0	ADC monitoring and comparison of DAC output for DEVICE_READY setting. 0 = disabled (only timer based) 1 = enabled
5:4	TIM_DAC_EN	R/W	00	DAC enable timing at power on in autonomous mode only: 00 = 1ms 01 = 2ms 10 = 4ms 11 = 6ms
3:0	I2C_BASE_ADDR	R/W	1000	4-bit MSB of the I^2C static address.

9.36 DEVICE_READY Configuration Register: Page = 0x01

Address = 0x68, Default value = 0x01

Table 120. DEVICE_READY Configuration Register Field Descriptions

Bit	Field	Type	Default	Description
7	ASSERT	R/W	0	Optional bit to assert the DEVICE_READY signal independent of the operating conditions. 0 = Normal operation. 1 = DEVICE_READY signal is forced HIGH.
6	DEASSERT	R/W	0	Optional bit to de-assert the DEVICE_READY signal independent of the operating conditions. 0 = Normal operation. 1 = DEVICE_READY signal is forced LOW.

Bit	Field	Type	Default	Description
5:0	TIMER	R/W	000001	TIMER[5:0] is used as an input to a 22-bit down counter as follows: counter_in[21:0] = { TIMER[5:0], 16'h0000 } In general, the wait time is (TIMER[5:0] x 65536) x oscillator clock. See below some examples of the estimated wait time based on a typical oscillator frequency of 26MHz. 0x00: Reserved 0x01: 65536 x oscillator clock (2.52ms) ... 0x3F: 4128769 x oscillator clock (158,8ms)

9.37 DAC Configuration Register: Page = 0x01

Address = 0x69, Default value = 0x00

Table 121. DAC Configuration Register Field Descriptions

Bit	Field	Type	Default	Description
7	DAC_CLEAR_ZERO_SEL	R/W	0	DACs Clear code selection 0 = REFDAC_1 for DAC_0/1 and REFDAC_2 for DAC_2/3 1 = 0x000
6	DAC_CLAMP_EN	R/W	0	DACs low clamping enable 0 = disable 1 = enable
5	REFDAC_2_CLAMP_DIS	R/W	0	Disable clamp functionality of REFDAC_2 0 = REFDAC_2 is clamp DAC 1 = REFDAC_2 is independent DAC
4	REFDAC_1_CLAMP_DIS	R/W	0	Disable clamp functionality of REFDAC_1 0 = REFDAC_1 is clamp DAC 1 = REFDAC_1 is independent DAC
3	RSVD_3	R	0	Reserved bit.
2:0	DAC_RANGE	R/W	000	DAC output voltage selection: 0xx: Range set by auto-range detection circuit. 100 = -10 to 0V. 101 = -5 to 0V. (not used) 110 = 0 to 10V. 111 = 0 to 5V. (not used)

9.38 DAC Clear Enable Register: Page = 0x01

Address = 0x6A, Default value = 0x00

Table 122. DAC Clear Enable Register Field Descriptions

Bit	Field	Type	Default	Description
7	CLREN_REFDAC2	R/W	0	If CLREN_REFDAC2 = 1, REFDAC_2 is forced into a clear state with a clear event. If CLREN_REFDAC2 = 0, a clear event does not affect the state of REFDAC_2.
6	CLREN_DAC_3	R/W	0	If CLREN_3 = 1, DAC_3 is forced into a clear state with a clear event. If CLREN_3 = 0, a clear event does not affect the state of DAC_3.

Bit	Field	Type	Default	Description
5	CLREN_DAC_2	R/W	0	If CLREN_2 = 1, DAC_2 is forced into a clear state with a clear event. If CLREN_2 = 0, a clear event does not affect the state of DAC_2.
4	RSVD_4	R	0	Reserved bit.
3	CLREN_REFDAC1	R/W	0	If CLREN_REFDAC1 = 1, REFDAC_1 is forced into a clear state with a clear event. If CLREN_REFDAC1 = 0, a clear event does not affect the state of REFDAC_1.
2	CLREN_DAC_1	R/W	0	If CLREN_1 = 1, DAC_1 is forced into a clear state with a clear event. If CLREN_1 = 0, a clear event does not affect the state of DAC_1.
1	CLREN_DAC_0	R/W	0	If CLREN_0 = 1, DAC_0 is forced into a clear state with a clear event. If CLREN_0 = 0, a clear event does not affect the state of DAC_0.
0	RSVD_0	R	0	Reserved bit.

9.39 DAC Clear Source Register: Page = 0x01

Address = 0x6B, Default value = 0x00

Table 123. DAC Clear Source 0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RSVD_7_6	R	00	Reserved bit.
5	RT_HIGH_ALR_CLR	R/W	0	Remote Temperature sensor high alarm.
4	RT_LOW_ALR_CLR	R/W	0	Remote Temperature sensor low alarm.
3	RSVD_3	R	0	Reserved bit.
2	THERM_ALR_CLR	R/W	0	Die Temperature alarm.
1	LT_HIGH_ALR_CLR	R/W	0	Local Temperature sensor high alarm.
0	LT_LOW_ALR_CLR	R/W	0	Local Temperature sensor low alarm.

9.40 DAC Load Capacitor Configuration Register: Page = 0x01

Address = 0x6C, Default value = 0x00

Table 124. DAC Clear Source 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	REFDAC_2_LOAD_CAP	R/W	0	Select REFDAC_2 load capacitor range 0 = 0 to 0.1µF 1 = 0.1µF to 15µF
6	DAC_3_LOAD_CAP	R/W	0	Select DAC_3 load capacitor range 0 = 0 to 0.1µF 1 = 0.1µF to 15µF
5	DAC_2_LOAD_CAP	R/W	0	Select DAC_2 load capacitor range 0 = 0 to 0.1µF 1 = 0.1µF to 15µF
4	RSVD_4	R/W	0	Reserved bit.
3	REFDAC_1_LOAD_CAP	R/W	0	Select REFDAC_1 load capacitor range 0 = 0 to 0.1µF 1 = 0.1µF to 15µF
2	DAC_1_LOAD_CAP	R/W	0	Select DAC_1 load capacitor range 0 = 0 to 0.1µF 1 = 0.1µF to 15µF
1	DAC_0_LOAD_CAP	R/W	0	Select DAC_0 load capacitor range 0 = 0 to 0.1µF 1 = 0.1µF to 15µF
0	RSVD_0	R	0	Reserved bit.

9.41 DAC LUT 0 Control (Low Byte) Register: Page = 0x02

Address = 0x00, Default value = 0x00

Table 125. DAC LUT 0 (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DAC_0_BASE_L	R/W	All zeros	8-bit LSB byte of the 13-bit BASE value (LUT_0 output at 24°C).

9.42 DAC LUT 0 Control (High Byte) Register: Page = 0x02

Address = 0x01, Default value = 0x00

Table 126. DAC LUT 0 (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD_7	R/W	0	Reserved bit.
6	DAC_0_BYP	R/W	0	ALU bypass control: 1 = Bypass ALU. Send BASE value to DAC_0. 0 = ALU output sent to DAC_0.
5	DAC_0_POL	R/W	0	LUT_0 incremental polarity control: 1 = All LUT_0 values are treated as negative numbers. This realize a monotonically decreasing LUT_0 transfer function. 0 = All LUT_0 values are treated as positive numbers. This realize a monotonically increasing LUT_0 transfer function.
4:0	DAC_0_BASE_H	R/W	1000	5-bit MSB nibble of the 13-bit BASE value (LUT_0 output at 24°C).

9.43 DAC LUT 1 Control (Low Byte) Register: Page = 0x02

Address = 0x02, Default value = 0x00

Table 127. DAC LUT 1 (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DAC_1_BASE_L	R/W	All zeros	8-bit LSB byte of the 13-bit BASE value (LUT_1 output at 24°C).

9.44 DAC LUT 1 Control (High Byte) Register: Page = 0x02

Address = 0x03, Default value = 0x00

Table 128. DAC LUT 1 (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD_7	R/W	0	Reserved bit.
6	DAC_1_BYP	R/W	0	ALU bypass control: 1 = Bypass ALU. Send BASE value to DAC_1. 0 = ALU output sent to DAC_1.
5	DAC_1_POL	R/W	0	LUT_1 incremental polarity control: 1 = All LUT_1 values are treated as negative numbers. This realize a monotonically decreasing LUT_1 transfer function. 0 = All LUT_1 values are treated as positive numbers. This realize a monotonically increasing LUT_1 transfer function.
4:0	DAC_1_BASE_H	R/W	0000	5-bit MSB nibble of the 13-bit BASE value (LUT_1 output at 24°C).

9.45 DAC LUT 2 Control (Low Byte) Register: Page = 0x02

Address = 0x04, Default value = 0x00

Table 129. DAC LUT 2 (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DAC_2_BASE_L	R/W	All zeros	8-bit LSB byte of the 13-bit BASE value (LUT_2 output at 24°C).

9.46 DAC LUT 2 Control (High Byte) Register: Page = 0x02

Address = 0x05, Default value = 0x00

Table 130. DAC LUT 2 (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD_7	R/W	0	Reserved bit.
6	DAC_2_BYP	R/W	0	ALU bypass control: 1 = Bypass ALU. Send BASE value to DAC_2. 0 = ALU output sent to DAC_2.
5	DAC_2_POL	R/W	0	LUT_2 incremental polarity control: 1 = All LUT_2 values are treated as negative numbers. This realize a monotonically decreasing LUT_2 transfer function. 0 = All LUT_2 values are treated as positive numbers. This realize a monotonically increasing LUT_2 transfer function.
4:0	DAC_2_BASE_H	R/W	0000	5-bit MSB nibble of the 13-bit BASE value (LUT_2 output at 24°C).

9.47 DAC LUT 3 Control (Low Byte) Register: Page = 0x02

Address = 0x06, Default value = 0x00

Table 131. DAC LUT 3 (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DAC_3_BASE_L	R/W	All zeros	8-bit LSB byte of the 13-bit BASE value (LUT_3 output at 24°C).

9.48 DAC LUT 3 Control (High Byte) Register: Page = 0x02

Address = 0x07, Default value = 0x00

Table 132. DAC LUT 3 (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD_7	R/W	0	Reserved bit.
6	DAC_3_BYP	R/W	0	ALU bypass control: 1 = Bypass ALU. Send BASE value to DAC_3. 0 = ALU output sent to DAC_3.
5	DAC_3_POL	R/W	0	LUT_3 incremental polarity control: 1 = All LUT_3 values are treated as negative numbers. This realize a monotonically decreasing LUT_3 transfer function. 0 = All LUT_3 values are treated as positive numbers. This realize a monotonically increasing LUT_3 transfer function.
3:0	DAC_3_BASE_H	R/W	0000	5-bit MSB nibble of the 13-bit BASE value (LUT_3 output at 24°C).

9.49 DAC LUT Coefficient Registers: Page = 0x02, Address 0x08 – 0x6B

The following registers store the LUT coefficients.

Table 133. LUT 0 Coefficient Delta 0–47 Registers Description

Address	Name	Type	Default	Bit	Description
0x08	Delta 1 (-44°C)	R/W	All zeros	7:4	Stores the 4-bit LUT_0 Delta 1 entries. Reset by Power-on, Hardware Reset.
	Delta 0 (-48°C)	R/W	All zeros	3:0	Stores the 4-bit LUT_0 Delta 0. Reset by Power-on, Hardware Reset.
0x09	Delta 3 (-36°C)	R/W	All zeros	7:4	Stores the 4-bit LUT_0 Delta 3. Reset by Power-on, Hardware Reset.
	Delta 2 (-40°C)	R/W	All zeros	3:0	Stores the 4-bit LUT_0 Delta 2. Reset by Power-on, Hardware Reset.
0x0A	Delta 5 (-28°C)	R/W	All zeros	7:4	Stores the 4-bit LUT_0 Delta 5. Reset by Power-on, Hardware Reset.
	Delta 4 (-32°C)	R/W	All zeros	3:0	Stores the 4-bit LUT_0 Delta 4. Reset by Power-on, Hardware Reset.
…	…	…	…	…	…
0x15	Delta 27 (64°C)	R/W	All zeros	7:4	Stores the 4-bit LUT_0 Delta 27. Reset by Power-on, Hardware Reset.
	Delta 26 (60°C)	R/W	All zeros	3:0	Stores the 4-bit LUT_0 Delta 26. Reset by Power-on, Hardware Reset.
…	…	…	…	…	…
0x1F	Delta 47 (144°C)	R/W	All zeros	7:4	Stores the 4-bit LUT_0 Delta 47 entries. Reset by Power-on, Hardware Reset.
	Delta 46 (140°C)	R/W	All zeros	3:0	Stores the 4-bit LUT_0 Delta 46. Reset by Power-on, Hardware Reset.

Table 134. LUT 0 Coefficient Delta 48 Registers Description

Address	Name	Type	Default	Bit	Description
0x20	DAC_0_SLOPE	R/W	All zeros	7:6	LUT Slope control: 00 = 4.88 mV/C LUT slope (13-bit LUT resolution) 01 = 9.76 mV/C LUT slope (12-bit LUT resolution) 10 = 19.53 mV/C LUT slope (11-bit LUT resolution) 11 = 39.06 mV/C LUT slope (10-bit LUT resolution)
	Reserved	R/W	All zeros	5:4	Reserved bits.
	Delta 48 (148°C)	R/W	All zeros	3:0	Stores the 4-bit LUT_0 Delta 48. Reset by Power-on, Hardware Reset.

Table 135. LUT 1 Coefficient Delta 0–47 Registers Description

Address	Name	Type	Default	Bit	Description
0x21	Delta 1 (-44°C)	R/W	All zeros	7:4	Stores the 4-bit LUT_1 Delta 1 entries. Reset by Power-on, Hardware Reset.
	Delta 0 (-48°C)	R/W	All zeros	3:0	Stores the 4-bit LUT_1 Delta 0. Reset by Power-on, Hardware Reset.
0x22	Delta 3 (-36°C)	R/W	All zeros	7:4	Stores the 4-bit LUT_1 Delta 3. Reset by Power-on, Hardware Reset.
	Delta 2 (-40°C)	R/W	All zeros	3:0	Stores the 4-bit LUT_1 Delta 2. Reset by Power-on, Hardware Reset.
0x23	Delta 5 (-28°C)	R/W	All zeros	7:4	Stores the 4-bit LUT_1 Delta 5. Reset by Power-on, Hardware Reset.
	Delta 4 (-32°C)	R/W	All zeros	3:0	Stores the 4-bit LUT_1 Delta 4. Reset by Power-on, Hardware Reset.
…	…	…	…	…	…
0x2C	Delta 23 (48°C)	R/W	All zeros	7:4	Stores the 4-bit LUT_1 Delta 23. Reset by Power-on, Hardware Reset.
	Delta 22 (44°C)	R/W	All zeros	3:0	Stores the 4-bit LUT_1 Delta 22. Reset by Power-on, Hardware Reset.
…	…	…	…	…	…
0x38	Delta 47 (144°C)	R/W	All zeros	7:4	Stores the 4-bit LUT_1 Delta 47 entries. Reset by Power-on, Hardware Reset.
	Delta 46 (140°C)	R/W	All zeros	3:0	Stores the 4-bit LUT_1 Delta 46. Reset by Power-on, Hardware Reset.

Table 136. LUT 1 Coefficient Delta 48 Registers Description

Address	Name	Type	Default	Bit	Description
0x39	DAC_1_SLOPE	R/W	All zeros	7:6	LUT Slope control: 00 = 4.88 mV/C LUT slope (13-bit LUT resolution) 01 = 9.76 mV/C LUT slope (12-bit LUT resolution) 10 = 19.53 mV/C LUT slope (11-bit LUT resolution) 11 = 39.06 mV/C LUT slope (10-bit LUT resolution)
	Reserved	R/W	All zeros	5:4	Reserved bits.
	Delta 48 (148°C)	R/W	All zeros	3:0	Stores the 4-bit LUT_1 Delta 48. Reset by Power-on, Hardware Reset.

Table 137. LUT 2 Coefficient Delta 0–47 Registers Description

Address	Name	Type	Default	Bit	Description
0x3A	Delta 1 (-44C)	R/W	All zeros	7:4	Stores the 4-bit LUT_2 Delta 1 entries. Reset by Power-on, Hardware Reset.
	Delta 0 (-48C)	R/W	All zeros	3:0	Stores the 4-bit LUT_2 Delta 0. Reset by Power-on, Hardware Reset.
0x3B	Delta 3 (-36C)	R/W	All zeros	7:4	Stores the 4-bit LUT_2 Delta 3. Reset by Power-on, Hardware Reset.
	Delta 2 (-40C)	R/W	All zeros	3:0	Stores the 4-bit LUT_2 Delta 2. Reset by Power-on, Hardware Reset.
0x3C	Delta 5 (-28C)	R/W	All zeros	7:4	Stores the 4-bit LUT_2 Delta 5. Reset by Power-on, Hardware Reset.
	Delta 4 (-32C)	R/W	All zeros	3:0	Stores the 4-bit LUT_2 Delta 4. Reset by Power-on, Hardware Reset.
…	…	…	…	…	…
0x43	Delta 19 (32C)	R/W	All zeros	7:4	Stores the 4-bit LUT_2 Delta 19. Reset by Power-on, Hardware Reset.
	Delta 18 (28C)	R/W	All zeros	3:0	Stores the 4-bit LUT_2 Delta 18. Reset by Power-on, Hardware Reset.
…	…	…	…	…	…
0x51	Delta 47 (144C)	R/W	All zeros	7:4	Stores the 4-bit LUT_2 Delta 47 entries. Reset by Power-on, Hardware Reset.
	Delta 46 (140C)	R/W	All zeros	3:0	Stores the 4-bit LUT_2 Delta 46. Reset by Power-on, Hardware Reset.

Table 138. LUT 2 Coefficient Delta 48 Registers Description

Address	Name	Type	Default	Bit	Description
0x52	DAC_2_SLOPE	R/W	All zeros	7:6	LUT Slope control: 00 = 4.88 mV/C LUT slope (13-bit LUT resolution) 01 = 9.76 mV/C LUT slope (12-bit LUT resolution) 10 = 19.53 mV/C LUT slope (11-bit LUT resolution) 11 = 39.06 mV/C LUT slope (10-bit LUT resolution)
	Reserved	R/W	All zeros	5:4	Reserved bits.
	Delta 48 (148C)	R/W	All zeros	3:0	Stores the 4-bit LUT_2 Delta 48. Reset by Power-on, Hardware Reset.

Table 139. LUT 3 Coefficient Delta 0–47 Registers Description

Address	Name	Type	Default	Bit	Description
0x53	Delta 1 (-44C)	R/W	All zeros	7:4	Stores the 4-bit LUT_3 Delta 1 entries. Reset by Power-on, Hardware Reset.
	Delta 0 (-48C)	R/W	All zeros	3:0	Stores the 4-bit LUT_3 Delta 0. Reset by Power-on, Hardware Reset.
0x54	Delta 3 (-36C)	R/W	All zeros	7:4	Stores the 4-bit LUT_3 Delta 3. Reset by Power-on, Hardware Reset.
	Delta 2 (-40C)	R/W	All zeros	3:0	Stores the 4-bit LUT_3 Delta 2. Reset by Power-on, Hardware Reset.
0x55	Delta 5 (-28C)	R/W	All zeros	7:4	Stores the 4-bit LUT_3 Delta 5. Reset by Power-on, Hardware Reset.
	Delta 4 (-32C)	R/W	All zeros	3:0	Stores the 4-bit LUT_3 Delta 4. Reset by Power-on, Hardware Reset.
…	…	…	…	…	…
0x5A	Delta 15 (12C)	R/W	All zeros	7:4	Stores the 4-bit LUT_3 Delta 15. Reset by Power-on, Hardware Reset.
	Delta 14 (8C)	R/W	All zeros	3:0	Stores the 4-bit LUT_3 Delta 14. Reset by Power-on, Hardware Reset.
…	…	…	…	…	…
0x6A	Delta 47 (144C)	R/W	All zeros	7:4	Stores the 4-bit LUT_3 Delta 47 entries. Reset by Power-on, Hardware Reset.
	Delta 46 (140C)	R/W	All zeros	3:0	Stores the 4-bit LUT_3 Delta 46. Reset by Power-on, Hardware Reset.

Table 140. LUT 3 Coefficient Delta 48 Registers Description

Address	Name	Type	Default	Bit	Description
0x6B	DAC_3_SLOPE	R/W	All zeros	7:6	LUT Slope control: 00 = 4.88 mV/C LUT slope (13-bit LUT resolution) 01 = 9.76 mV/C LUT slope (12-bit LUT resolution) 10 = 19.53 mV/C LUT slope (11-bit LUT resolution) 11 = 39.06 mV/C LUT slope (10-bit LUT resolution)
	Reserved	R/W	All zeros	5:4	Reserved.
	Delta 48 (148C)	R/W	All zeros	3:0	Stores the 4-bit LUT_3 Delta 48. Reset by Power-on, Hardware Reset.

9.50 REFDAC Data Registers: Page = 0x02, Address 0x6C– 0x6F

9.50.1. REFDAC1 Data (Low Byte) Register

Address = 0x6C, Default value = 0x00

Table 141. XDAC REFDAC1 Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	REFDAC_1_DATA_L	R/W	All zeros	8-bit LSB byte to be loaded to the REFDAC_1.

9.50.2. REFDAC1 Data (High Byte) Register

Address = 0x6D, Default value = 0x00

Table 142. DAC_0_OVRD_H Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R/W	All zeros	Reserved bit.
3:0	REFDAC_1_DATA_H	R/W	All zeros	4-bit MSB nibble to be loaded to the REFDAC_1.

9.50.3. REFDAC2 Data (Low Byte) Register

Address = 0x6E, Default value = 0x00

Table 143. XDAC REFDAC1 Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	REFDAC_2_DATA_L	R/W	All zeros	8-bit LSB byte to be loaded to the REFDAC_2.

9.50.4. REFDAC2 Data (High Byte) Register

Address = 0x6F, Default value = 0x00

Table 144. DAC_0_OVRD_H Data (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RSVD_7_4	R/W	All zeros	Reserved bit.
3:0	REFDAC_2_DATA_H	R/W	All zeros	4-bit MSB nibble to be loaded to the REFDAC_2.

9.51 Remote Temperature Sensor Calibration Registers: Page 0x02, Address 0x70 – 0x71

9.51.1. ADC Remote Temperature Sensor Offset Calibration Register

Address = 0x70, Default value = 0x00

Table 145. Local Temp Sensor Offset Calibration Register Field Descriptions

Bit	Field	Type	Default	Description
7	SIGN	R/W	All zeros	Sign bit. 0 = OFFSET_VALUE has positive polarity. 1 = OFFSET_VALUE has negative polarity.
6:0	OFFSET_VALUE	R/W	All zeros	Offset value for remote temperature ADC channel.

9.51.2. ADC Remote Temperature Sensor Calibration Register

Address = 0x71, Default value = 0x2A

Table 146. Local Temp Sensor Calibration Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD_7	R	-	Reserved bit.
6:4	RT_SENSE_GAIN_CAL_H	R/W	010	Coarse trim 3 MSB bits- Amplifier gain adjustment. 000 (Highest gain) 001 010 011 100 101 110, 111 (Lowest gain)
3:0	RT_SENSE_GAIN_CAL_L	R/W	1010	Fine trim 4 LSB bits- Ibias change for finer gain adjustment 0000 – Ibias=5uA (Highest gain) 0001 – Ibias=15µA 0010 – Ibias=25µA 0011 – Ibias=35µA 0100 – Ibias=45vA 0101 – Ibias=55µA 0110 – Ibias=65µA 0111 – Ibias=75µA 1000 – Ibias=85µA 1001 – Ibias=95µA 1010 – Ibias=105µA 1011 – Ibias=115µA 11xx – Ibias=120µA (Lowest gain)

9.52 Alarm Configuration Registers: Page 0x03, Address 0x00 – 0x02

9.52.1. Alarm Source 0 Register: Page = 0x03

Address = 0x00, Def. Value 0x00

Table 147. Alarm Configuration 0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	S0S1_ERR_ALR	R/W	0	S0/S1 error types
6	PAR_ERR_ALR	R/W	0	Parity check error
5	RT_HIGH_ALR	R/W	0	Remote Temperature sensor high alarm.
4	RT_LOW_ALR	R/W	0	Remote Temperature sensor low alarm.
3:0	RSVD_3_0	R	-	Reserved bit.

9.52.2. Alarm Source 1 Register: Page = 0x03

Address = 0x01, Def. Value 0x00

Table 148. Alarm Configuration 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	DAV_ALR	R/W	0	ADC Data available flag
6:3	RSVD_6_3	R	-	Reserved bit.
2	THERM_ALR	R/W	0	Die temperature alarm.
1	LT_HIGH_ALR	R/W	0	Temperature sensor high alarm.
0	LT_LOW_ALR	R/W	0	Temperature sensor low alarm.

9.53 False Alarm Configuration: Page 0x03, Address 0x03

9.53.1. False Alarm Configuration Register

Address = 0x03, Default value = 0x15

Table 149. False Alarm Configuration Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RSVD_7_5	R		Reserved bit.
4:3	LT_FALR_CT	R/W	10	False alarm protection for local temperature sensor. Number of consecutive samples before alarm is set: 00 = 1 01 = 2 10 = 4 (default) 11 = 8
2:1	RT_FALR_CT	R/W	10	False alarm protection for remote temperature sensor. Number of consecutive samples before alarm is set: 00 = 1 01 = 2 10 = 4 (default) 11 = 8
0	ALR_LATCH_DIS	R/W	1	Alarm latch disable bit. When cleared to 0 the alarm bits are latched. When an alarm occurs, the corresponding alarm bit is set to 1. The alarm bit remains until the error condition subsides and the alarm register is read. Before reading, the alarm bit is not cleared even if the alarm condition disappears. When set to 1 the alarm bits are not latched. When the alarm condition subsides, the alarm bits are cleared regardless of whether the alarm bits have been read or not.

9.54 Temperature Sensor Threshold Registers: Page 0x03, Address 0x04 – 0x0B

The F39510 includes high-limit and low-limit detection for the Local and Remote Temperature Sensor. The values in the Local Temperature Sensor Upper and Lower Threshold registers (address 0x04 through 0x07) set the limits for the Local Temperature Sensor.

The temperature sensor detector can issue either a high-alarm (lt_high_alr_evt) or a low-alarm (lt_low_alr_evt) depending on whether the high or low thresholds were exceeded. To implement single, upper-bound threshold detection for the temperature sensor, the host processor can set the upper-bound threshold to the desired value and the lower-bound threshold to the default value.

For lower-bound threshold detection, the host processor can set the lower-bound threshold to the desired value and the upper-bound threshold to the default value.

The high-limit and low-limit detection for the Remote Temperature Sensor (address 0x08 through 0x0B) is the same as for the Local Temperature Sensor. A die thermal-alarm flag is not included in the Remote Temperature Sensor detection circuit.

9.54.1. Local Temperature Sensor Upper-Threshold (Low Byte) Register

Address = 0x04, Default value = 0xC0

Table 150. Local Temperature Sensor Upper-Threshold (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LT_UP_THR_L	R/W	1100 0000	8-bit LSB byte (right aligned format) or trailing zeros padded nibble (left aligned format) of the 12-bit upper threshold value for the local temperature sensor.

9.54.2. Local Temperature Sensor Upper-Threshold (High Byte) Register

Address = 0x05, Default value = 0xFF

Table 151. Local Temperature Sensor Upper-Threshold (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LT_UP_THR_H	R/W	0111	8-bit MSB byte (left aligned format) or leading zeros padded nibble (right aligned format) of the 12-bit upper threshold value for the local temperature sensor.

9.54.3. Local Temperature Sensor Lower-Threshold (Low Byte) Register

Address = 0x06, Default value = 0x00

Table 152. Local Temperature Sensor Lower-Threshold (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LT_LO_THR_L	R/W	All zeros	8-bit LSB byte (right aligned format) or trailing zeros padded nibble (left aligned format) of the 12-bit lower threshold value for the local temperature sensor.

9.54.4. Local Temperature Sensor Lower-Threshold (High Byte) Register

Address = 0x07, Default value = 0x00

Table 153. Local Temperature Sensor Lower-Threshold (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LT_LO_THR_H	R/W	1000	8-bit MSB byte (left aligned format) or leading zeros padded nibble (right aligned format) of the 12-bit lower threshold value for the local temperature sensor.

9.54.5. Remote Temperature Sensor Upper-Threshold (Low Byte) Register

Address = 0x08, Default value = 0xC0

Table 154. Remote Temperature Sensor Upper-Threshold (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RT_UP_THR_L	R/W	1100 0000	8-bit LSB byte (right aligned format) or trailing zeros padded nibble (left aligned format) of the 12-bit upper threshold value for the remote temperature sensor.

9.54.6. Remote Temperature Sensor Upper-Threshold (High Byte) Register

Address = 0x09, Default value = 0xFF

Table 155. Remote Temperature Sensor Upper-Threshold (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RT_UP_THR_H	R/W	1111 1111	8-bit MSB byte (left aligned format) or leading zeros padded nibble (right aligned format) of the 12-bit upper threshold value for the remote temperature sensor.

9.54.7. Remote Temperature Sensor Lower-Threshold (Low Byte) Register

Address = 0x0A, Default value = 0x00

Table 156. Remote Temperature Sensor Lower-Threshold (Low Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RT_LO_THR_L	R/W	All zeros	8-bit LSB byte (right aligned format) or trailing zeros padded nibble (left aligned format) of the 12-bit lower threshold value for the remote temperature sensor.

9.54.8. Remote Temperature Sensor Lower-Threshold (High Byte) Register

Address = 0x0B, Default value = 0x00

Table 157. Remote Temperature Sensor Lower-Threshold (High Byte) Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RT_LO_THR_H	R/W	All zeros	8-bit MSB byte (left aligned format) or leading zeros padded nibble (right aligned format) of the 12-bit lower threshold value for the remote temperature sensor.

9.55 Hysteresis Registers: Page 0x03, Address 0x0C – 0x0D

9.55.1. Local Temperature Hysteresis Register

Address = 0x0C, Default value = 0x08

Table 158. LT Hysteresis Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RSVD_7_5	R	All zeros	Reserved bit.
4:0	HYST_LT	R/W	01000	Hysteresis of local temperature sensor, 1°C per step. The range is 0°C to 31°C.

9.55.2. Remote Temperature Hysteresis Register

Address = 0x0D, Default value = 0x08

Table 159. RT Hysteresis Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RSVD_7_5	R	All zeros	Reserved bit.
4:0	HYST_RT	R/W	01000	Hysteresis of remote temperature sensor, 1°C per step. The range is 0°C to 31°C.

9.56 NOTEPAD Registers: Page = 0x0F, Address = 0x00 – 0x13

Table 160. Notepad Register Field Descriptions

Address	Name	Type	Default	Bit	Description
0x00–0x13	NOTEPAD0-19	R/W	All zeros	7:0	User arbitrary storage

9.57 EEPROM Config Register: Page 0x11, Address 0x01

Address = 0x01, Default value = 0x00

Table 161. RT Hysteresis Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RSVD_7_2	R	All zeros	Reserved bit.
1	EEPROM_CFG	R/W	0	Configure the EEPROM to fast mode. 0: Normal mode 1: Fast mode
0	RSVD	R	0	Reserved bit.

10. Evaluation Kit Information

10.1 Evaluation Board Picture

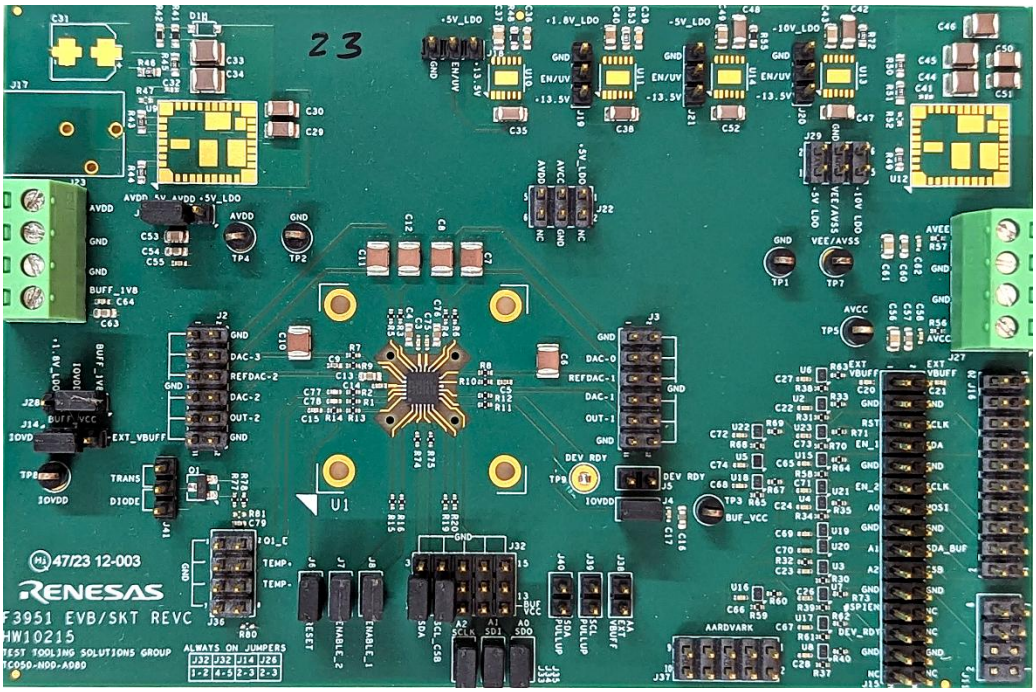


Figure 46: Evaluation Board (Front)

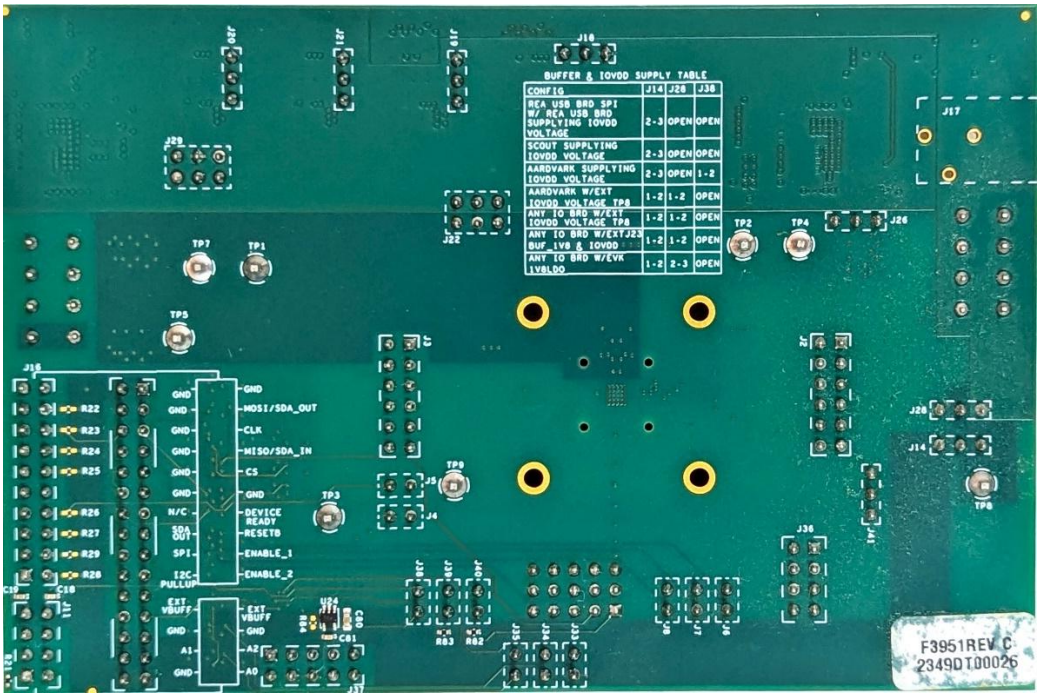


Figure 47: Evaluation Board (Back)

10.2 Evaluation Kit Bill-of-Materials (BOM)

Part Reference	Qty	Pack Type	Description	Manufacturer	Part Number
C3,C14,C17,C18,C19,C20, C21,C22,C23,C24,C26,C27 ,C28,C55,C58,C62,C64,C6 5,C66,C67,C68,C69,C70, C71,C72,C73,C74,C75,C81	29	0402	X7R Surface Mount Capacitor	Murata Electronics	GCM155R71E104KE02D
C4,C13,C16,C54,C57,C61, C63,C76,C80	9	0603	X7R Surface Mount Capacitor	Murata Electronics	GCM188R71E105KA64D
C5,C9	2	0402	X7R Surface Mount Capacitor	Murata Electronics	GRM155R71E223J
C6,C7,C8,C10,C11,C12	6	1210	X7R Surface Mount Capacitor	TDK Corporation	CGA6M3X7R1E156M200AB
C15	1	0402		Murata Electronics	GRM1555C1E102J
C29,C30,C50,C51	4	1206	X5R Surface Mount Capacitor	Murata Electronics	GRM31CR61E476ME44L
C33,C34,C44,C45	4	1210		TDK Corporation	CGA6P3X7R1H475K250
C35,C38,C42,C47,C48,C52	6	1206	X7R Surface Mount Capacitor	TDK Corporation	C3216X7R1E475K160AC
C36,C39	2	0603		Murata Electronics	GRM188R71E474K
C37,C40,C43,C49,C53,C56 ,C60	7	0805		Murata Electronics	GRM21BC71E106K
C46	1	1210		TDK Corporation	C3225X7R1H225K250
C77,C78	2	0402	X8R Surface Mount Capacitor	Kemet	C0402C100J5HACAUTO
C79	1	0402	COG Surface Mount Capacitor	Murata Electronics	GRM1555C1H101JA01D
J2,J3	2	Vertical	Molex C-Grid Header Dual, Gold, Unshrouded, Breakaway, 100mil pitch	Molex	10-89-7120
J4,J5,J6,J7,J8,J33,J34,J35, J38,J39,J40	11	Vertical	Molex: Header, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240 inch contact mating length	Molex	22-28-4023
J11,J36	2	Vertical	Molex: C-Grid Header Dual, Gold, Unshrouded, Breakaway, 100mil pitch	Molex	10-89-7080
J14,J18,J19,J20,J21,J26, J28,J41	8	Vertical	Molex: Header, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240 inch contact mating length	Molex	22-28-4033
J15	1	Vertical	Sullins: Connector Header Through Hole 30 position 0.100" (2.54mm)	Sullins	PBC15DFAN
J16	1	Vertical	Molex: Header Dual, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240 inch contact mating length	Molex	10-89-7200

J22,J29	2	Vertical	Molex: Unshrouded Header Vert 100 MIL	Molex	10-89-7062
J23,J27	2	Thru Hole	Phoenix: 4 Position Wire to Board Terminal Block Horizontal with Board 0.150" (3.81mm) Through Hole	Phoenix Contact	1705566
J32	1	Vertical	Samtec: Connector Header Through Hole 15 position 0.100" (2.54mm)	Samtec	TSW-105-07-F-T
J37	1	Vertical	Molex: Header Dual, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240 inch contact mating length	Molex	10-89-7100
Q1	1	SOT23-3	ON: Bipolar (BJT) Transistor PNP 150 V 600 mA 300MHz 350 mW Surface Mount SOT-23-3	ON Semiconductor	MMBT5401
R1,R2,R3,R4,R5,R6,R7,R8,R9,R10,R11,R12,R13,R14,R15,R16,R19,R20,R56,R57	20	0402		Panasonic	ERJ-2GE0R00
R21,R67	2	0402	Surface Mount Resistor	Yageo	RC0402FR-0710KL
R30,R31,R34,R37,R38,R39,R58,R59,R61,R65,R68,R70	12	0402			CRCW0402100KFKED
R32	1	0402			CRCW04024K70FK
R33,R35,R40,R60,R62,R63,R64,R69,R71,R73	10	0402	Surface Mount Resistor	Vishay	CRCW0402510KFK
R41,R48,R55	3	0603	Surface Mount Resistor	Vishay	CRCW060349K9FKEA
R42	1	0603	Surface Mount Resistor	Panasonic	ERJ-3EKF2402
R43	1	0603	Surface Mount Resistor	Vishay	CRCW0603220KFK
R44,R45,R49,R50	4	0603	Surface Mount Resistor	Vishay	CRCW0603160KFK
R46,R51	2	0603	Surface Mount Resistor	Vishay	CRCW060313K0FK
R53	1	0603	Surface Mount Resistor	Susumu	RGT1608P-183-B-T5
R72	1	0603	Surface Mount Resistor	Vishay	CRCW0603100KFK
R74,R75,R77,R78	4	0402	Surface Mount Resistor	Vishay	CRCW040251R0FK
R82,R83	2	0402	Surface Mount Resistor	Vishay	CRCW04023K30FK
R84	1	0402	Surface Mount Resistor		DNI
TP1,TP2,TP3,TP4,TP5,TP7,TP8,TP9	8	Thru Hole	Keystone Electronics: Phosphor Bronze Wire Loop, heat resistant nylon base	Keystone	5006

U1	1	QFN24	TTS: QFN24 4.0mm x 4.0mm 0.5 Pitch	Test Tooling Solutionss	DNI
U2,U3,U4,U6,U7,U8,U15,U16,U17,U18,U19,U20,U21,U22,U23	15	SON6	TI: Buffer, Non-Inverting 1 Element 1 Bit per Element 3-State Output 6-SON (1.45x1)	Texas Instruments	1P1G125QDRYRQ1
U5	1	SON6	TI: Inverter IC 1 Channel - 6-SON (1.45x1)	Texas Instruments	SN74LVC1G04DRYR
U24	1	SC70-5	TI: IC REG LINEAR 3.3V 50MA FIXED SC70-5	Texas Instruments	TPS71533DCKR

11. Application Information

The F39510 is primarily used as a power amplifier bias controller in multi-channel RF communication applications such as 5G mMIMO/Macro base stations and wireless infrastructure. The device can also be used in other closed-loop systems designed for test and measurement.

The F39510 offers four temperature compensated DAC channels to autonomously adjust the power amplifier (PA) bias points in response to temperature changes during PA operation and two DAC channels to selectively program the clamp voltages. The temperature-to-voltage transfer functions are user defined and stored in the internal EEPROM. This helps to optimize PA RF performance, power efficiency, and stability. The device has an internal temperature sensor and remote temperature sensor that can monitor the PA temperature variations during operation.

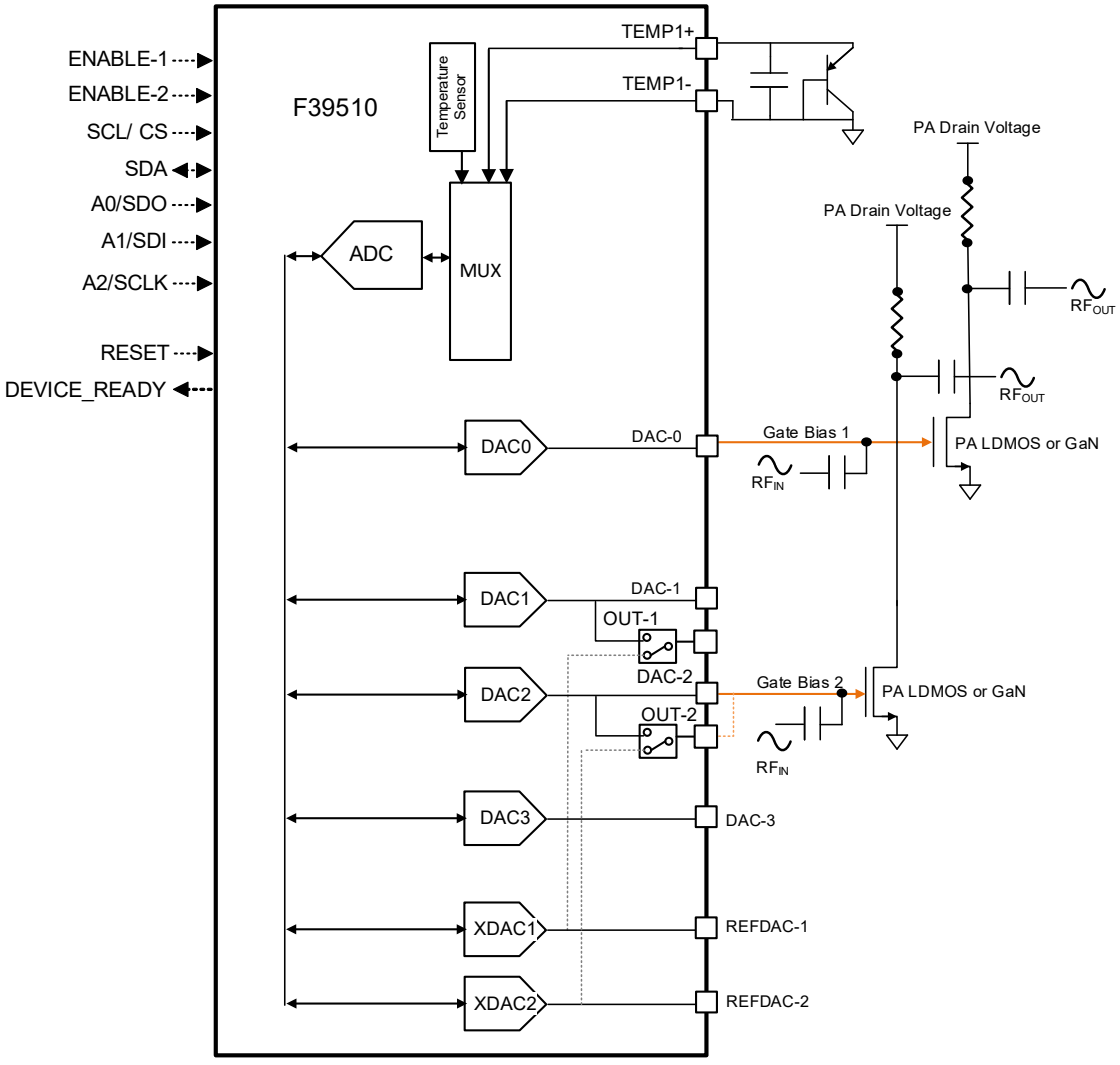


Figure 48. Simplified Diagram of F39510 PA Bias and Temperature Monitoring System

12. Power Sequencing

12.1 Power-Up Sequence

The required pin order for applying power is A_{VSS}, followed by A_{VDD} and IO_{VDD}, A_{VCC}. To enable autonomous mode, A_{VCC} must be applied after the EEPROM data transfer is completed. When power sequencing, ensure that all digital pins are not powered or in an active state while the IO_{VDD} pin ramps.

For any deviation from the above power-up sequence, contact your local Axiro Sales representative.

12.2 Power-Down Sequence

Before starting the Power-Down Sequence, enter the power-down mode (Device Configuration Register) in which the device is non-operational except for the Serial Interface as determined by the Power-Down registers.

The preferred Power-Down Sequence is the exact reverse of the Power-Up Sequence described in section 12.1.

12.3 Power-on-Reset (POR)

In the F39510, after all the power supplies are present, a POR event occurs. The POR event causes all registers to initialize to their default values and prevents communication with the device for a duration of 350µs (power-on reset delay). Communication with the device resumes (becomes valid) only after the power-on reset delay.

The F39510 operates by default in power-down mode (register 0x02 default value 0x03). In power-down mode, the device is non-operational except for the communication interface as determined by the power-down registers. Before enabling normal operation, a hardware reset is necessary.

A power failure on A_{VDD}, IO_{VDD} or A_{VSS} has the potential to initiate a power-on-reset event. A power failure event will not occur if A_{VDD}, IO_{VDD} and A_{VCC} remain above the minimum recommended operating conditions. When any of these supplies drop below the minimum recommended operating condition, the device may not initiate a POR. In this case, issuing a hardware reset or proper POR is recommended to resume proper operation. For an appropriate POR event to occur, IO_{VDD} supply must not fall below 1.6V.

12.4 Hardware Reset

In the F39510, a hardware reset occurs by applying a minimum 20ns logic low on the $\overline{\text{RESET}}$ pin. A hardware reset causes all registers to initialize to their default value and prevents communication with the device for a duration of 350µs (reset delay). Communication with the device resumes (becomes valid) after 350µs.

12.5 Software Reset

In the F39510, a software reset occurs by setting the SOFT-RESET bit in register 0x04 (interface configuration 0). A software reset causes all registers except addresses 0x04 and 0x05 to initialize to their default value, and communication with the device becomes valid only after a 100ns delay

13. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Axiro website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

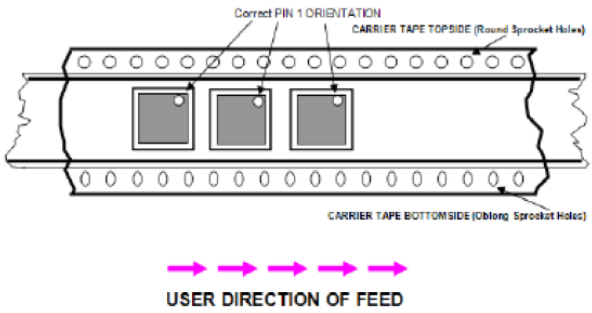
14. Ordering Information

Part Number	Package Description	MSL Rating	Carrier Type	Temperature Range
RRF39510-B00	24-VFQFPN, 4 × 4 mm	MSL3	Tray	-40°C to +125°C
RRF39510-K00		MSL3	Tape and Reel (see Table 162)	
RTKRF39510-000	Evaluation Kit			

15. Marking Information

Top Marking Illustration	Marking	Representation
	$	Factory Code
	Y	Last Digit of the Year
	WW	Work Week
	***	Lot Sequential Code

Table 162. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
K00	Quadrant 2 (EIA-481-D)	

16. Revision History

Revision	Date	Description
2.0	Feb 12, 2026	Final Datasheet.