

# F1358

DPD Demodulator for PA Linearization 3200 MHz to 4000 MHz

## GENERAL DESCRIPTION

This document describes the specification for the AXIROF1358 Digital Pre-Distortion Demodulator for PA linearization. This series of devices is offered in 3 variants to cover common UTRA bands.

## COMPETITIVE ADVANTAGE

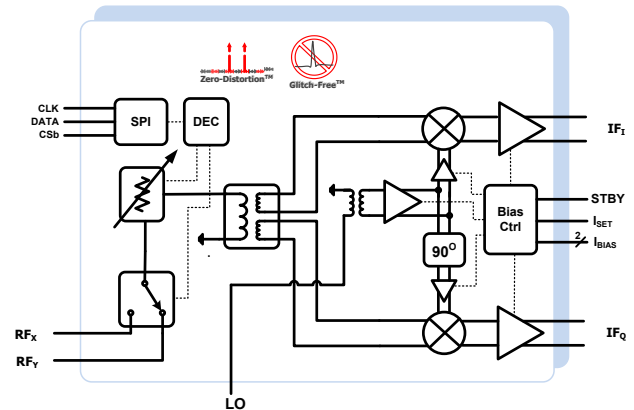
In typical basestation transmitters, digital pre-distortion is employed to improve the Transmitter performance. The signal coming out of the PA is sampled and the incoming Tx chain I&Q data is pre-distorted to counteract the distortion inherent in the PA. The PA signal is adjusted via a digital step attenuator to a lower level and then sub-sampled at an IF frequency of ~200 MHz which necessitates the need for a highly linear demodulator to downmix to quadrature IF from the Transmit frequency. By sampling IF\_I and IF\_Q independently and then digitally combining these signals, an effective doubling of the sample rate can be achieved. Any distortion in this path will degrade the performance of the DPD algorithm. By utilizing an ultra-linear demodulator w/integrated DSA such as the AXIROF1358, the ACLR and/or power consumption of the full Tx system can be improved significantly.

- ✓ GlitchFree™ Technology gives better gain control
- ✓ Zero-Distortion™ eliminates the need for a second IF amplifier in the channel
- ✓ ACLR is reduced for the full channel
- ✓ Power Consumption is reduced by 40%
- ✓ Integrates 2 BPFs, 2 Baluns, and a SPDT RF switch

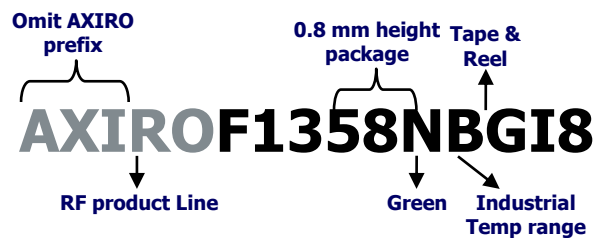
## FEATURES

- Wide flat performance IF BW
- Wide RF and LO BWs (~ 800 MHz)
- LO can be High or Low Side
- Ideal for Multi-Carrier Systems
- Drives ADC directly
- Ultra linear +41 dBm OIP3
- Excellent ACLR performance
- 200  $\Omega$  output impedance
- Fully integrated DPD demodulator
- Standby Mode w/Fast Recovery
- Current draw is 216 mA
- 6 x 6 mm 36 pin package

## FUNCTION BLOCK DIAGRAM



## ORDERING INFORMATION



**ABSOLUTE MAXIMUM RATINGS**

| Parameter                                                 | Symbol                  | Min  | Max                    | Units |
|-----------------------------------------------------------|-------------------------|------|------------------------|-------|
| V <sub>CC</sub> to GND                                    | V <sub>CC</sub>         | -0.3 | +5.5                   | V     |
| DATA, CSb, CLK, SW_Latch                                  | V <sub>Logic</sub>      | 0.0  | 3.6                    | V     |
| STBY                                                      | V <sub>Logic-Stby</sub> | 0.0  | V <sub>CC</sub>        |       |
| IF_I+, IF_I-, IF_Q+, IF_Q-,                               | I <sub>IF</sub>         | 1.00 | V <sub>CC</sub> + 0.30 | V     |
| RF_INX, RF_INY                                            | V <sub>RF</sub>         | -0.3 | +0.30                  | V     |
| LO_IN                                                     | V <sub>LO</sub>         | -0.3 | +0.30                  | V     |
| LO_ADJ to Ground                                          | V <sub>LOBias</sub>     | +2.1 | +4.0                   | V     |
| IF_BiasI, IF_BiasQ to Ground                              | V <sub>IFbias</sub>     | -0.3 | +1.20                  | V     |
| Maximum RF Input Power<br>(RFIN_X, RFIN_Y)                | P <sub>RFIN</sub>       |      | +27                    | dBm   |
| Continuous Power Dissipation                              | P <sub>diss</sub>       |      | 2.5                    | W     |
| Junction Temperature                                      | T <sub>j</sub>          |      | 150                    | °C    |
| Storage Temperature Range                                 | T <sub>st</sub>         | -65  | 150                    | °C    |
| Lead Temperature (soldering, 10s)                         |                         |      | 260                    | °C    |
| ElectroStatic Discharge – HBM<br>(JEDEC/ESDA JS-001-2012) |                         |      | 1000<br>(Class 1C)     | Volts |
| ElectroStatic Discharge – CDM<br>(JEDEC 22-C101F)         |                         |      | 500<br>(Class C4)      | Volts |

*Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**ESD CAUTION**

*This product features proprietary protection circuitry. However, it may be damaged if subjected to high energy ESD. Please use proper ESD precautions when handling to avoid damage or loss of performance.*

**PACKAGE THERMAL AND MOISTURE CHARACTERISTICS**

|                                                                               |         |
|-------------------------------------------------------------------------------|---------|
| θ <sub>JA</sub> (Junction – Ambient)                                          | 40 °C/W |
| θ <sub>JC</sub> (Junction – Case) [The Case is defined as the exposed paddle] | 3 °C/W  |
| Moisture Sensitivity Rating (Per J-STD-020)                                   | MSL1    |



**F1358 RECOMMENDED OPERATING CONDITIONS**

| Parameter                   | Symbol                                     | Conditions                                                                                              | Min  | Typ  | Max  | Units |
|-----------------------------|--------------------------------------------|---------------------------------------------------------------------------------------------------------|------|------|------|-------|
| Supply Voltage(s)           | V <sub>CC</sub>                            | All VCC pins                                                                                            | 4.75 | 5.00 | 5.25 | V     |
| Operating Temperature Range | T <sub>CASE</sub>                          | Case Temperature                                                                                        | -40  |      | 105  | °C    |
| RF Freq Range - Linearity   | F <sub>RF-LIN</sub>                        | ATTN = 0 dB<br>P <sub>RF</sub> = -11 dBm/Tone<br>F <sub>IF</sub> = 200 MHz<br>OIP3 > +35 dBm            | 3200 |      | 4000 | MHz   |
| RF Freq Range - Oversampled | F <sub>RF-OS</sub>                         | ATTN = 0 dB<br>RF_INX<br>F <sub>LO</sub> = 3180-3500 MHz<br>Gain Delta < 2.5 dB                         | 3200 |      | 4000 | MHz   |
| LO Freq Range               | F <sub>LO</sub>                            |                                                                                                         | 3100 |      | 3800 | MHz   |
| LO Power                    | P <sub>LO</sub>                            |                                                                                                         | -3   |      | 3    | dBm   |
| IF Freq Range - Linearity   | F <sub>IF-LIN</sub>                        | ATTN = 0 dB<br>RF_INX<br>P <sub>RF</sub> = -11 dBm/Tone<br>F <sub>RF</sub> = 3600 MHz<br>OIP3 > +35 dBm | 100  |      | 300  | MHz   |
| IF Freq Range- Oversampled  | F <sub>IF-OS</sub>                         | ATTN = 0 dB<br>RF_INX<br>F <sub>LO</sub> = 3180-3500 MHz<br>Gain Delta < 2.5 dB                         | 20   |      | 500  | MHz   |
| RF Source Impedance         | Z <sub>RF_INX</sub><br>Z <sub>RF_INY</sub> | Single Ended                                                                                            |      | 50   |      | Ω     |
| LO Source Impedance         | Z <sub>LO</sub>                            | Single Ended                                                                                            |      | 50   |      | Ω     |
| IF Load Impedance           | Z <sub>IF_I</sub><br>Z <sub>IF_Q</sub>     | Differential                                                                                            |      | 200  |      | Ω     |

## F1358 SPECIFICATION

Specifications apply at  $V_{CC} = +5.00\text{ V}$ ,  $T_{CASE} = +25\text{ }^{\circ}\text{C}$ ,  $F_{RF} = 3455\text{ MHz}$ ,  $G_{max}$ ,  $P_{RF} = -11\text{ dBm}$ ,  $F_{LO} = 3255\text{ MHz}$ ,  $P_{LO} = 0\text{ dBm}$ ,  $STBY = GND$ ,  $V_{IH} = 3.3\text{ V}$ ,  $V_{IL} = 0.0\text{ V}$  unless otherwise noted. Trace, Connector, and external transformer losses are de-embedded.

| Parameter                    | Symbol               | Conditions                                                                                    | Min          | Typ  | Max                    | Units         |
|------------------------------|----------------------|-----------------------------------------------------------------------------------------------|--------------|------|------------------------|---------------|
| Logic Input High             | $V_{IH}$             | All Control Pins                                                                              | <b>2</b>     |      |                        | V             |
| Logic Input Low              | $V_{IL}$             | All Control Pins                                                                              |              |      | <b>0.5</b>             | V             |
| Logic Current                | $I_{IH}, I_{IL}$     | All Control Pins                                                                              | <b>-130</b>  |      | <b>+10</b>             | $\mu\text{A}$ |
| Standby Mode Logic           | STBY                 | STBY = $V_{IH}$                                                                               | Power OFF    |      |                        |               |
|                              |                      | STBY = $V_{IL}$                                                                               | Power ON     |      |                        |               |
| Supply Current               | $I_{CC\_ON}$         |                                                                                               | <b>180</b>   | 216  | <b>250<sup>1</sup></b> | mA            |
|                              | $I_{CC\_STBY}$       | Standby Mode                                                                                  |              | 20   | <b>25</b>              |               |
| Attenuator Range             |                      |                                                                                               |              | 25.5 |                        | dB            |
| Attenuator Step              | LSB                  |                                                                                               |              | 0.5  |                        | dB            |
| Gain                         | $G_{max}$            | ATTN = 0 dB                                                                                   | <b>8.7</b>   | 10.2 | <b>11.7</b>            | dB            |
|                              | $G_{min}$            | ATTN = 25.5 dB                                                                                | <b>-16.5</b> | -15  | <b>-13.5</b>           |               |
| Return Loss, RF ports        | $S_{RFX}, S_{RFY}$   |                                                                                               |              | 16   |                        | dB            |
| Return Loss, LO port         | $S_{LO}$             |                                                                                               |              | 15   |                        | dB            |
| Return Loss, IF ports        | $S_{IFI}, S_{IFI}$   | Single Ended                                                                                  |              | 20   |                        | dB            |
| Noise Figure                 | $NF_0$               | ATTN = 0 dB                                                                                   |              | 19   |                        | dB            |
| Output IP3                   | OIP3 <sub>0</sub>    | ATTN = 0 dB                                                                                   | <b>36</b>    | 41   |                        | dBm           |
|                              | OIP3 <sub>20</sub>   | ATTN = 20 dB, $P_{RF} = +9\text{ dBm}$                                                        |              | 42   |                        |               |
| Output IP2                   | OIP2 <sub>0</sub>    | ATTN = 0 dB                                                                                   |              | 59   |                        | dBm           |
| Second Harmonic              | H2 <sub>0</sub>      | ATTN = 0 dB, $P_{IF} = -6\text{ dBm}$                                                         |              | -72  |                        | dBc           |
| Input Compression            | IP1dB-C <sub>0</sub> | ATTN = 0 dB<br>Gain delta for RF input power set at +5 dBm and RF Input power set at -11 dBm. |              | 0.2  | <b>1</b>               | dB            |
| Gain Ripple                  | $G_{ripple}$         | $F_{LO} = 3380\text{ MHz}$<br>$F_{RF} = 3400\text{ to }3880\text{ MHz}$                       |              | 1.6  | 2.5 <sup>2</sup>       | dB            |
| Group Delay Distortion       | GDD                  | $F_{LO} = 3380\text{ MHz}$<br>$F_{RF} = 3400\text{ to }3880\text{ MHz}$                       |              | 5    |                        | ns            |
| Attenuator Step Accuracy     | DNL                  |                                                                                               |              | 0.2  |                        | dB            |
| Absolute Attenuator Accuracy | INL                  |                                                                                               | <b>-0.75</b> | -0.1 | <b>0.75</b>            | dB            |

Note 1: Items in min/max columns in **bold italics** are Guaranteed by Test.

Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.

Note 3: Timing measurements are measured after SPI programming is completed (data latched with LE = HIGH).

Note 4: Gain across the entire frequency band is affected by the inclusion of the RF switch.

## F1358 SPECIFICATION

Specifications apply at  $V_{CC} = +5.00\text{ V}$ ,  $T_{CASE} = +25\text{ }^{\circ}\text{C}$ ,  $F_{RF} = 3455\text{ MHz}$ ,  $G_{max}$ ,  $P_{RF} = -11\text{ dBm}$ ,  $F_{LO} = 3255\text{ MHz}$ ,  $P_{LO} = 0\text{ dBm}$ ,  $STBY = GND$ ,  $V_{IH} = 3.3\text{ V}$ ,  $V_{IL} = 0.0\text{ V}$  unless otherwise noted. Trace, Connector, and external transformer losses are de-embedded.

| Parameter                                       | Symbol             | Conditions                                                                                                                      | Min         | Typ | Max        | Units   |
|-------------------------------------------------|--------------------|---------------------------------------------------------------------------------------------------------------------------------|-------------|-----|------------|---------|
| Quadrature Amplitude Balance                    | $BAL_G$            | Over Oversampled Range                                                                                                          | <b>-0.3</b> |     | <b>0.3</b> | dB      |
| Quadrature Amplitude Balance over environmental | $BAL_{G\Delta}$    | $T_{Amb} = -40\text{ to }+85\text{ }^{\circ}\text{C}$<br>$P_{LO} = -3\text{ to }+3\text{ dBm}$                                  | -0.5        |     | +0.5       | dB      |
| Quadrature Phase Balance                        | $BAL_{\Phi}$       |                                                                                                                                 | -1          | 0.3 | 1.5        | degrees |
| Quadrature Phase Balance over environmental     | $BAL_{\Phi\Delta}$ | $T_{Amb} = -40\text{ to }+85\text{ }^{\circ}\text{C}$<br>$P_{LO} = -3\text{ to }+3\text{ dBm}$                                  | -1.5        | 0.5 | +2.5       | degrees |
| LO to IF Leakage                                | $ISO_{LI}$         | Output Balun not de-embedded.                                                                                                   |             | -37 | -32        | dBm     |
| RF to IF Isolation                              | $ISO_{RI}$         | Output Balun not de-embedded. Reference to $P_{IF}$ .                                                                           |             | -42 | -32        | dBc     |
| LO to RF Leakage                                | $ISO_{LR}$         |                                                                                                                                 |             | -41 |            | dBm     |
| RF Switch Isolation                             | $ISO_{RFX-RXY}$    |                                                                                                                                 |             | -40 |            | dB      |
| Switch Time                                     |                    | RF_INX: 3600 MHz, -11 dBm<br>LO: 3415 MHz, 0 dBm<br>50% CSb to 10%/90% settled to within 0.1dB of final value of power at IF_I. |             |     |            | ns      |
|                                                 | $\tau_{EN\_ON}$    | EN Bit set high                                                                                                                 |             | 100 |            |         |
|                                                 | $\tau_{EN\_OFF}$   | EN Bit set low                                                                                                                  |             | 50  |            |         |
|                                                 | $\tau_{RF\_XY}$    | Switched from RF_INX to RF_INY. No power at RF_INY.                                                                             |             | 150 |            |         |
|                                                 | $\tau_{RF\_YX}$    | Switched from RF_INY to RF_INX. No power at RF_INY                                                                              |             | 200 |            |         |
| DSA Settling time                               | $\tau_{SET}$       | RF_INX: 3600 MHz, -11 dBm<br>LO: 3415 MHz, 0 dBm<br>50% CSb to 10%/90% settled to within 0.1dB of final value of power at IF_I. |             |     |            | ns      |
|                                                 | $\tau_{SET1}$      | ATTN= 0.0 dB to 25.5 dB                                                                                                         |             | 300 |            |         |
|                                                 | $\tau_{SET2}$      | ATTN= 25.5 dB to 0.0 dB                                                                                                         |             | 300 |            |         |
|                                                 | $\tau_{SET3}$      | ATTN= 15.5 dB to 16.0 dB                                                                                                        |             | 250 |            |         |
|                                                 | $\tau_{SET4}$      | ATTN= 16.0 dB to 15.5 dB                                                                                                        |             | 250 |            |         |
| Control Interface                               | $SPI_{BIT}$        |                                                                                                                                 |             | 16  |            | bit     |
| Serial Clock Speed                              | $SPI_{CLK}$        |                                                                                                                                 |             | 20  | <b>50</b>  | MHz     |

Note 1: Items in min/max columns in **bold italics** are Guaranteed by Test.

Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.

Note 3: Timing measurements are measured after SPI programming is completed (data latched with CSb = HIGH).

Note 4: Gain across the entire frequency band is affected by the inclusion of the RF switch.

## POWER-ON SEQUENCE

The power-on sequence will ensure that the F1358 works in the default mode once powered on. If the F1358 is programmed after applying DC power, the following power-on sequence is not needed.

Note: To use power on sequence, SW\_LATCH cannot be grounded permanently.

The power-on sequence should be:

1. CSb & SW\_LATCH must be set low at power-on.
2. Once powered on, first set SW\_LATCH high, then set CSb high.
3. Proceed with normal programming.

The default state after using power-on sequence:

- Maximum attenuation
- RF\_INX selected
- Normal operation (not Standby Mode)

## REGARDING PHASE OF I & Q:

- When LO is high-side injected, IF\_I leads IF\_Q by 90 degrees
- When LO is low-side injected, IF\_Q leads IF\_I by 90 degrees

## OPERATING MODE

There are two hardware pin, STBY on Pin 14 SW\_Latch on Pin 1, which allows multiple operating modes.

**Table 1 - Operating Mode Logic Table**

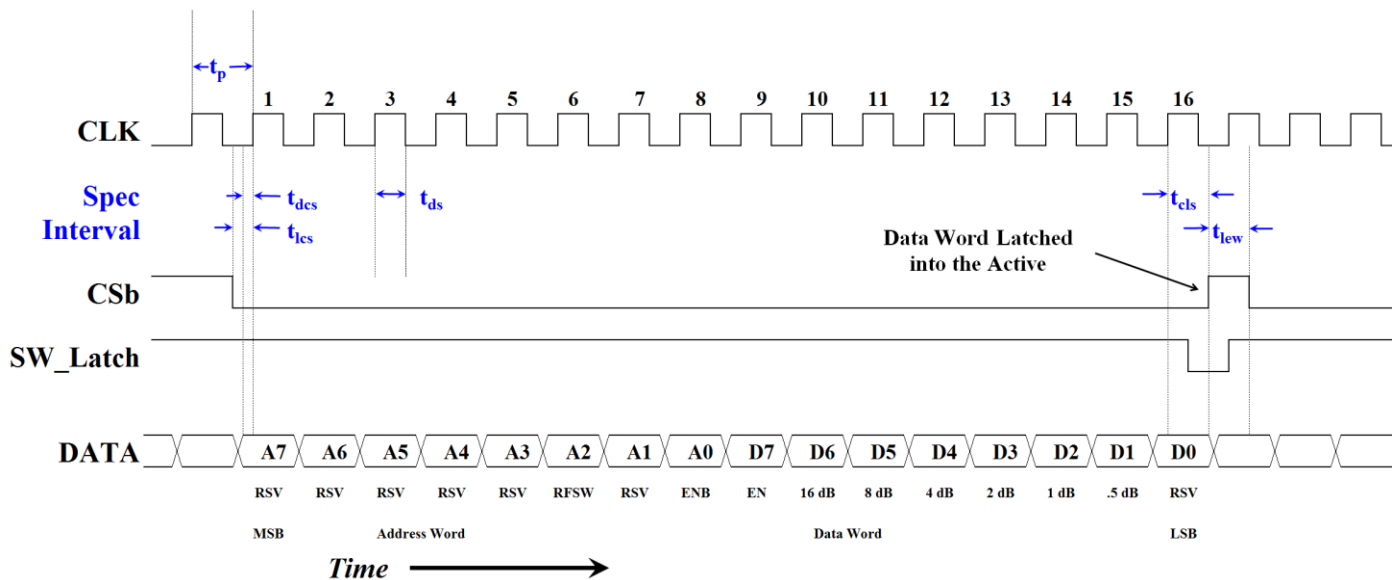
| STBY | SW_Latch | Mode           | Write Access                  | Comment                                                                                                                |
|------|----------|----------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------|
| 0    | 0        | Operating Mode | A2,A0 Enabled, D7:D0 Enabled  | RF Switch control (A2).<br>Software Standby allowed (A0).<br>Attenuator control (D7:D0).                               |
| 0    | 1        | Operating Mode | A2,A0 Disabled, D7:D0 Enabled | No RF Switch control.<br>No Software Standby allowed.<br>Attenuator control (D7:D0).                                   |
| 1    | 0        | Off            | A2,A0 Enabled, D7:D0 Enabled  | RF Switch control (A2).<br>Software Standby allowed (A0).<br>Attenuator control (D7:D0).<br>Device is in Standby mode. |
| 1    | 1        | Off            | A2,A0 Disabled, D7:D0 Enabled | No RF Switch control.<br>No Software Standby allowed.<br>Attenuator control (D7:D0).<br>Device is in Standby mode.     |

## SERIAL CONTROL MODE

Data is clocked in MSB first via serial mode. Serial data is formatted as a 16-bit word. The 16-bit word contains logic for switching the RF switch, 6-bit attenuator setting, and Enabling (software standby). Each word contains the following sequence:

**Table 2 - 16 Bit SPI Word Sequence**

|    |                               |
|----|-------------------------------|
| A7 | Reserved                      |
| A6 | Reserved                      |
| A5 | Reserved                      |
| A4 | Reserved                      |
| A3 | Reserved                      |
| A2 | RF Switch                     |
| A1 | Reserved                      |
| A0 | Enable Off=0, On=1            |
| D7 | Reserved                      |
| D6 | Attenuator 16 dB Control Bit  |
| D5 | Attenuator 8 dB Control Bit   |
| D4 | Attenuator 4 dB Control Bit   |
| D3 | Attenuator 2 dB Control Bit   |
| D2 | Attenuator 1 dB Control Bit   |
| D1 | Attenuator 0.5 dB Control Bit |
| D0 | Reserved                      |



**Figure 1 - Serial Register Timing Diagram**

**Table 3 - Serial Mode Timing Table**

| Interval Symbol | Description                                                                                                      | Min Spec  | Max Spec | Units |
|-----------------|------------------------------------------------------------------------------------------------------------------|-----------|----------|-------|
| $t_p$           | Clock Pulse Width                                                                                                | <b>10</b> |          | ns    |
| $t_{ds}$        | Clock high pulse width                                                                                           | <b>5</b>  |          | ns    |
| $t_{cls}$       | Clock to CSb Hold Time. From the rising edge of CLK pulse for D0 to Csb rising edge minus half the clock period. | <b>10</b> |          | ns    |
| $t_{lew}$       | CSb pulse width                                                                                                  | <b>3</b>  |          | ns    |
| $t_{dcs}$       | Data Setup Time - From the starting edge of Data bit to rising edge of CLK                                       | <b>3</b>  |          | ns    |
| $t_{dht}$       | Data Hold Time - From rising edge of CLK to falling edge of the Data bit.                                        | <b>10</b> |          | ns    |

**To program the serial interface:**

If CSb is de-asserted (set to high), the serial interface will ignore the CLK line. Once CSb is asserted (set to low), the serial interface will recognize the CLK and any data present on DATA will be clocked into the registers with each rising CLK edge. After the 16<sup>th</sup> CLK cycle, and before the 17<sup>th</sup> CLK cycle, CSb must be de-asserted to successfully program the part with the desired bytes. If CSb is de-asserted before the 16<sup>th</sup> CLK cycle, or after the 17<sup>th</sup> CLK cycle, there is no guarantee that the correct bytes will be programmed and the user will have to re-program the interface in accordance with the aforementioned procedure.

**SW\_LATCH programming sequence**

- When SW\_LATCH is pinned high during the programming sequence, "RFSW" and "ENb" registers cannot be programmed and therefore will not toggle.
- If SW\_LATCH is pinned low during the programming sequence, the "RFSW" and "ENb" register will toggle. This can be prevented with the "Programming Sequence" below.

**Sequence for programming registers A2, A0**

1. SW\_Latch = 1; CSb = 0
2. CLK in 8- or 16-bit word, do not de-assert (pull high) CSb
3. Set SW\_LATCH = 0 while CSb = 0 remains)
4. With SW\_Latch = 0, set CSb = 1
5. Set SW\_Latch = 1
6. Program complete

**F1358 Attenuation Table**

The F1358 attenuation setting is controlled by 6 bits in the data word. The device provides for an attenuation range from 0 dB to 25.5 dB in 0.5 dB steps. A "high" or "1" bit corresponds to attenuation stepped IN, while a "low" or "0" bit corresponds to attenuation stepped OUT.

Because the first and last bits of the Data Word are not presently used by the F1358, two additional hex character pairs exist for each of those in this table. For example, data words of either H00, H80, or H01 (binary "00000000," "10000000," or "00000001") will place the F1358 in its minimum attenuation state. Likewise, data words of either H66, HE6, or H67 (binary "01100110" or "11100110" or "01100111") will place the F1358 in its maximum attenuation state of 25.5 added attenuation.



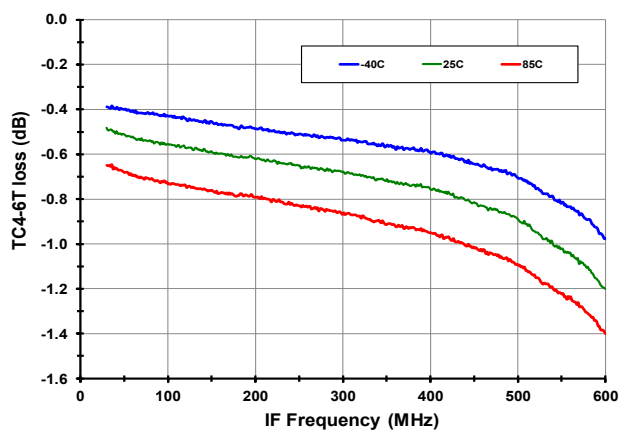
**Table 4 - Attenuation Digital Word Table**

| State | Attenuation (dB) | Hex | Binary D7 – D0 | State | Attenuation (dB) | Hex | Binary D7 – D0 |
|-------|------------------|-----|----------------|-------|------------------|-----|----------------|
| 0     | 0.0              | 00  | 00000000       | 26    | 13.0             | 34  | 00110100       |
| 1     | 0.5              | 02  | 00000010       | 27    | 13.5             | 36  | 00110110       |
| 2     | 1.0              | 04  | 00000100       | 28    | 14.0             | 38  | 00111000       |
| 3     | 1.5              | 06  | 00000110       | 29    | 14.5             | 3A  | 00111010       |
| 4     | 2.0              | 08  | 00001000       | 30    | 15.0             | 3C  | 00111100       |
| 5     | 2.5              | 0A  | 00001010       | 31    | 15.5             | 3E  | 00111110       |
| 6     | 3.0              | 0C  | 00001100       | 32    | 16.0             | 40  | 01000000       |
| 7     | 3.5              | 0E  | 00001110       | 33    | 16.5             | 42  | 01000010       |
| 8     | 4.0              | 10  | 00010000       | 34    | 17.0             | 44  | 01000100       |
| 9     | 4.5              | 12  | 00010010       | 35    | 17.5             | 46  | 01000110       |
| 10    | 5.0              | 14  | 00010100       | 36    | 18.0             | 48  | 01001000       |
| 11    | 5.5              | 16  | 00010110       | 37    | 18.5             | 4A  | 01001010       |
| 12    | 6.0              | 18  | 00011000       | 38    | 19.0             | 4C  | 01001100       |
| 13    | 6.5              | 1A  | 00011010       | 39    | 19.5             | 4E  | 01001110       |
| 14    | 7.0              | 1C  | 00011100       | 40    | 20.0             | 50  | 01010000       |
| 15    | 7.5              | 1E  | 00011110       | 41    | 20.5             | 52  | 01010010       |
| 16    | 8.0              | 20  | 00100000       | 42    | 21.0             | 54  | 01010100       |
| 17    | 8.5              | 22  | 00100010       | 43    | 21.5             | 56  | 01010110       |
| 18    | 9.0              | 24  | 00100100       | 44    | 22.0             | 58  | 01011000       |
| 19    | 9.5              | 26  | 00100110       | 45    | 22.5             | 5A  | 01011010       |
| 20    | 10.0             | 28  | 00101000       | 46    | 23.0             | 5C  | 01011100       |
| 21    | 10.5             | 2A  | 00101010       | 47    | 23.5             | 5E  | 01011110       |
| 22    | 11.0             | 2C  | 00101100       | 48    | 24.0             | 60  | 01100000       |
| 23    | 11.5             | 2E  | 00101110       | 49    | 24.5             | 62  | 01100010       |
| 24    | 12.0             | 30  | 00110000       | 50    | 25.0             | 64  | 01100100       |
| 25    | 12.5             | 32  | 00110010       | 51    | 25.5             | 66  | 01100110       |

## TYPICAL OPERATING CONDITIONS (TOC)

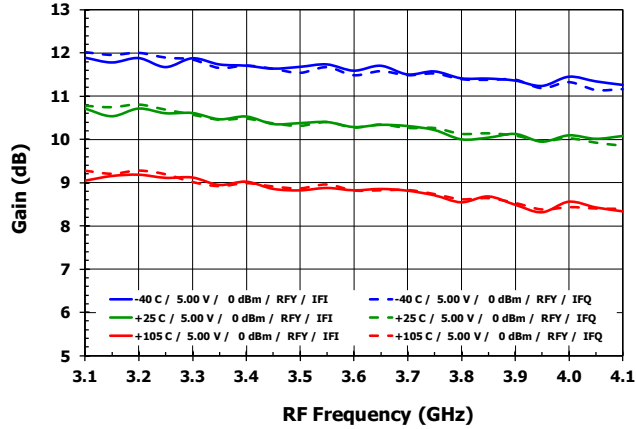
Unless otherwise noted for the TOC graphs on the following pages, the following conditions apply.

- **IF = 200 MHz**
- **Tone spacing = 5 MHz**
- **Pin = -11 dBm / Tone**
- **Pout ~ 0 dBm / Tone**
- **RF\_INX, IF\_Q selected**
- **Minimum Attenuation selected (0 dB ATTN)**
- **VCC = 5.00 V**
- **LO level = 0 dBm**
- **Case Temperature = +25 °C**
- **All Temperatures are Case Temperature ( $T_{CASE}$ )**
- **Output Transformers are de-embedded**
- **Input RF trace losses are de-embedded**

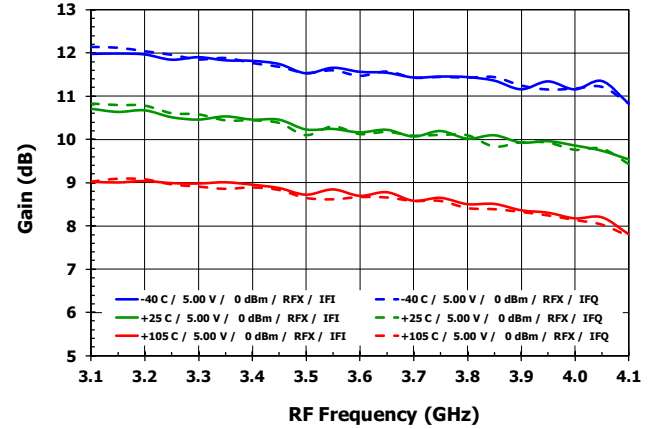


## TYPICAL OPERATING CONDITIONS (- 1 -)

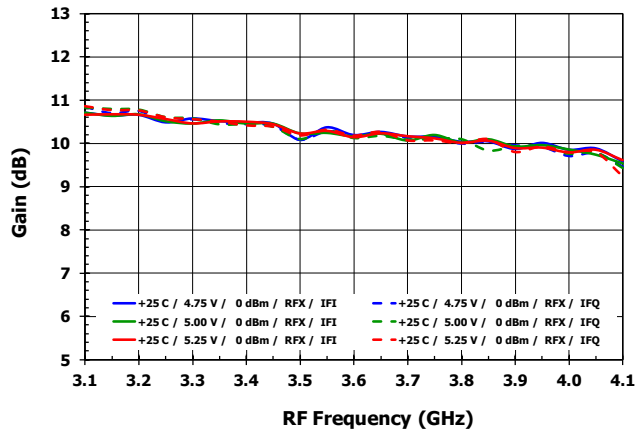
Gain vs.  $T_{case}$  [Low Side LO, RF<sub>X</sub>]



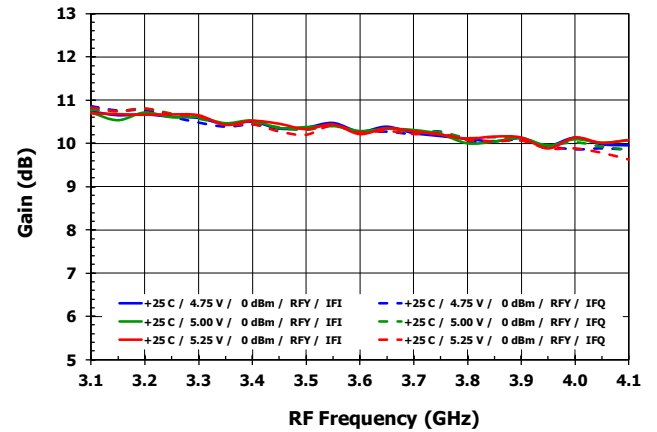
Gain vs.  $T_{case}$  [Low Side LO, RF<sub>Y</sub>]



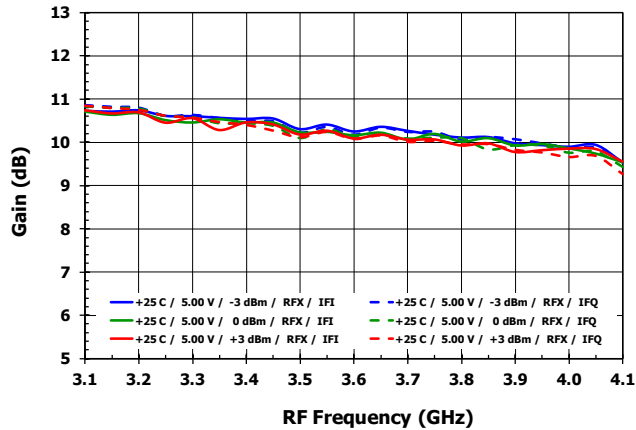
Gain vs.  $V_{cc}$  [Low Side LO, RF<sub>X</sub>]



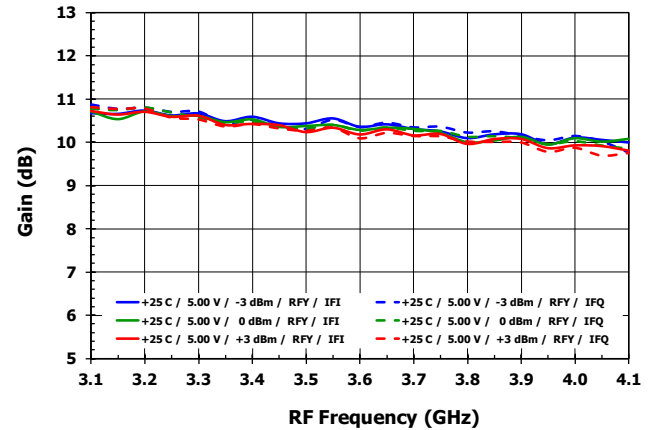
Gain vs.  $V_{cc}$  [Low Side LO, RF<sub>Y</sub>]



Gain vs. LO Power [Low Side LO, RF<sub>X</sub>]

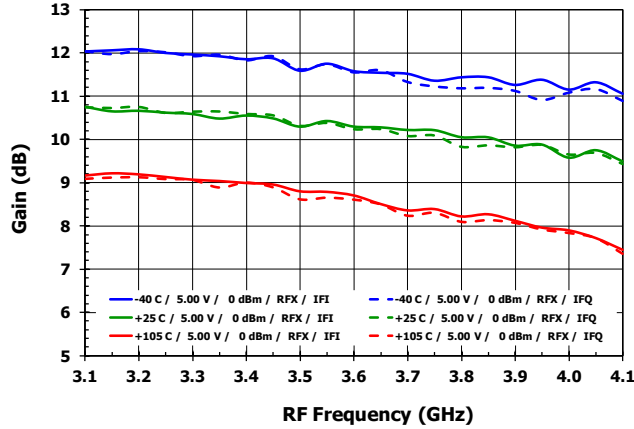


Gain vs. LO Power [Low Side LO, RF<sub>Y</sub>]

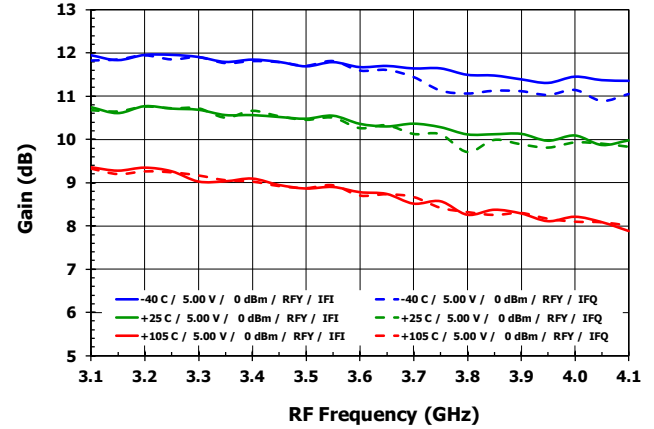


## TYPICAL OPERATING CONDITIONS (- 2 -)

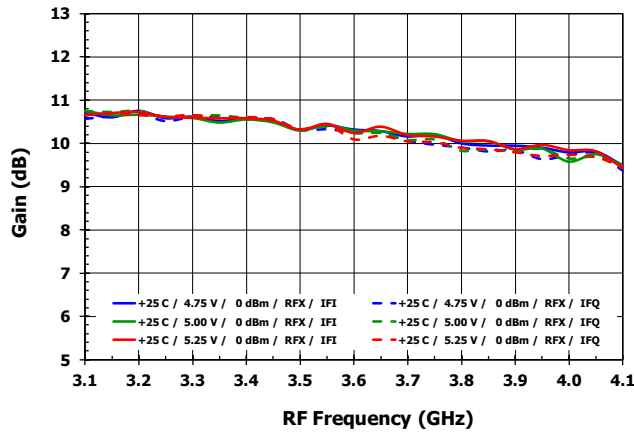
Gain vs.  $T_{case}$  [High Side LO,  $RF_X$ ]



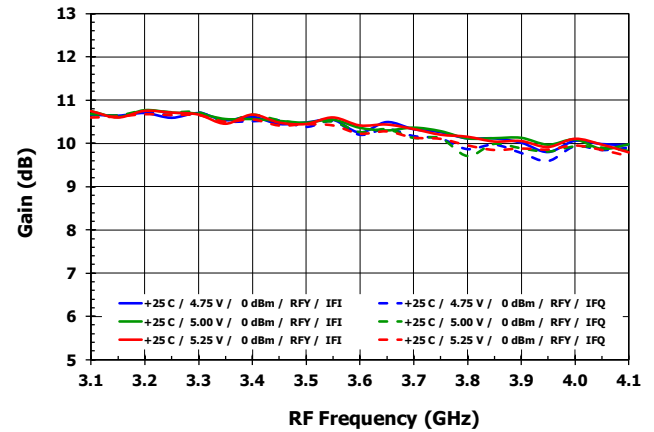
Gain vs.  $T_{case}$  [High Side LO,  $RF_Y$ ]



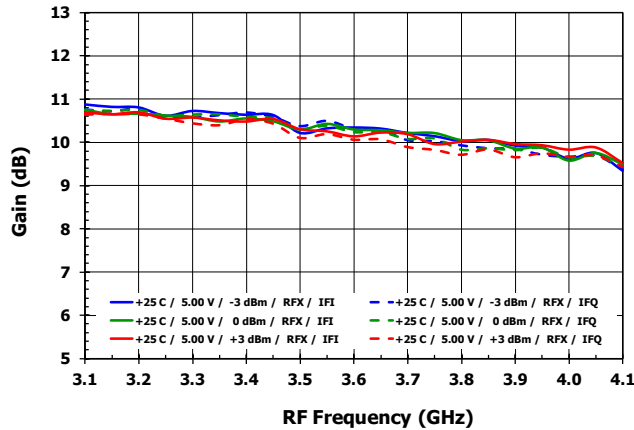
Gain vs.  $V_{cc}$  [High Side LO,  $RF_X$ ]



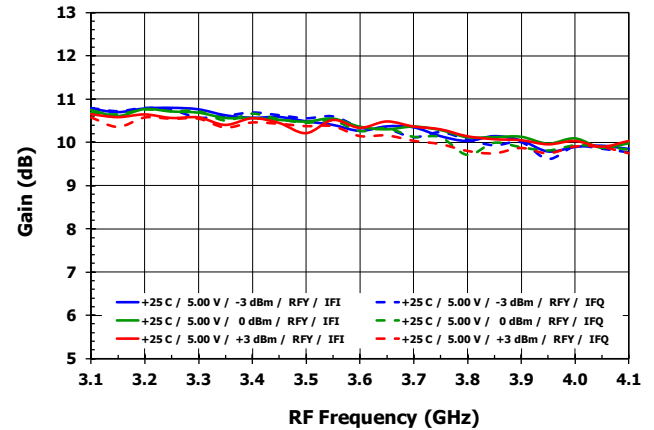
Gain vs.  $V_{cc}$  [High Side LO,  $RF_Y$ ]



Gain vs. LO Power [High Side LO,  $RF_X$ ]

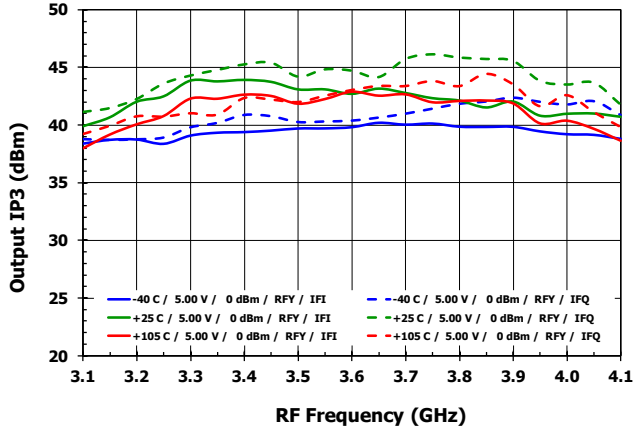


Gain vs. LO Power [High Side LO,  $RF_Y$ ]

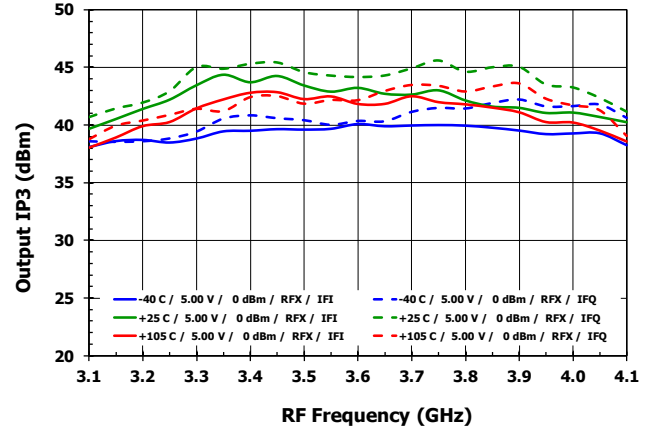


## TYPICAL OPERATING CONDITIONS (- 3 -)

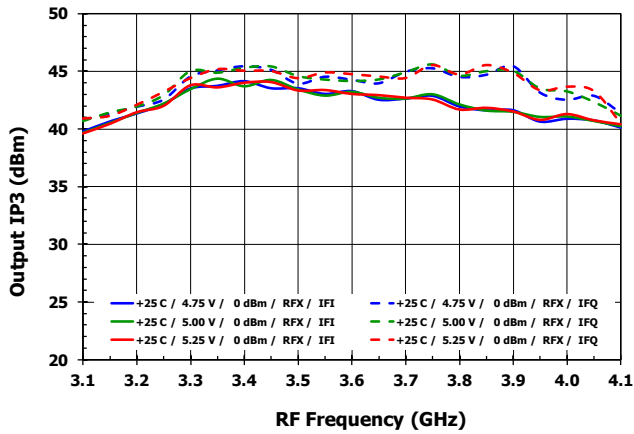
OIP3 vs.  $T_{case}$  [Low Side LO,  $RF_X$ ]



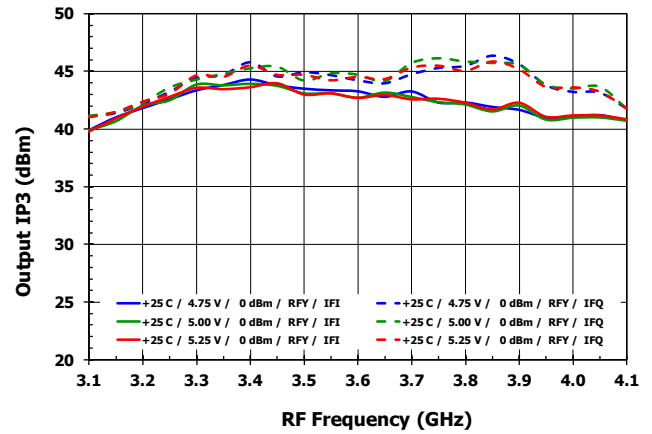
OIP3 vs.  $T_{case}$  [Low Side LO,  $RF_Y$ ]



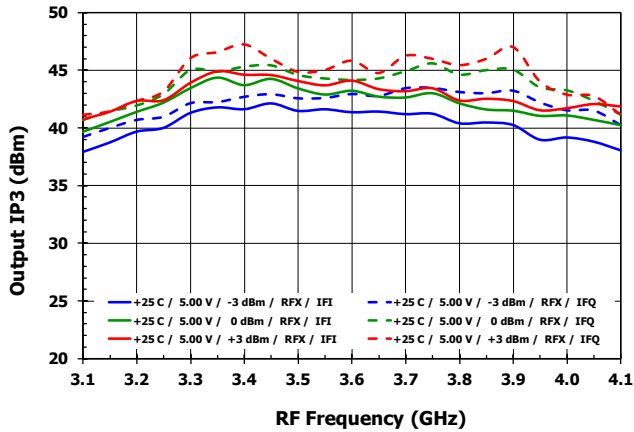
OIP3 vs.  $V_{cc}$  [Low Side LO,  $RF_X$ ]



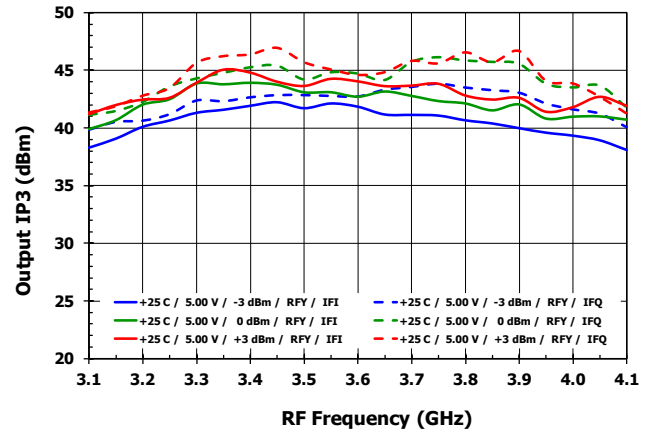
OIP3 vs.  $V_{cc}$  [Low Side LO,  $RF_Y$ ]



OIP3 vs. LO Power [Low Side LO,  $RF_X$ ]

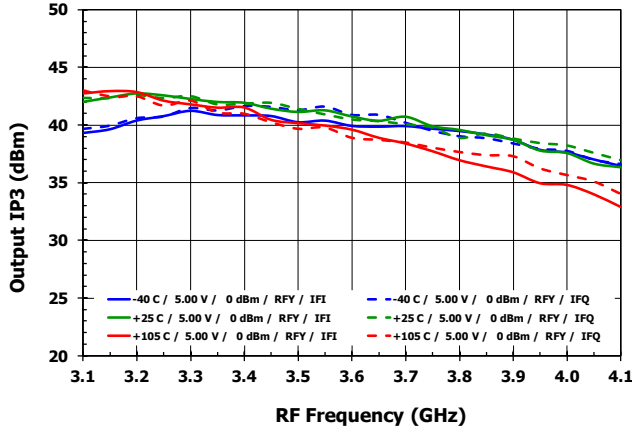


OIP3 vs. LO Power [Low Side LO,  $RF_Y$ ]

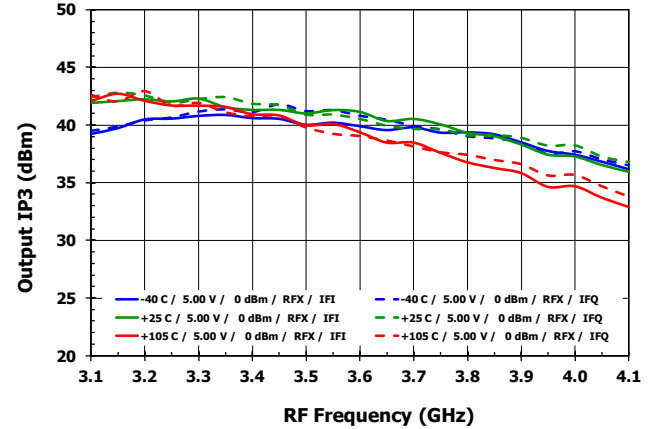


## TYPICAL OPERATING CONDITIONS (- 4 -)

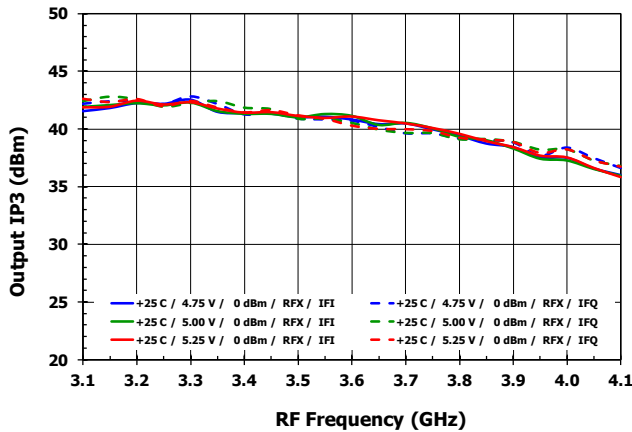
OIP3 vs.  $T_{case}$  [High Side LO,  $RF_X$ ]



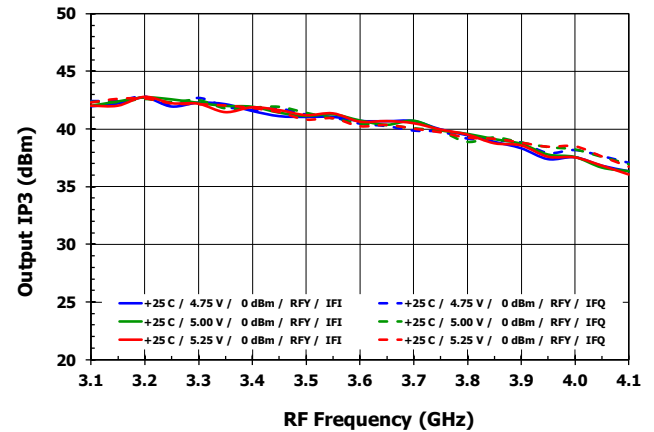
OIP3 vs.  $T_{case}$  [High Side LO,  $RF_Y$ ]



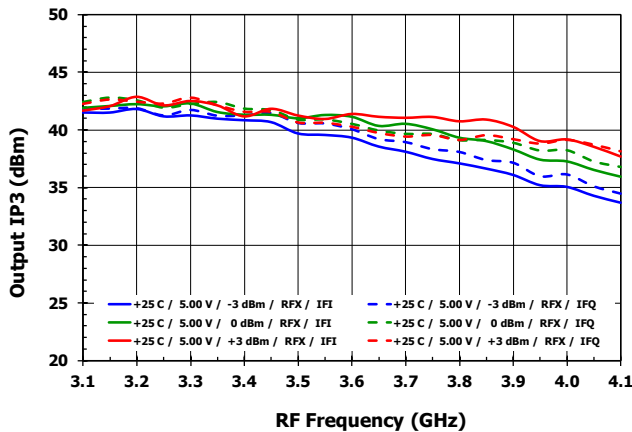
OIP3 vs.  $V_{cc}$  [High Side LO,  $RF_X$ ]



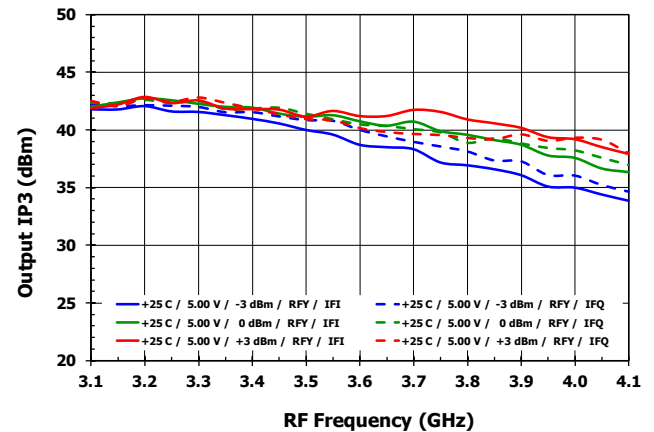
OIP3 vs.  $V_{cc}$  [High Side LO,  $RF_Y$ ]



OIP3 vs. LO Power [High Side LO,  $RF_X$ ]

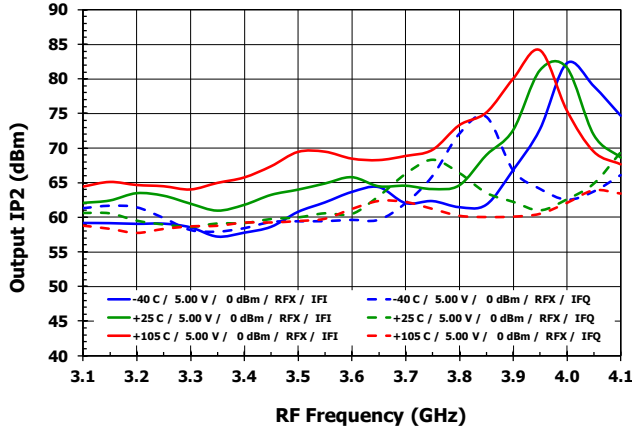


OIP3 vs. LO Power [High Side LO,  $RF_Y$ ]

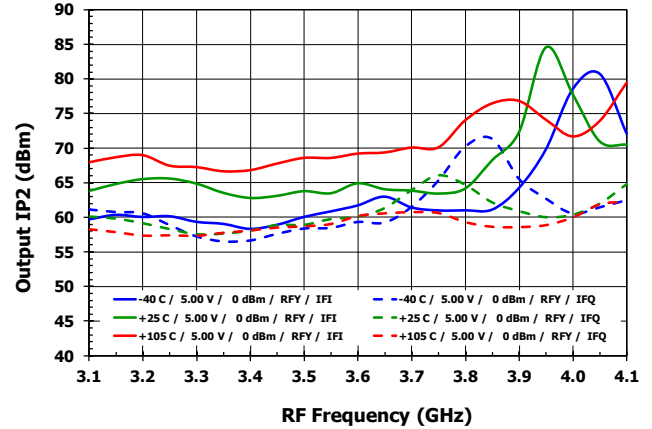


## TYPICAL OPERATING CONDITIONS (- 5 -)

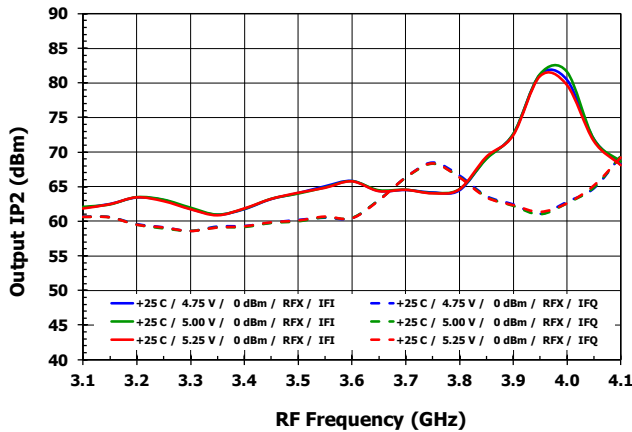
OIP2 vs.  $T_{case}$  [Low Side LO,  $RF_X$ ]



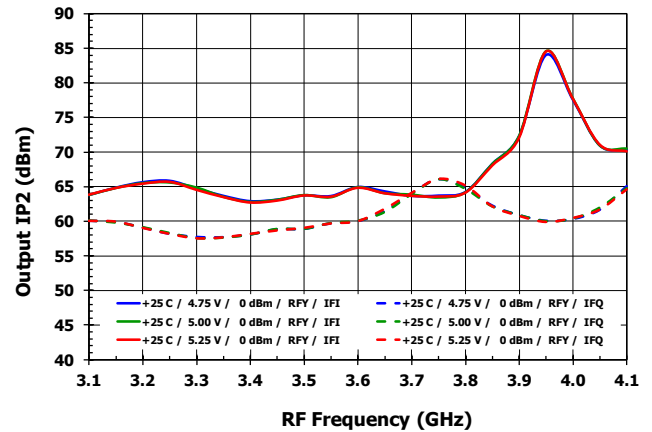
OIP2 vs.  $T_{case}$  [Low Side LO,  $RF_Y$ ]



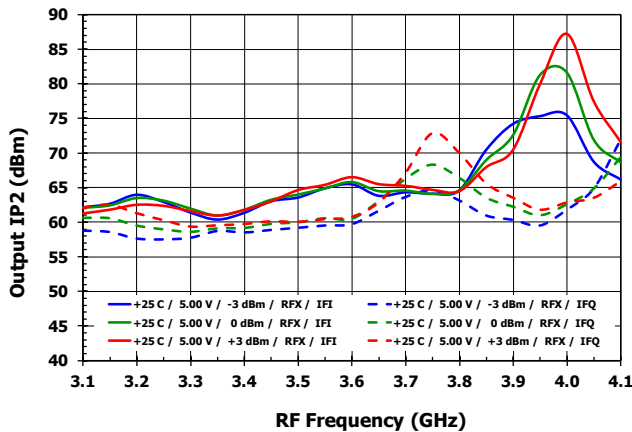
OIP2 vs.  $V_{cc}$  [Low Side LO,  $RF_X$ ]



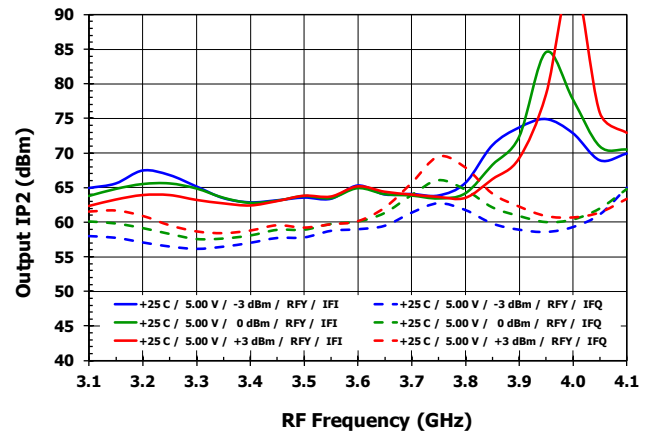
OIP2 vs.  $V_{cc}$  [Low Side LO,  $RF_Y$ ]



OIP2 vs. LO Power [Low Side LO,  $RF_X$ ]

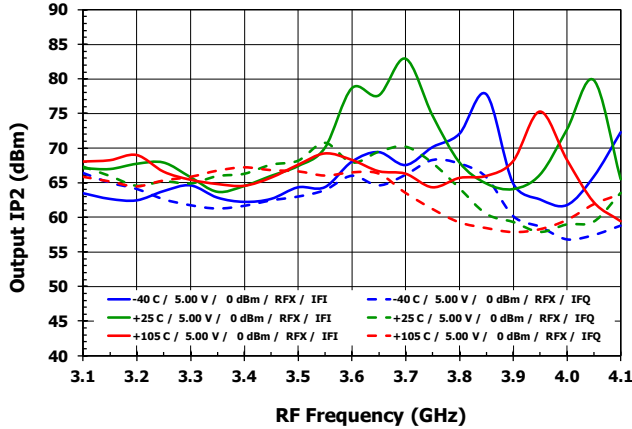


OIP2 vs. LO Power [Low Side LO,  $RF_Y$ ]

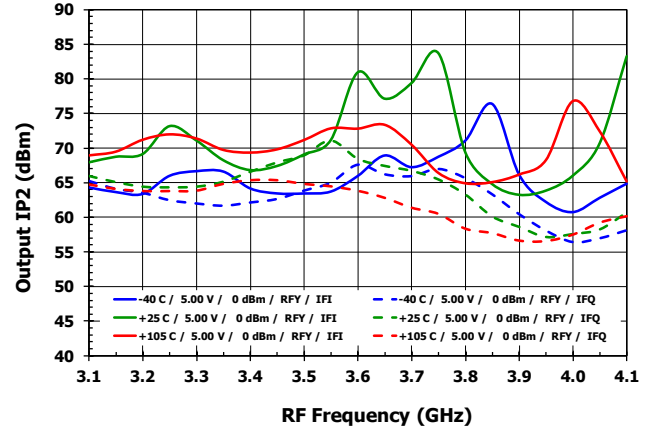


## TYPICAL OPERATING CONDITIONS (- 6 -)

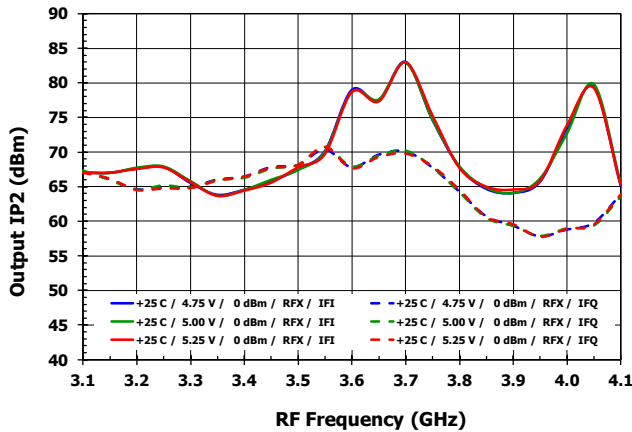
OIP2 vs.  $T_{case}$  [High Side LO,  $RF_X$ ]



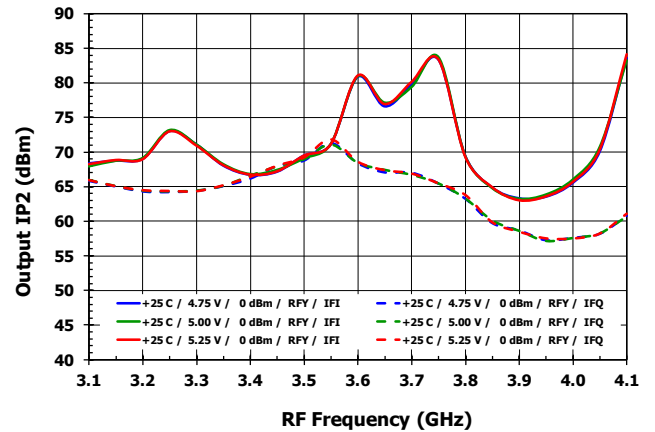
OIP2 vs.  $T_{case}$  [High Side LO,  $RF_Y$ ]



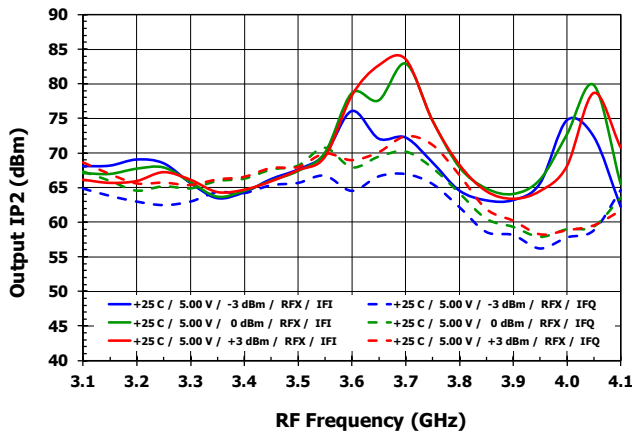
OIP2 vs.  $V_{cc}$  [High Side LO,  $RF_X$ ]



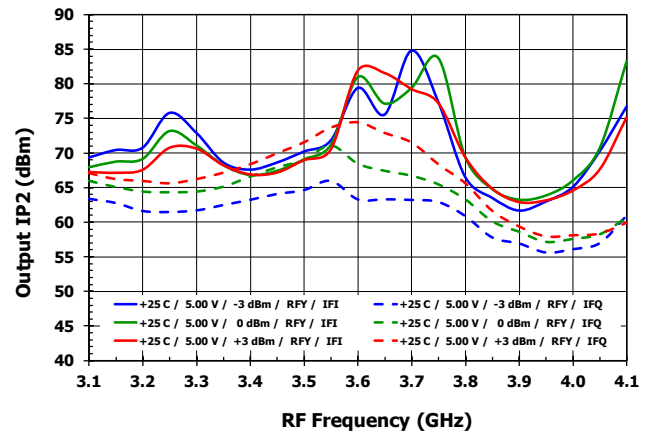
OIP2 vs.  $V_{cc}$  [High Side LO,  $RF_Y$ ]



OIP2 vs. LO Power [High Side LO,  $RF_X$ ]



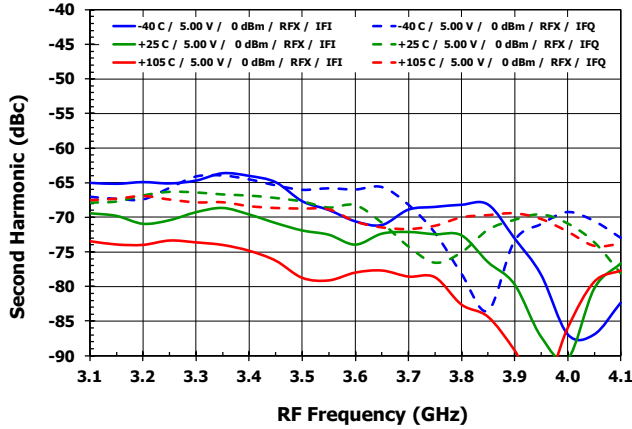
OIP2 vs. LO Power [High Side LO,  $RF_Y$ ]



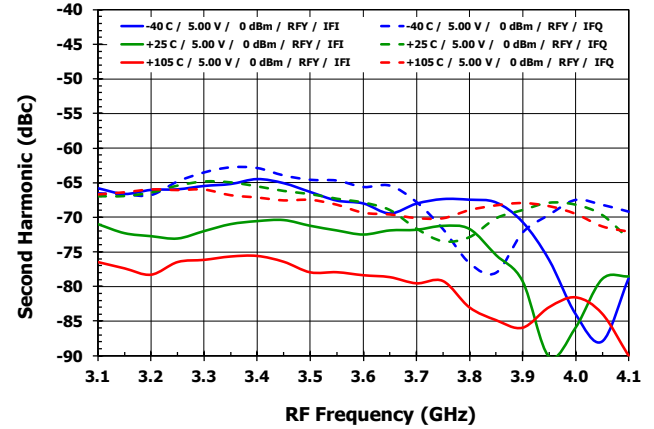


## TYPICAL OPERATING CONDITIONS (- 7 -)

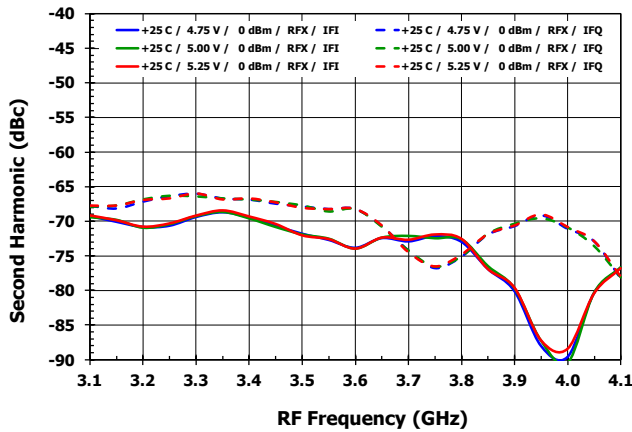
2<sup>nd</sup> Harmonic vs. T<sub>case</sub> [Low Side LO, RF<sub>X</sub>, P<sub>IF</sub>=-6 dBm]



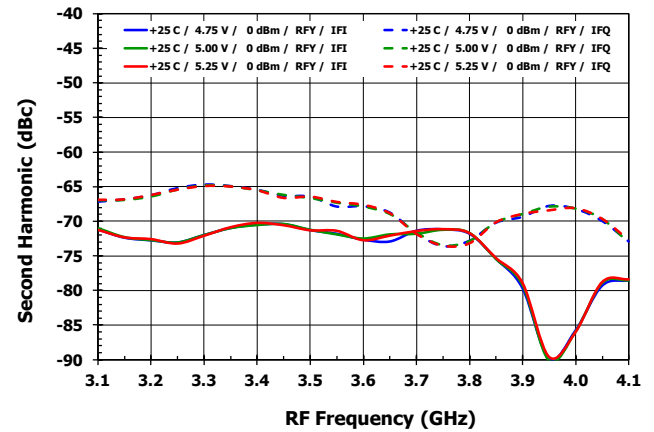
2<sup>nd</sup> Harmonic vs. T<sub>case</sub> [Low Side LO, RF<sub>Y</sub>, P<sub>IF</sub>=-6 dBm]



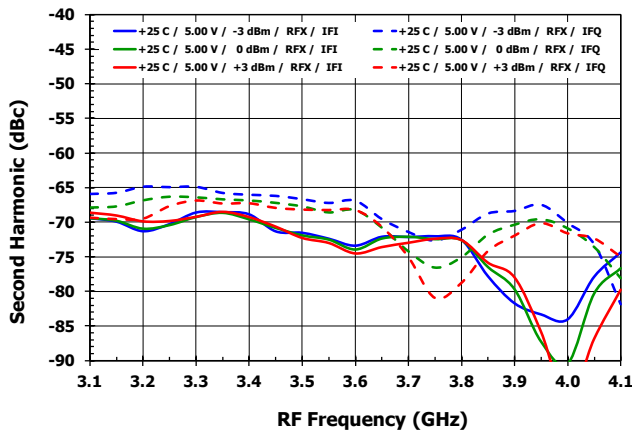
2<sup>nd</sup> Harmonic vs. V<sub>cc</sub> [Low Side LO, RF<sub>X</sub>, P<sub>IF</sub>=-6 dBm]



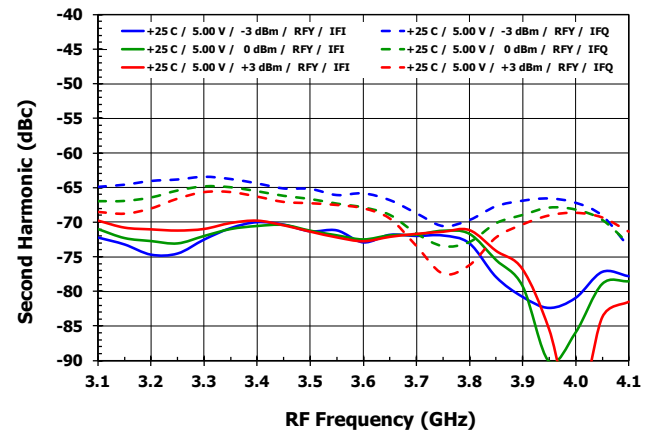
2<sup>nd</sup> Harmonic vs. V<sub>cc</sub> [Low Side LO, RF<sub>Y</sub>, P<sub>IF</sub>=-6 dBm]



2<sup>nd</sup> Harmonic vs. LO Power [Low Side LO, RF<sub>X</sub>, P<sub>IF</sub>=-6 dBm]

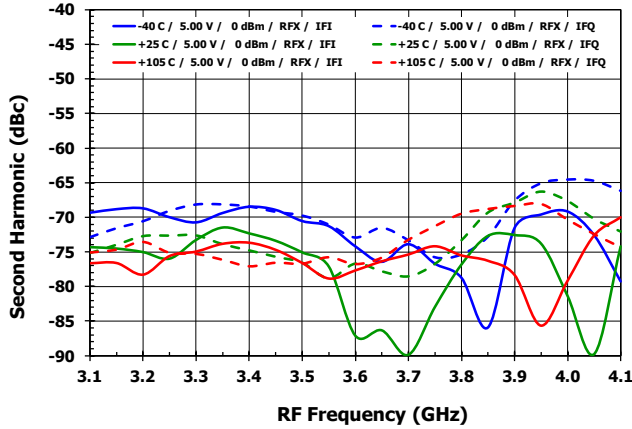


2<sup>nd</sup> Harmonic vs. LO Power [Low Side LO, RF<sub>Y</sub>, P<sub>IF</sub>=-6 dBm]

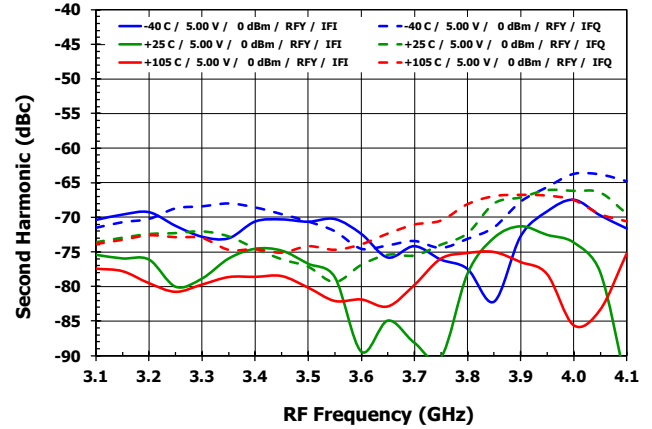


## TYPICAL OPERATING CONDITIONS (- 8 -)

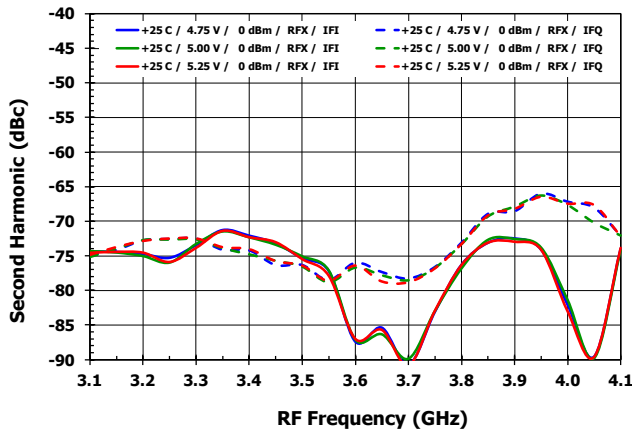
2<sup>nd</sup> Harmonic vs. T<sub>case</sub> [High Side LO, RF<sub>x</sub>, P<sub>IF</sub>=-6 dBm]



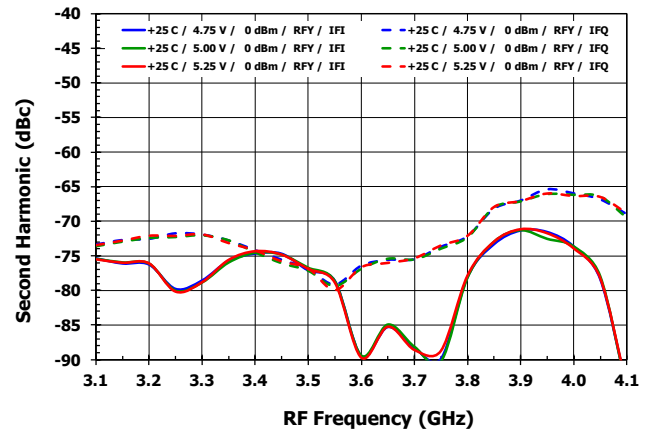
2<sup>nd</sup> Harmonic vs. T<sub>case</sub> [High Side LO, RF<sub>y</sub>, P<sub>IF</sub>=-6 dBm]



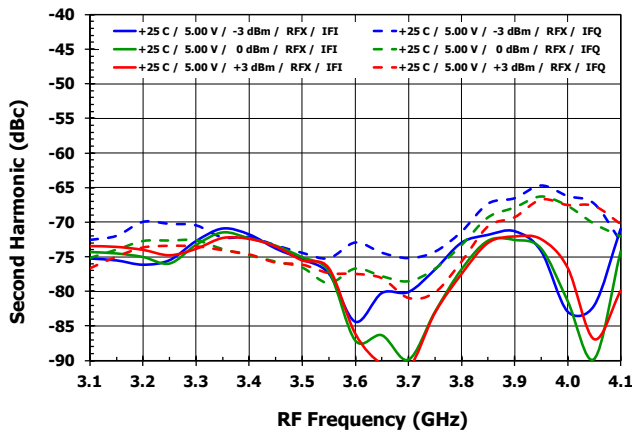
2<sup>nd</sup> Harmonic vs. V<sub>cc</sub> [High Side LO, RF<sub>x</sub>, P<sub>IF</sub>=-6 dBm]



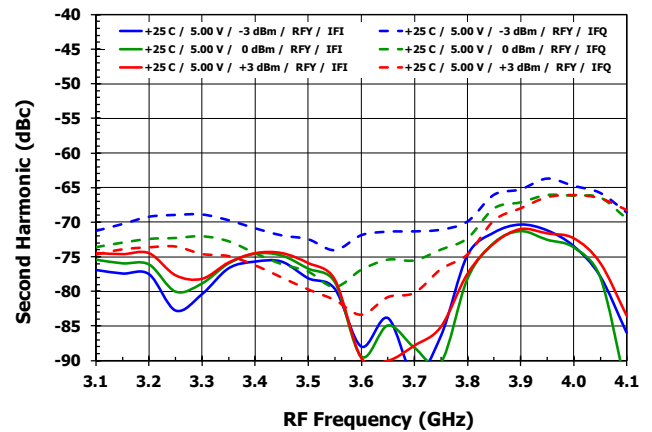
2<sup>nd</sup> Harmonic vs. V<sub>cc</sub> [High Side LO, RF<sub>y</sub>, P<sub>IF</sub>=-6 dBm]



2<sup>nd</sup> Harmonic vs. LO Power [High Side LO, RF<sub>x</sub>, P<sub>IF</sub>=-6 dBm]

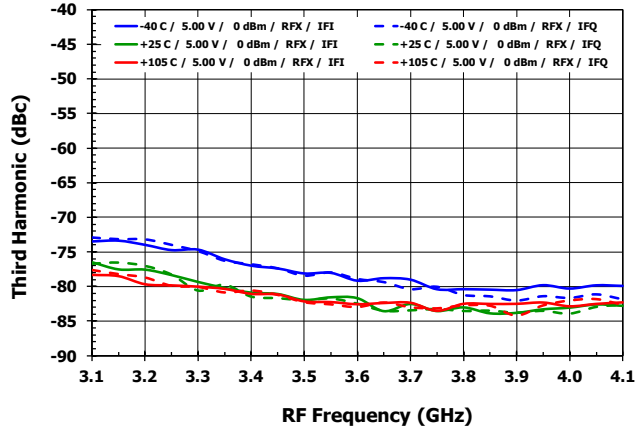


2<sup>nd</sup> Harmonic vs. LO Power [High Side LO, RF<sub>y</sub>, P<sub>IF</sub>=-6 dBm]

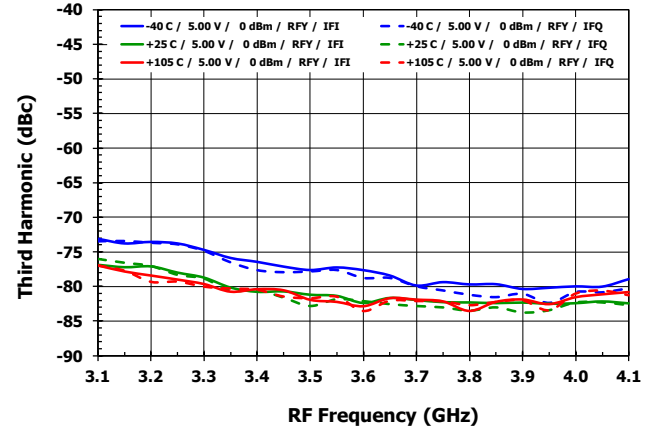


## TYPICAL OPERATING CONDITIONS (- 9 -)

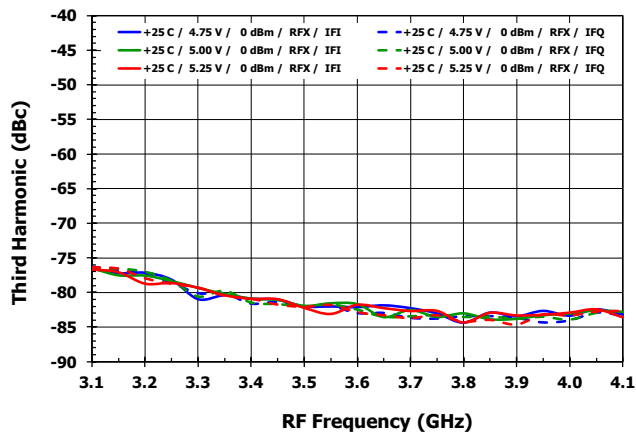
3<sup>rd</sup> Harmonic vs. T<sub>case</sub> [Low Side LO, RF<sub>X</sub>]



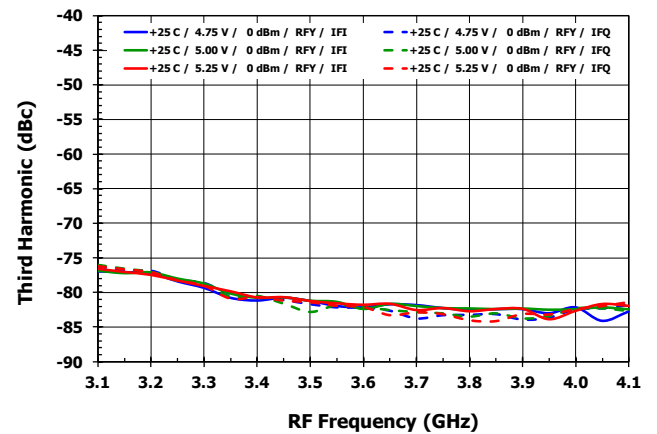
3<sup>rd</sup> Harmonic vs. T<sub>case</sub> [Low Side LO, RF<sub>Y</sub>]



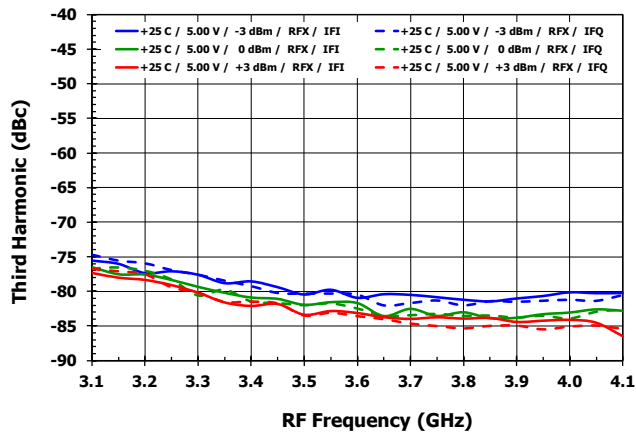
3<sup>rd</sup> Harmonic vs. V<sub>cc</sub>[Low Side LO, RF<sub>X</sub>]



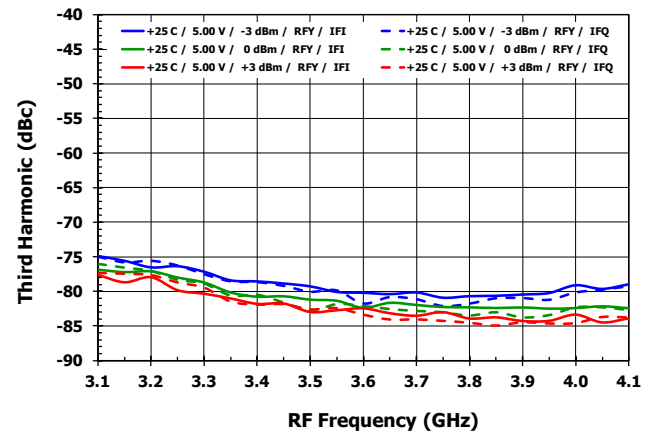
3<sup>rd</sup> Harmonic vs. V<sub>cc</sub>[Low Side LO, RF<sub>Y</sub>]



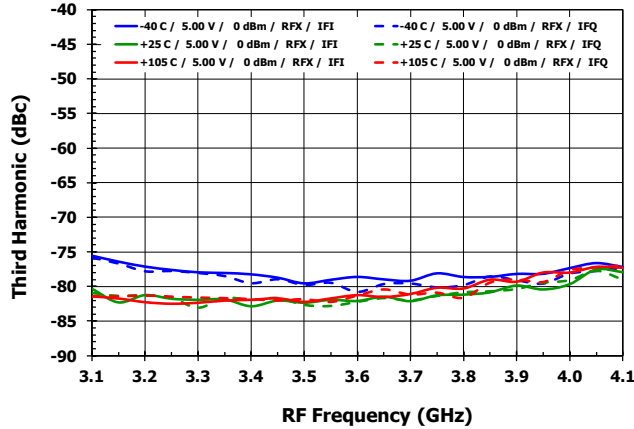
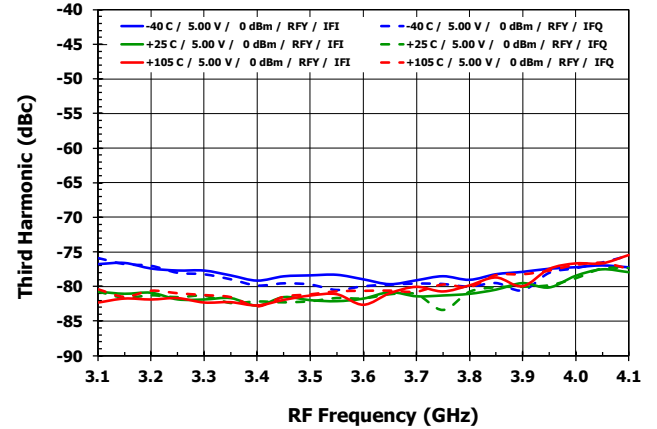
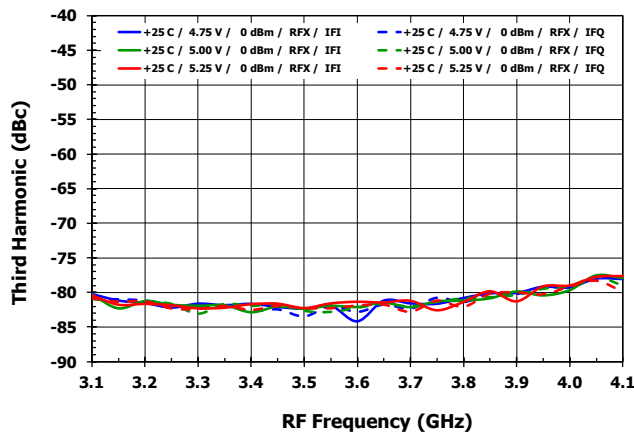
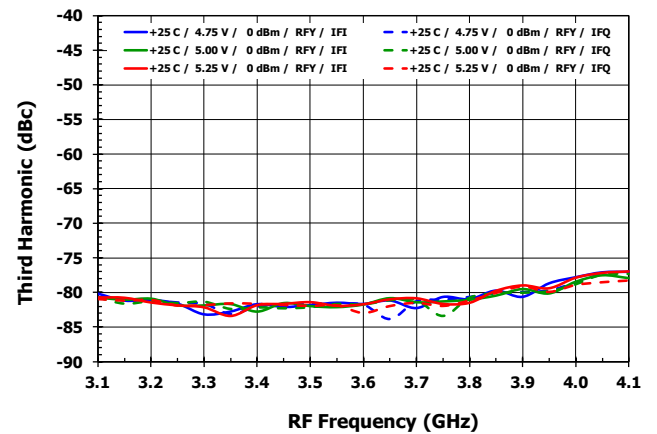
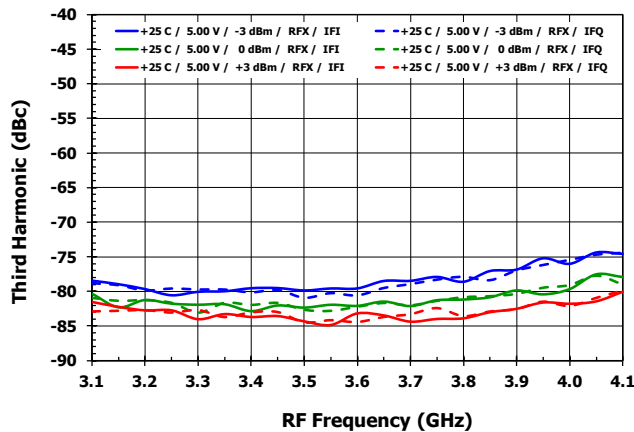
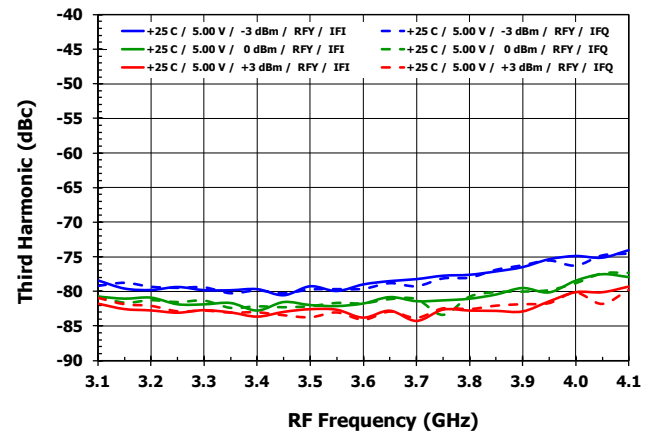
3<sup>rd</sup> Harmonic vs. LO Power [Low Side LO, RF<sub>X</sub>]



3<sup>rd</sup> Harmonic vs. LO Power [Low Side LO, RF<sub>Y</sub>]

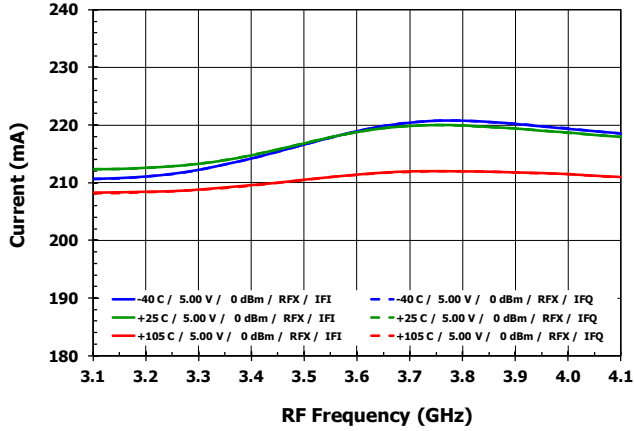


## TYPICAL OPERATING CONDITIONS (- 10 -)

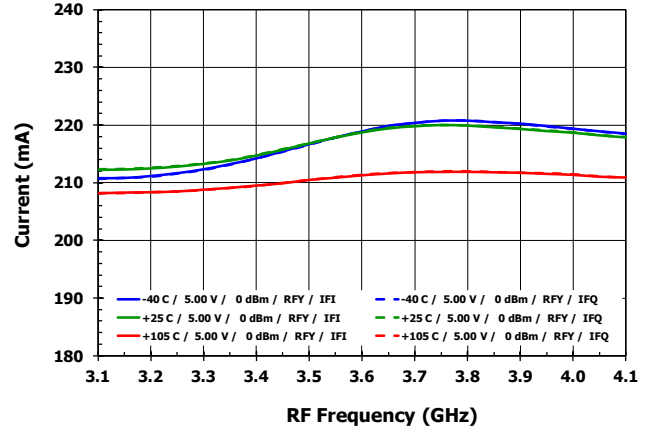
3<sup>rd</sup> Harmonic vs. T<sub>case</sub> [High Side LO, RF<sub>X</sub>]3<sup>rd</sup> Harmonic vs. T<sub>case</sub> [High Side LO, RF<sub>Y</sub>]3<sup>rd</sup> Harmonic vs. V<sub>cc</sub> [High Side LO, RF<sub>X</sub>]3<sup>rd</sup> Harmonic vs. V<sub>cc</sub> [High Side LO, RF<sub>Y</sub>]3<sup>rd</sup> Harmonic vs. LO Power [High Side LO, RF<sub>X</sub>]3<sup>rd</sup> Harmonic vs. LO Power [High Side LO, RF<sub>Y</sub>]

## TYPICAL OPERATING CONDITIONS (- 11 -)

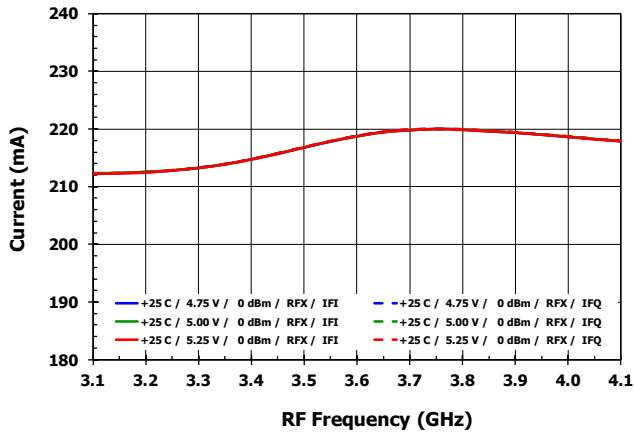
Current vs.  $T_{case}$  [Low Side LO, RF<sub>x</sub>]



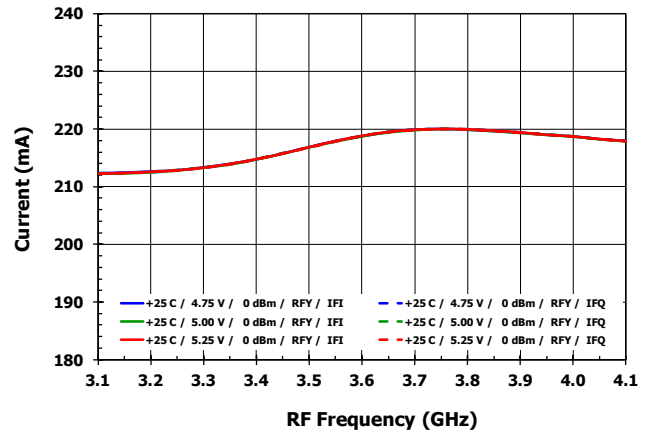
Current vs.  $T_{case}$  [Low Side LO, RF<sub>y</sub>]



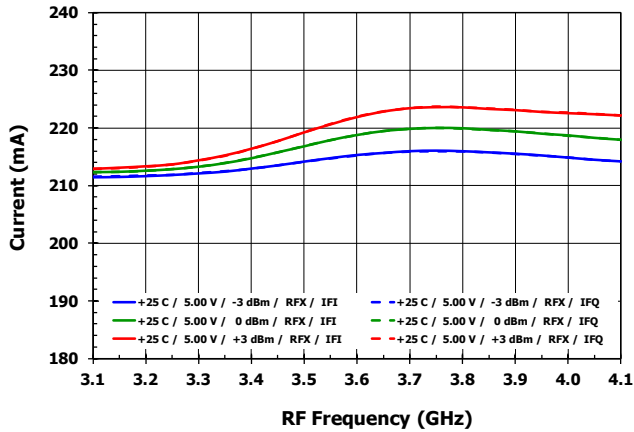
Current vs.  $V_{cc}$  [Low Side LO, RF<sub>x</sub>]



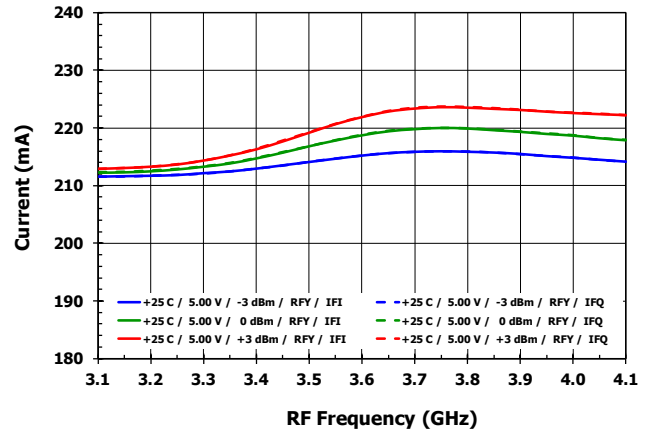
Current vs.  $V_{cc}$  [Low Side LO, RF<sub>y</sub>]



Current vs. LO Power [Low Side LO, RF<sub>x</sub>]

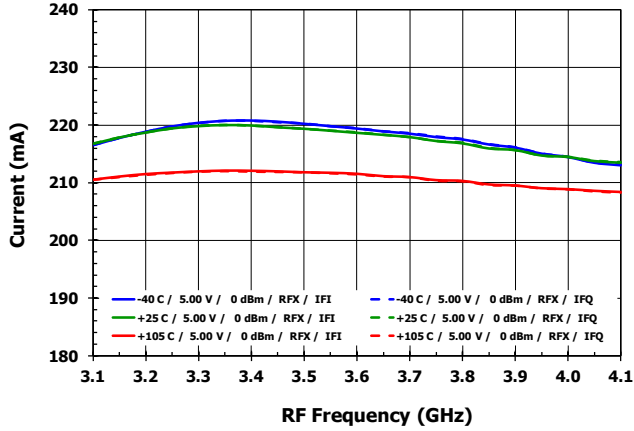


Current vs. LO Power [Low Side LO, RF<sub>y</sub>]

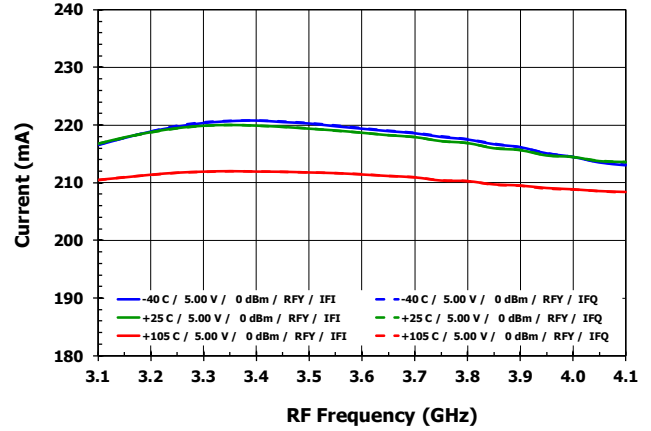


## TYPICAL OPERATING CONDITIONS (- 12 -)

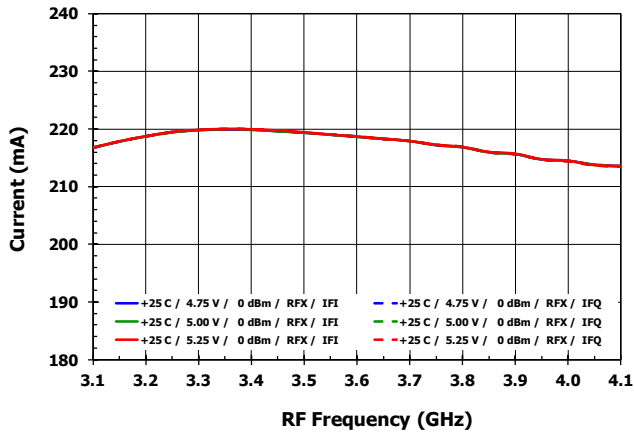
Current vs.  $T_{case}$  [High Side LO,  $RF_X$ ]



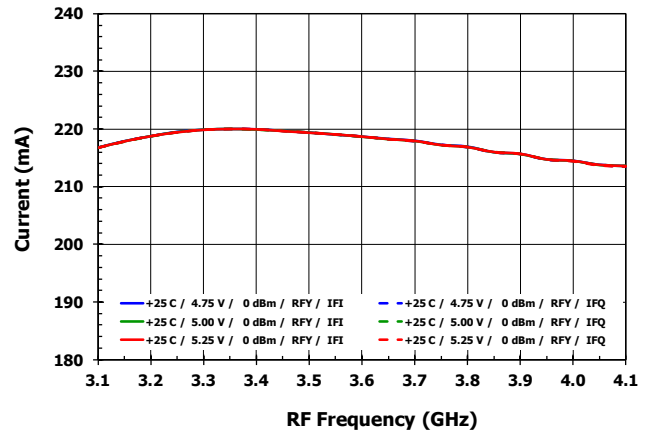
Current vs.  $T_{case}$  [High Side LO,  $RF_Y$ ]



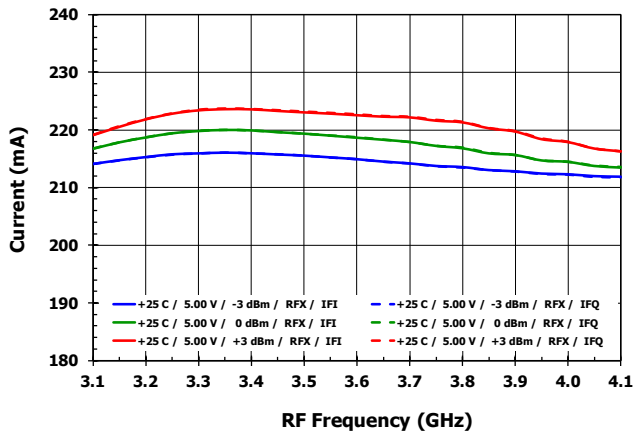
Current vs.  $V_{cc}$  [High Side LO,  $RF_X$ ]



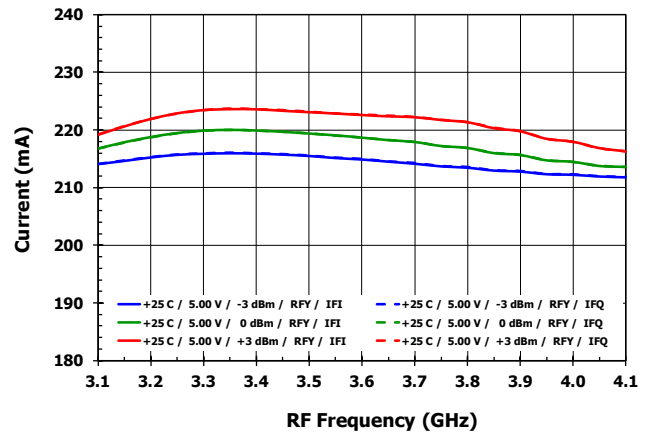
Current vs.  $V_{cc}$  [High Side LO,  $RF_Y$ ]



Current vs. LO Power [High Side LO,  $RF_X$ ]

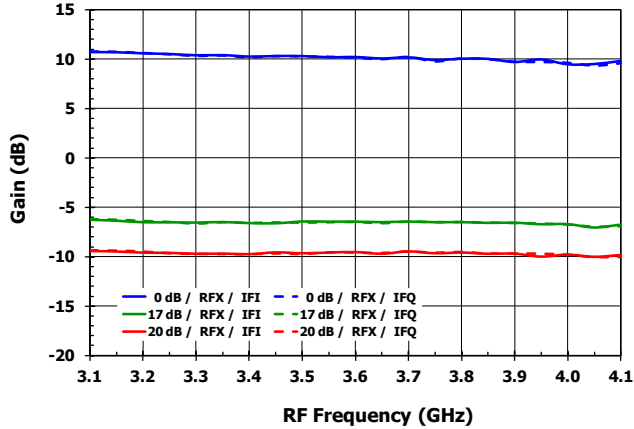


Current vs. LO Power [High Side LO,  $RF_Y$ ]

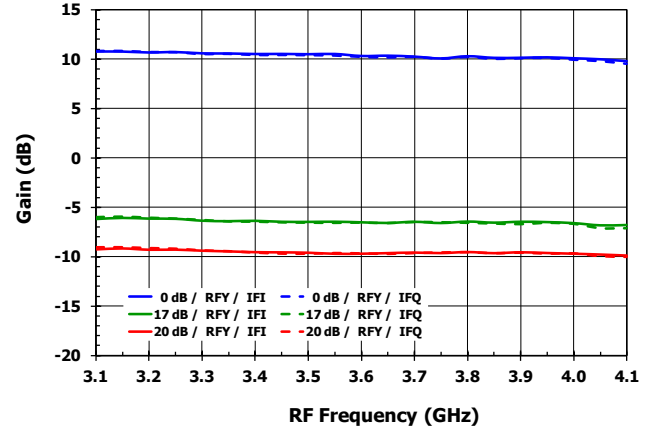


## TYPICAL OPERATING CONDITIONS (- 13 -)

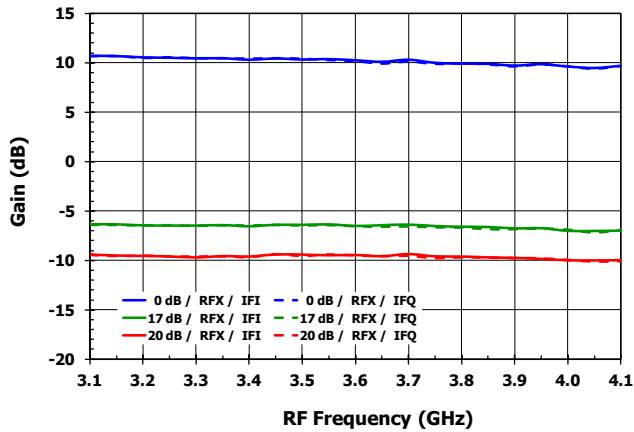
Gain vs. Attenuator Setting [Low Side LO, RF<sub>x</sub>]



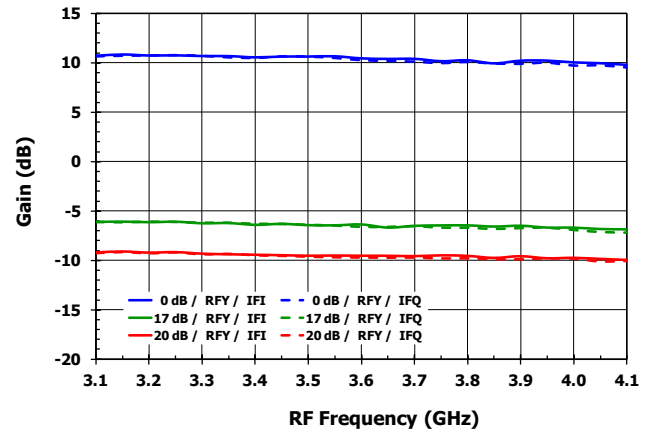
Gain vs. Attenuator Setting [Low Side LO, RF<sub>y</sub>]



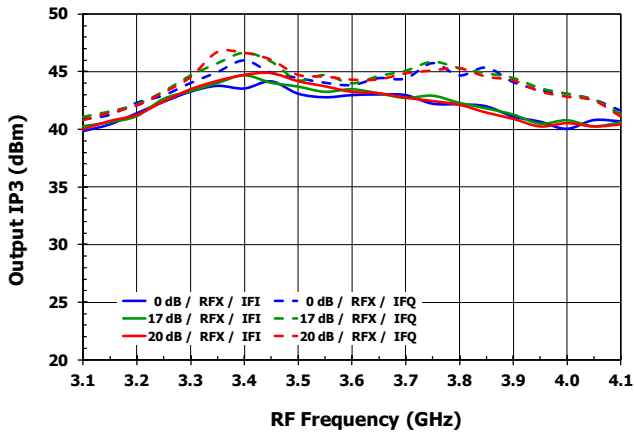
Gain vs. Attenuator Setting [High Side LO, RF<sub>x</sub>]



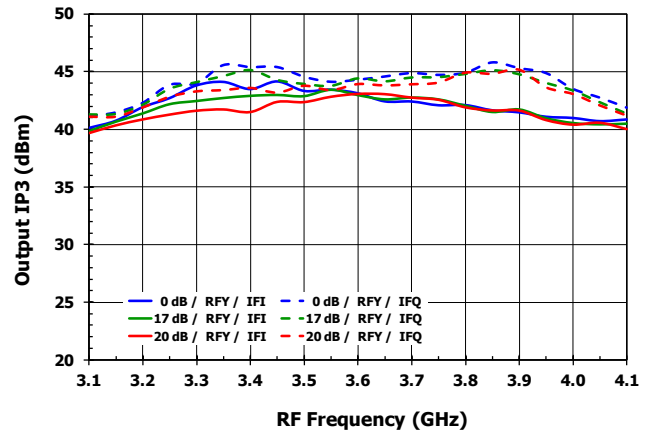
Gain vs. Attenuator Setting [High Side LO, RF<sub>y</sub>]



OIP3 vs. Attenuation Setting [Low Side LO, RF<sub>x</sub>]

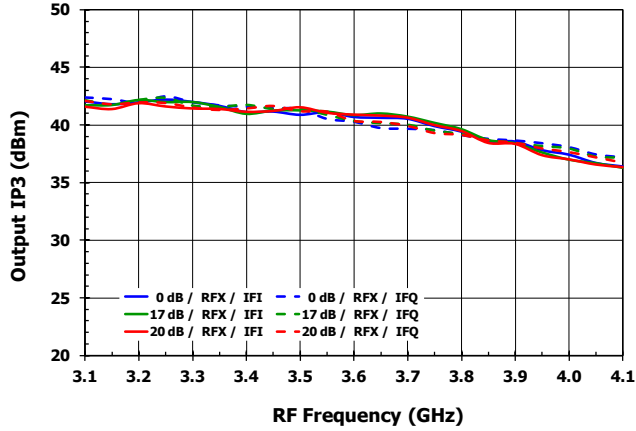


OIP3 vs. Attenuation Setting [Low Side LO, RF<sub>y</sub>]

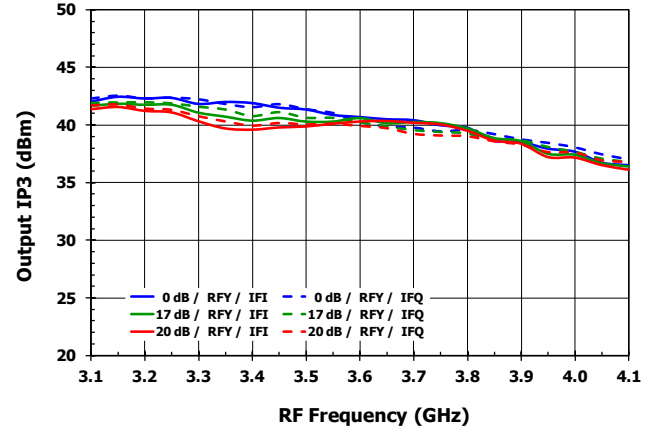


## TYPICAL OPERATING CONDITIONS (- 14 -)

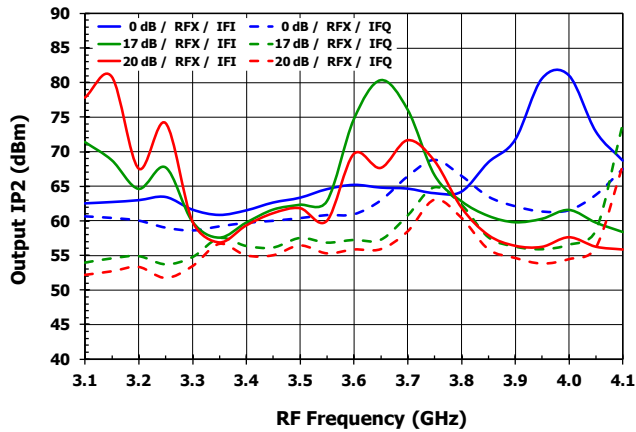
OIP3 vs. Attenuation Setting [High Side LO, RF<sub>X</sub>]



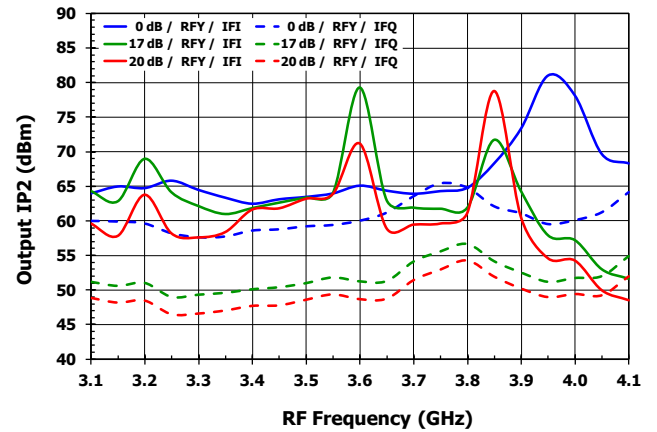
OIP3 vs. Attenuation Setting [High Side LO, RF<sub>V</sub>]



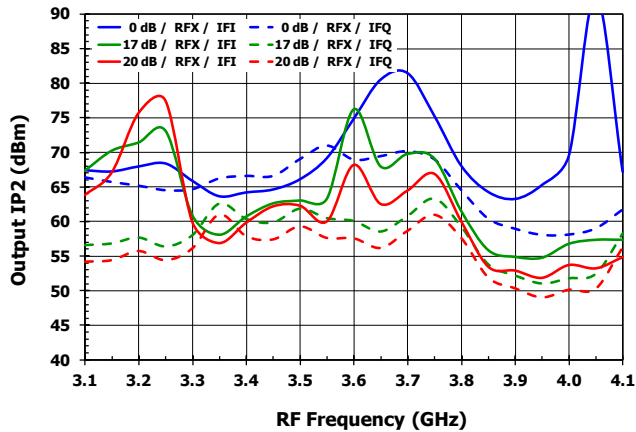
OIP2 vs. Attenuation Setting [Low Side LO, RF<sub>X</sub>]



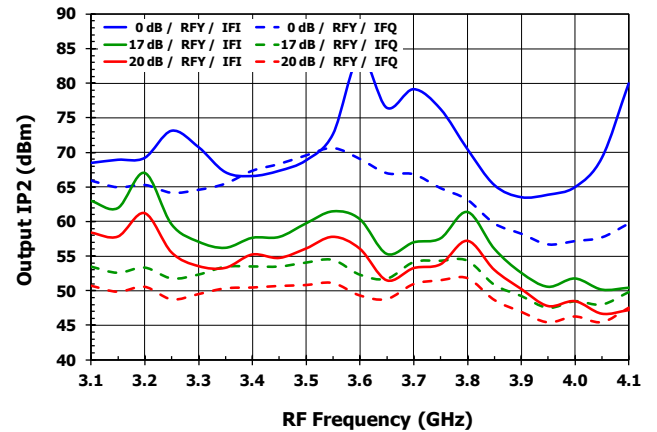
OIP2 vs. Attenuation Setting [Low Side LO, RF<sub>V</sub>]



OIP2 vs. Attenuation Setting [High Side LO, RF<sub>X</sub>]



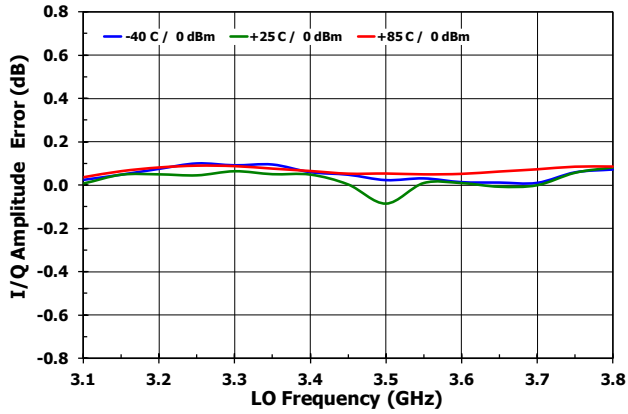
OIP2 vs. Attenuation Setting [High Side LO, RF<sub>V</sub>]



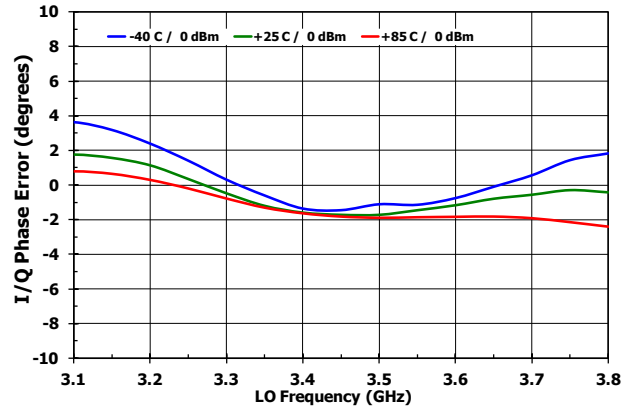


## TYPICAL OPERATING CONDITIONS (- 15 -)

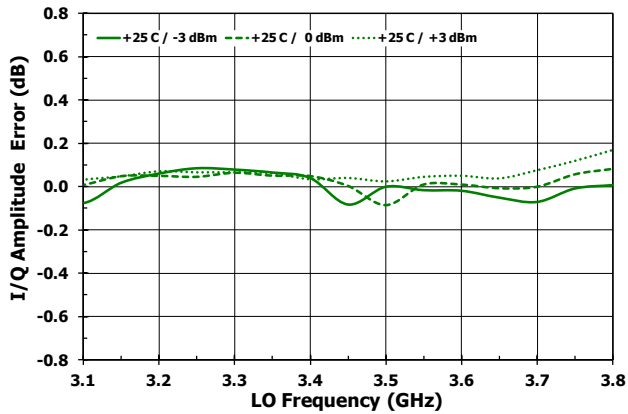
Amplitude Imbalance vs  $T_{\text{Ambient}}$  [ $P_{\text{LO}} = 0 \text{ dBm}$ ]



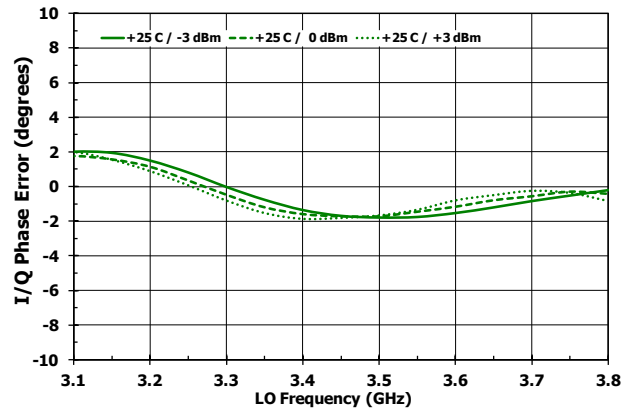
Phase Imbalance vs  $T_{\text{Ambient}}$  [ $P_{\text{LO}} = 0 \text{ dBm}$ ]



Amplitude Imbalance vs LO Power [ $T_{\text{Ambient}}$ ]

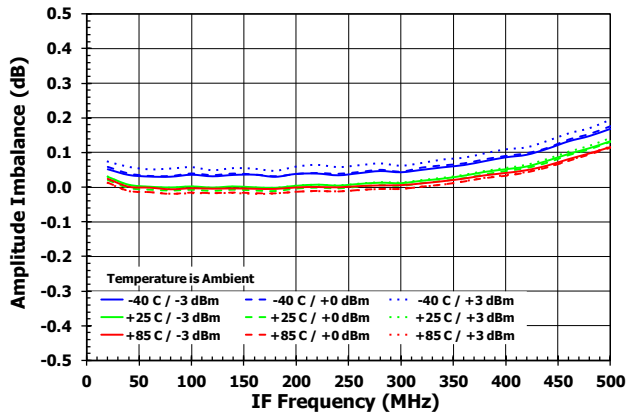


Phase Imbalance vs LO Power [ $T_{\text{Ambient}}$ ]

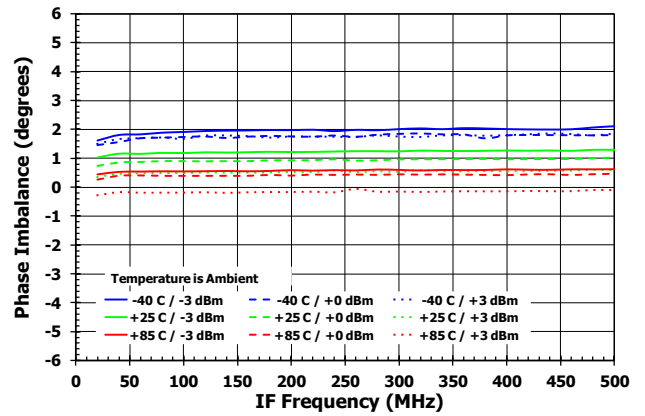


## TYPICAL OPERATING CONDITIONS (- 16 -)

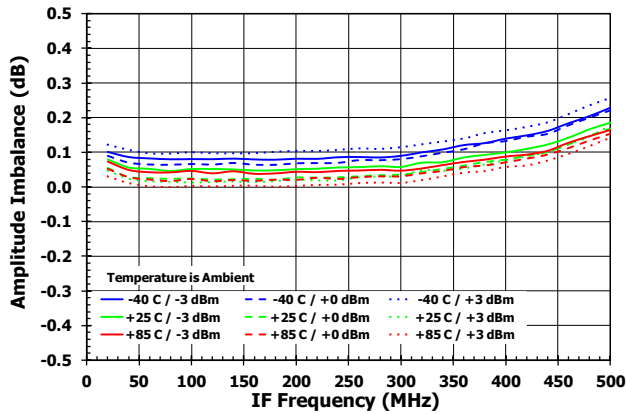
Amplitude Imbalance [ $F_{LO} = 3.155 \text{ GHz}$ ]



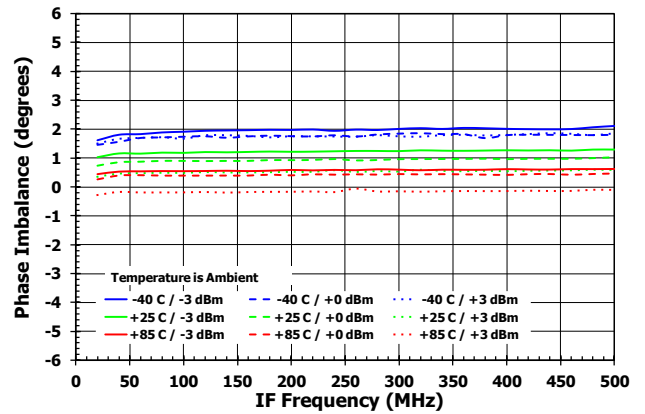
Phase Imbalance [ $F_{LO} = 3.155 \text{ GHz}$ ]



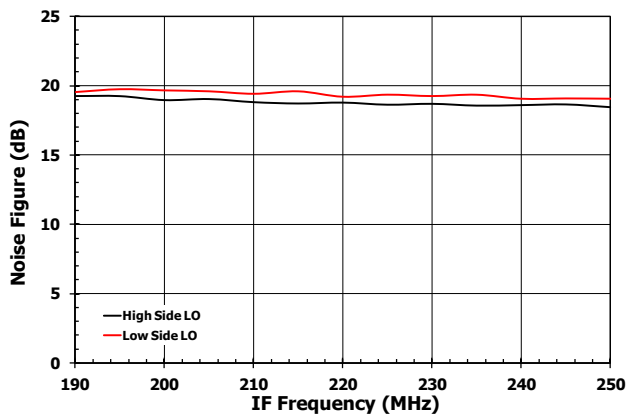
Amplitude Imbalance [ $F_{LO} = 3.255 \text{ GHz}$ ]



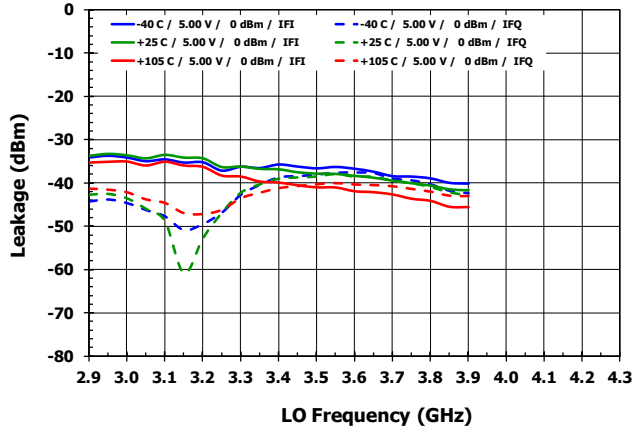
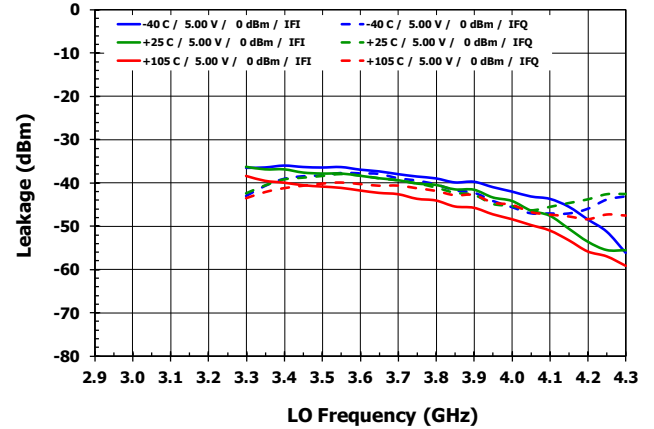
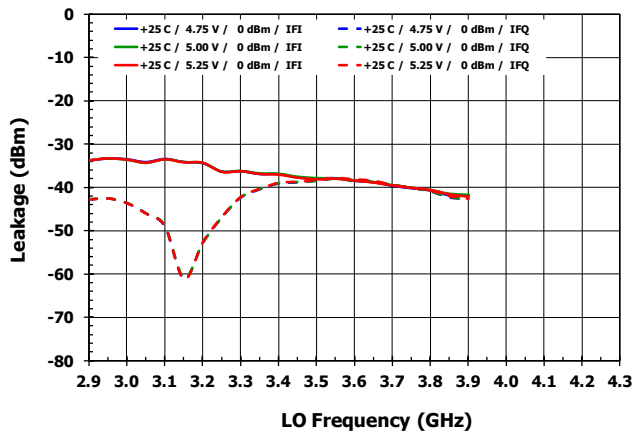
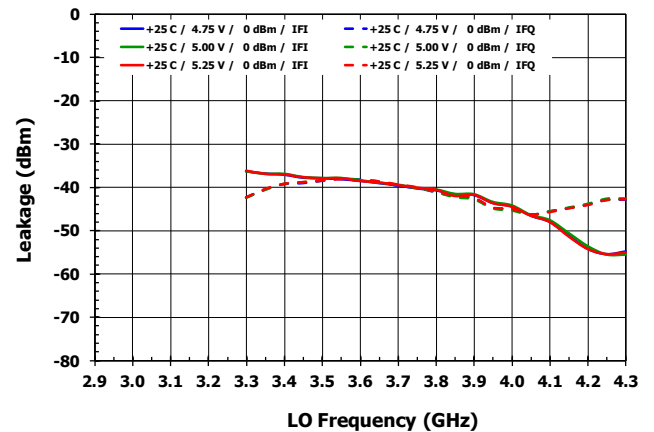
Phase Imbalance [ $F_{LO} = 3.255 \text{ GHz}$ ]



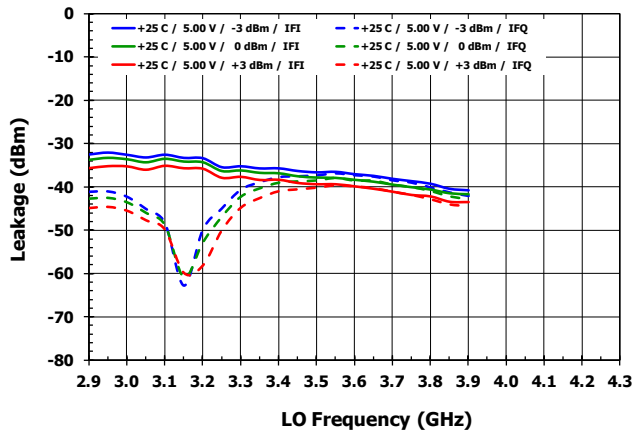
Noise Figure [ $F_{LO}=3.48 \text{ GHz}$ ]



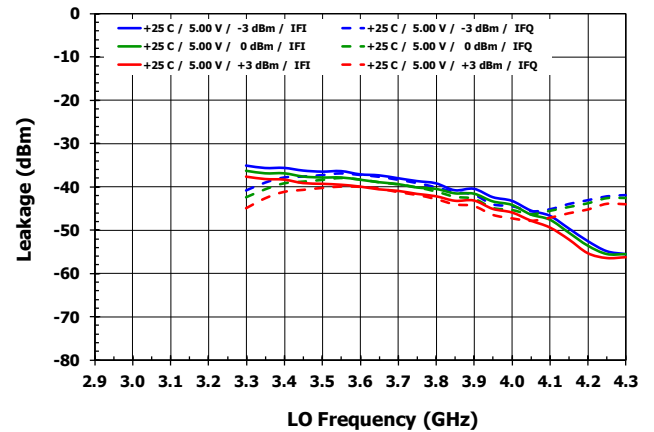
## TYPICAL OPERATING CONDITIONS (- 17 -)

LO to IF Leakage vs.  $T_{case}$  [Low Side LO]LO to IF Leakage vs.  $T_{case}$  [High Side LO]LO to IF Leakage vs.  $V_{cc}$  [Low Side LO]LO to IF Leakage vs.  $V_{cc}$  [High Side LO]

LO to IF Leakage vs. LO Power [Low Side LO]

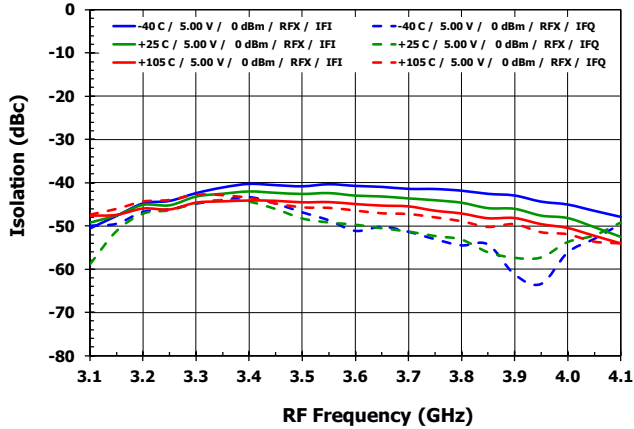


LO to IF Leakage vs. LO Power [High Side LO]

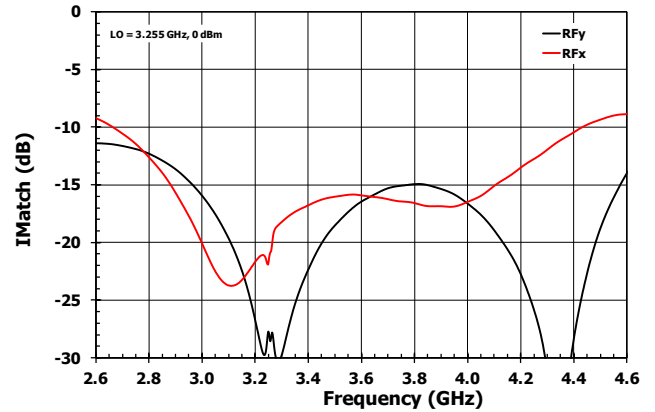


## TYPICAL OPERATING CONDITIONS (- 18 -)

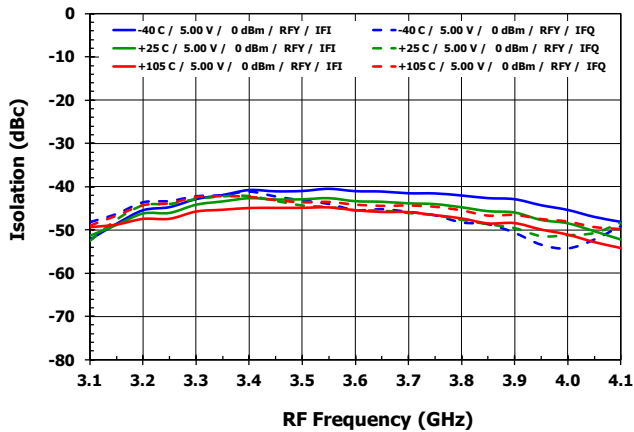
RF<sub>x</sub> to IF Isolation



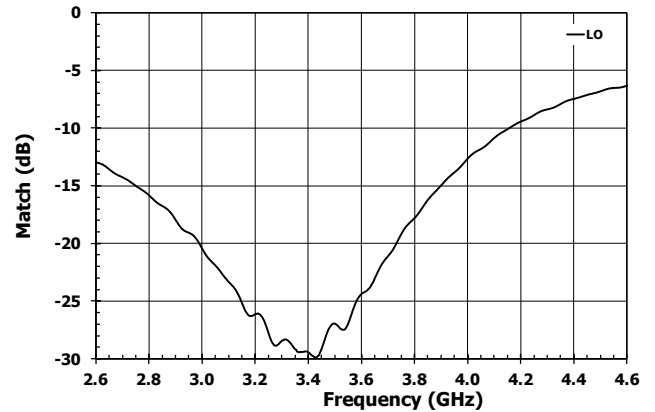
RF Match



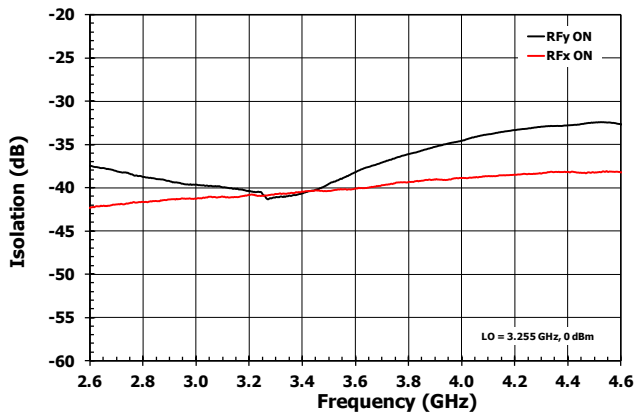
RF<sub>y</sub> to IF Isolation



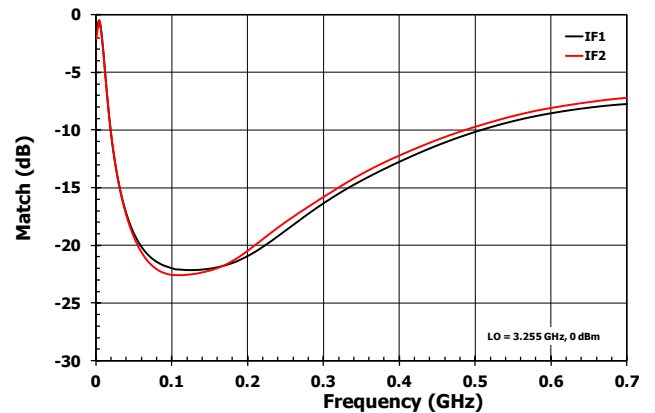
LO Match



RF Switch Isolation



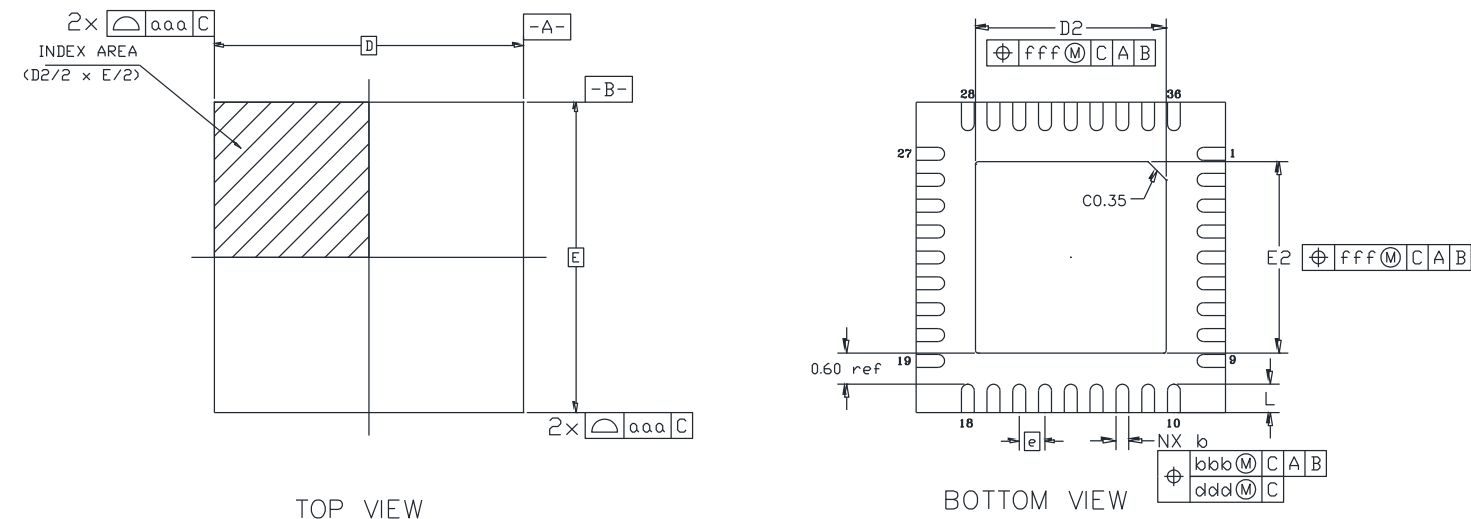
IF Match



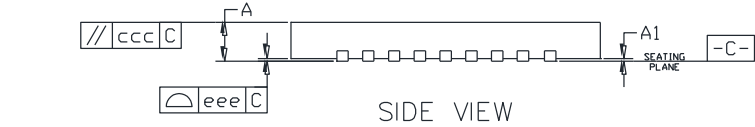
PACKAGE DRAWING

(6mm x 6mm 36-pin TQFN), NBG36 EPad option P1

All dimensions are in mm.



| SYMBOL | DIMENSION |      |      |
|--------|-----------|------|------|
|        | MIN       | NOM  | MAX  |
| L      | 0.45      | 0.55 | 0.65 |
| D      | 6.00 BSC  |      |      |
| E      | 6.00 BSC  |      |      |
| e      | 0.50 BSC  |      |      |
| A      | 0.70      | 0.75 | 0.80 |
| A1     | 0.00      | 0.02 | 0.05 |
| b      | .20       | .25  | .30  |
| aaa    | 0.15      |      |      |
| bbb    | 0.10      |      |      |
| ccc    | 0.10      |      |      |
| ddd    | 0.05      |      |      |
| eee    | 0.08      |      |      |
| fff    | 0.10      |      |      |



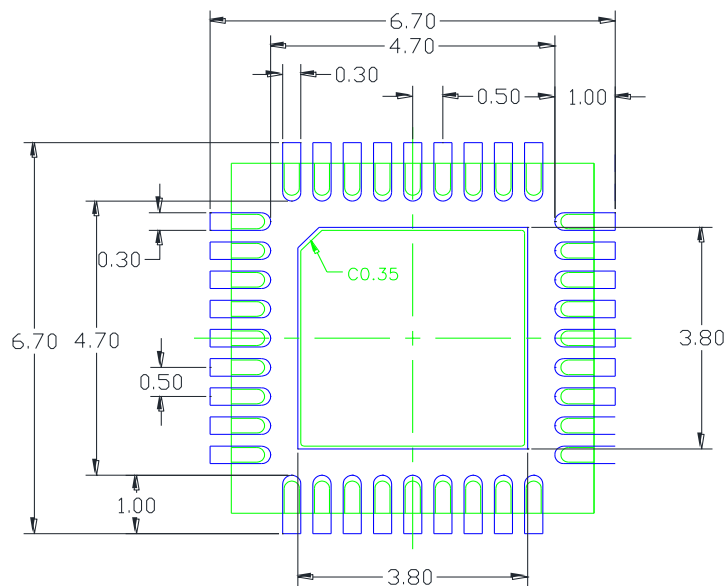
EPAD OPTION

| SYMBOL | P1   |      |      | P2   |      |      |
|--------|------|------|------|------|------|------|
|        | MIN  | NOM  | MAX  | MIN  | NOM  | MAX  |
| E2     | 3.60 | 3.70 | 3.80 | 4.00 | 4.10 | 4.20 |
| D2     | 3.60 | 3.70 | 3.80 | 4.00 | 4.10 | 4.20 |

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

## LAND PATTERN DIMENSION

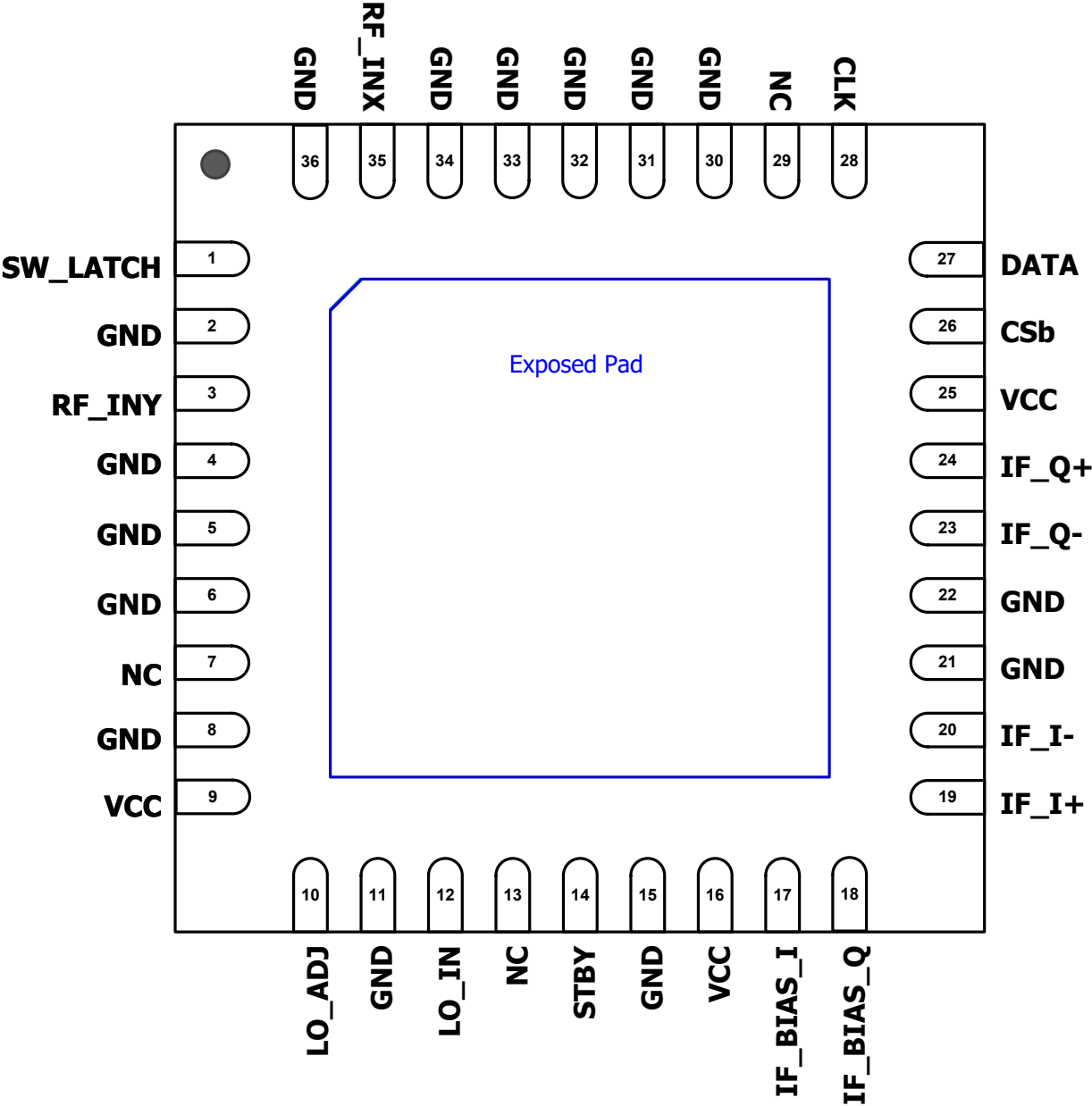


RECOMMENDED LAND PATTERN DIMENSION

### NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

PIN DIAGRAM

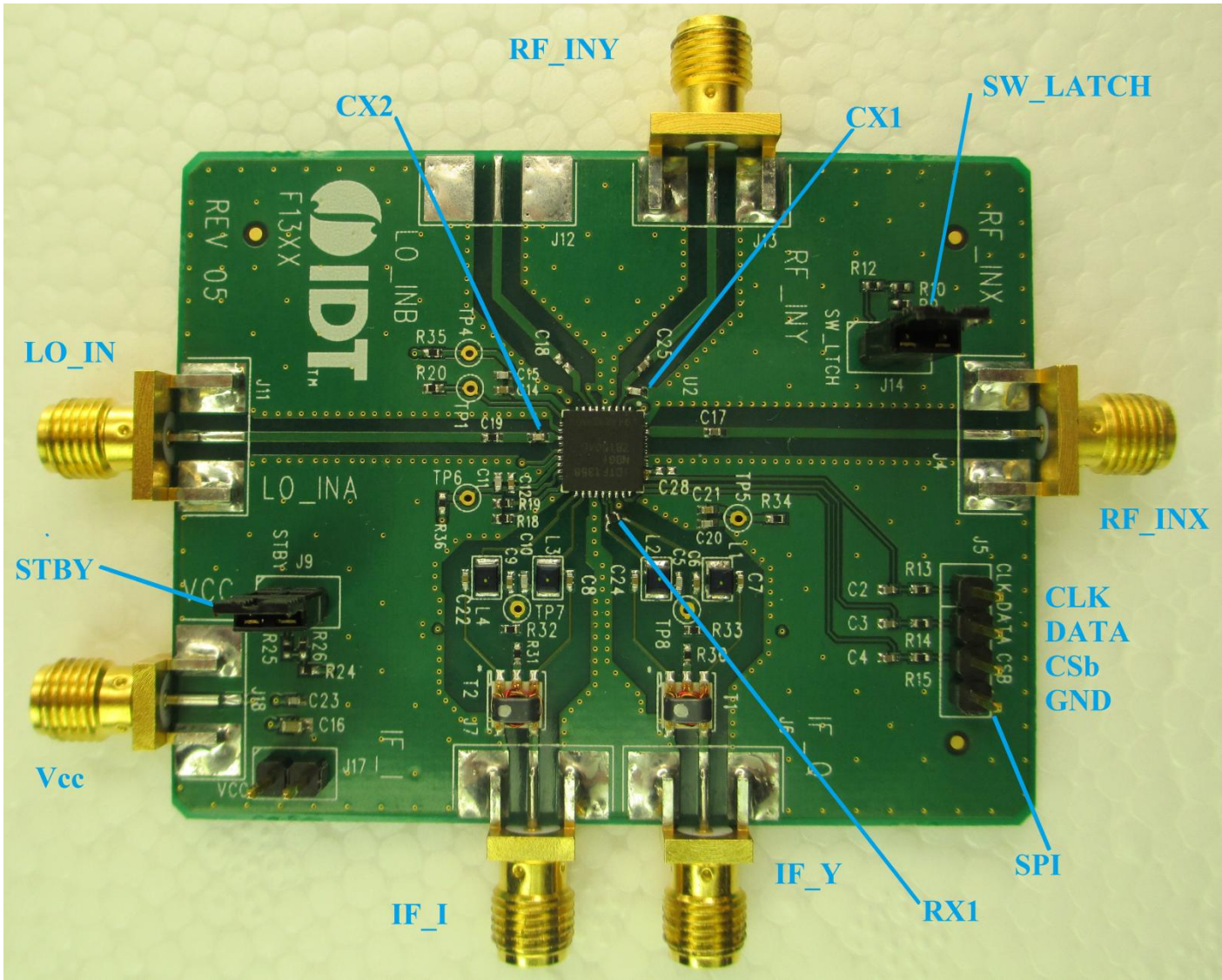


**PIN DESCRIPTION**

| Pin                                                         | Name                   | Function                                                                                                                                                                                                                                                               |
|-------------------------------------------------------------|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                                                           | SW_LATCH               | Stand-by latch. Pull Low or Ground for Normal Operation. If left floating, this input will be internally pulled high, disabling SPI writes to ENb (Standby) and RF SW bits (A0, A2).                                                                                   |
| 2, 4, 5, 6, 8, 11, 15,<br>21, 22, 30, 31, 32, 33,<br>34, 36 | GND                    | Ground these Pins.                                                                                                                                                                                                                                                     |
| 3                                                           | RF_INY                 | Alternate RF Input. Separated from RF_INX by internal SP2T. AC couple to this pin. This is a reflective switch and is not internally matched to 50 ohms.                                                                                                               |
| 9, 16, 25                                                   | VCC                    | Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.                                                                                                                                                      |
| 10                                                          | LO_ADJ                 | Connect the specified resistor from this pin to ground to set the LO path I <sub>cc</sub> . This IS a current setting resistor                                                                                                                                         |
| 12                                                          | LO_IN                  | LO Input. AC couple to this pin. Internally matched to 50 ohms                                                                                                                                                                                                         |
| 7, 13, 29                                                   | NC                     | No Connection. Not internally connected. OK to connect to V <sub>cc</sub> . Recommended Connection is Ground                                                                                                                                                           |
| 14                                                          | STBY                   | STBY Mode. Pull this pin high for Standby mode (30mA). Pull low or Ground for normal Operation                                                                                                                                                                         |
| 17,<br>18                                                   | IF_BIAS_I<br>IF_BIAS_Q | Connect the specified resistor from this pin to ground to set the IF amplifier bias reference. This is NOT a current setting resistor.                                                                                                                                 |
| 19,<br>20                                                   | IF_I+<br>IF_I-         | <i>In-Phase</i> Mixer Differential IF Output. Connect pull-up inductors from each of these pins to V <sub>cc</sub> (see the Typical Application Circuit).                                                                                                              |
| 23,<br>24                                                   | IF_Q-<br>IF_Q+         | <i>Quadrature</i> Mixer Differential IF Output. Connect pull-up inductors from each of these pins to V <sub>cc</sub> (see the Typical Application Circuit).                                                                                                            |
| 26                                                          | CSb                    | Chip Select Bar. The falling edge initiates a programming cycle and the rising edge latches the programmed shift register data into the active register.                                                                                                               |
| 27                                                          | DATA                   | Serial Data Input                                                                                                                                                                                                                                                      |
| 28                                                          | CLK                    | Serial Clock Input                                                                                                                                                                                                                                                     |
| 35                                                          | RF_INX                 | Main RF Input. Separated from RF_INY by internal SP2T. AC couple to this pin. This is a reflective switch and is not internally matched to 50 ohms.                                                                                                                    |
|                                                             | — EP                   | Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the noted RF performance. |

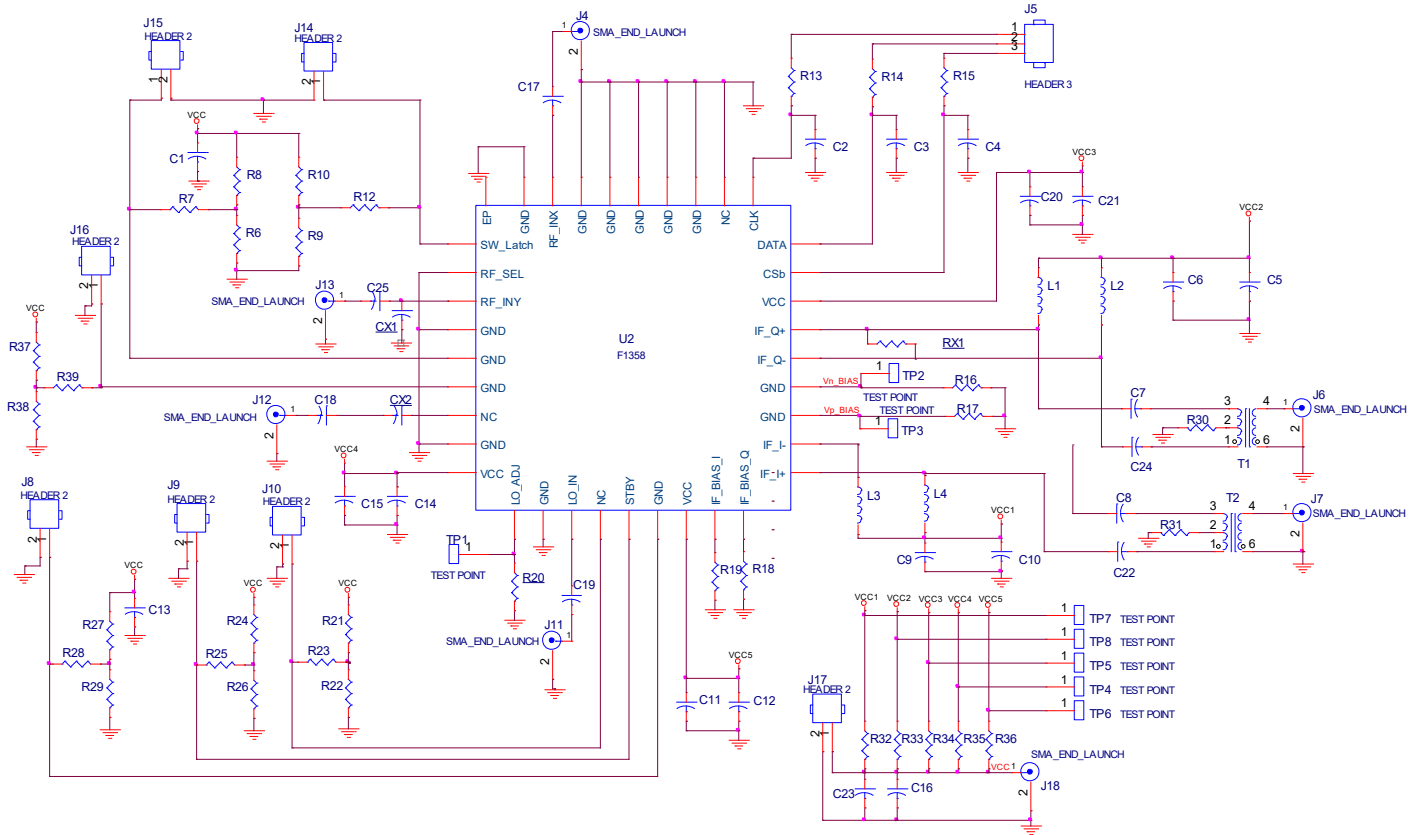


EVKIT PICTURE



Note: Our standard evaluation board is modified with components RX1, CX1, and CX2

## EVKIT / APPLICATIONS CIRCUIT



**EVKIT BOM**

| Item # | Part Reference                                | QTY | DESCRIPTION                                      | Mfr. Part #    | Mfr.            |
|--------|-----------------------------------------------|-----|--------------------------------------------------|----------------|-----------------|
| 1      | C2, C3, C4                                    | 3   | 100pF ±5%, 50V, C0G Ceramic Capacitor (0402)     | GRM1555C1H101J | MURATA          |
| 2      | C6, C7, C8, C9,<br>C12, C14, C21,<br>C22, C24 | 9   | 10nF ±5%, 50V, X7R Ceramic Capacitor (0402)      | GRM155R71H103J | MURATA          |
| 3      | C5, C10, C11,<br>C15, C20, C23                | 6   | 1000pF ±5%, 50V, C0G Ceramic Capacitor (0402)    | GRM1555C1H102J | MURATA          |
| 4      | C17, C25                                      | 2   | 39pF ±5%, 50V, C0G Ceramic Capacitor (0402)      | GRM1555C1H390J | MURATA          |
| 5      | C16                                           | 1   | 10uF ±20%, 6.3V, X5R Ceramic Capacitor (0603)    | GRM188R60J106M | MURATA          |
| 6      | CX1                                           | 1   | 0.4pF ±0.05pF, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1HR40W | MURATA          |
| 7      | CX2                                           | 1   | 0.8pF ±0.05pF, 50V, C0G Ceramic Capacitor (0402) | GJM1555C1HR80W | MURATA          |
| 8      | R30, R31, R32,<br>R33, R34, R35,<br>C19       | 7   | 0Ω Resistors (0402)                              | ERJ-2GE0R00X   | Panasonic       |
| 9      | R36                                           | 1   | 20Ω ±1%, 1/10W, Resistor (0402)                  | ERJ-2RKF20R0X  | Panasonic       |
| 10     | R13, R14, R15                                 | 3   | 100Ω ±1%, 1/10W, Resistor (0402)                 | ERJ-2RKF1000X  | Panasonic       |
| 11     | R18, R19                                      | 2   | 226Ω ±1%, 1/10W, Resistor (0402)                 | ERJ-2RKF2260X  | Panasonic       |
| 12     | R20                                           | 1   | 4.3kΩ ±1%, 1/10W, Resistor (0402)                | ERJ-2RKF4301X  | Panasonic       |
| 13     | R10, R24                                      | 2   | 43kΩ ±1%, 1/10W, Resistor (0402)                 | ERJ-2RKF4302X  | Panasonic       |
| 14     | R12, R25                                      | 2   | 47kΩ ±1%, 1/10W, Resistor (0402)                 | ERJ-2RKF4702X  | Panasonic       |
| 15     | R9, R26                                       | 2   | 75kΩ ±1%, 1/10W, Resistor (0402)                 | ERJ-2RKF7502X  | Panasonic       |
| 16     | RX1                                           | 1   | 7.5kΩ ±1%, 1/10W, Resistor (0402)                | ERJ-2RKF7501X  | Panasonic       |
| 17     | J9, J14, J17                                  | 3   | CONN HEADER VERT SGL 2 X 1 POS GOLD              | 961102-6404-AR | 3M              |
| 18     | J5                                            | 1   | CONN HEADER VERT SGL 4 X 1 POS GOLD              | 961104-6404-AR | 3M              |
| 19     | J6, J7, J18                                   | 3   | Edge Launch SMA (0.250 inch pitch ground, round) | 142-0711-821   | Emerson Johnson |
| 20     | J4, J11, J13                                  | 3   | Edge Launch SMA (0.375 inch pitch ground, tab)   | 142-0701-851   | Emerson Johnson |
| 21     | L1, L2, L3, L4                                | 4   | 1uH ±5%, .500A, Ferrite Chip Inductor (0805)     | 0805LS-102XJLB | COILCRAFT       |
| 22     | T1, T2                                        | 2   | 1.5-600Mhz 50Ω, RF Transformer (4:1)             | TC4-6TG2+      | Mini Circuits   |
| 23     | U1                                            | 1   | DPD Demodulator                                  | F1358          | AXIRO           |
| 24     |                                               | 1   | Printed Circuit Board                            | F13XX REV 05   | AXIRO           |
| 25     |                                               | 1   | Bill Of Material (Rev 02)                        |                | AXIRO           |

## TOP MARKINGS

| Top Marking Illustration                                                          | Marking      | Representation                                                      |
|-----------------------------------------------------------------------------------|--------------|---------------------------------------------------------------------|
|  | IDTF1358NBGI | Manufacturer Part Number                                            |
|                                                                                   | ##           | Die Version                                                         |
|                                                                                   | YYWW         | Date code, two digits for the year and two digits for the work week |
|                                                                                   | \$           | Assembly Site                                                       |
|                                                                                   | *****        | Assembly Lot Number                                                 |

## APPLICATIONS INFORMATION

F1358 has been optimized for use in high performance RF applications from 3200 MHz to 4000 MHz.

### Matching Components

For proper optimization three components were added and one was removed from our standard evaluation board.

| Component | Value          | Component                                                                                                                                             |
|-----------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| RX1       | 7.5 k $\Omega$ |                                                                                                                                                       |
| CX1       | 0.4 pF         | This shunt capacitor is used to create an better match on the second RF input line.                                                                   |
| CX2       | 0.8 pF         | This series capacitor must be as close to the package as possible for the best possible match on the LO port.                                         |
| C18       | 0 $\Omega$     | For better return loss the capacitor was moved closer to the package (CX2). This position was filled with a 0 ohm resistor to span the component gap. |

### Power Supplies

All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V over 20  $\mu$ S ( $< 0.05$  V/  $\mu$ S). In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

**F1358 Digital Pin Voltage & Resistance Values (pins not connected)**

The following table lists the resistance between various pins and ground when no DC power is applied. When the device is powered up with +5 Volts DC these same pins should have the measured voltage to ground.

| Pin | Name     | DC voltage (volts) | Resistance (ohms) |
|-----|----------|--------------------|-------------------|
| 1   | SW_LATCH | 1.75               | 1.6M              |
| 14  | STBY     | 5.0                | 50k               |
| 26  | CSb      | 1.75               | 1.6M              |
| 27  | DATA     | 1.75               | 1.6M              |
| 28  | CLK      | 1.75               | 1.6M              |

**I/Q Phase Error**

The standard configuration results in less than 4 degrees of I/Q Phase error with LO frequencies from 3100 to 3800 MHz. The I/Q phase error can be further improved for a given LO frequency via applications changes.

**Revision History**

| Revision | Date        | Description                                                                                                                 |
|----------|-------------|-----------------------------------------------------------------------------------------------------------------------------|
| 2.00     | Aug 3, 2026 | Updated document branding and layout to Axiro Semiconductor standard. No changes to device functionality or specifications. |