F1427

2.3 to 4.2GHz 100Ω DIFF-In 50Ω SE-Out Driver Amplifier

The F1427 is a high gain RF amplifier designed to operate within the 2.3GHz to 4.2GHz frequency range. Using a single 5V power supply, the F1427 provides 35.5dB of gain and 28dBm OP1dB at 2.6GHz.

The F1427 is packaged in a 3 × 3 mm, 16-VFQFPN package, with a differential 100Ω input and single-ended 50Ω output impedances for ease of integration into the signal path.

Competitive Advantage

- Excellent gain flatness
- High linearity
- Flexible bias adjustment through external resistors to accommodate different applications

Applications

- 5G sub-6GHz massive MIMO
- Wireless infrastructure base stations
- FDD or TDD systems
- Point-to-point infrastructure
- Public safety infrastructure
- Military handhelds
- Repeaters and DAS
- General purpose RF

Features

- Frequency range: 2.3GHz to 4.2GHz
- 35.5dB typical gain at 2.6GHz
- 0.6dB max gain flatness across 100MHz BW
- 28dBm typical OP1dB at 2.6GHz
- 100Ω differential input and 50Ω singled-ended output impedances
- 5V power supply
- 1.8V logic compatible Standby Mode for power savings
- Operating temperature (T_{EPAD}) range: -40°C to +115°C
- 3 × 3 mm 16-VFQFPN package

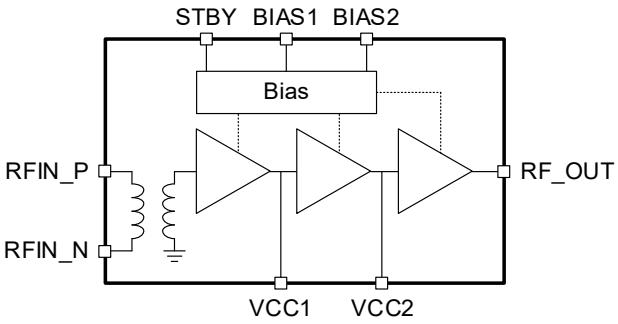

Figure 1. Block Diagram

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1. Pin Information

1.1 Pin Assignments

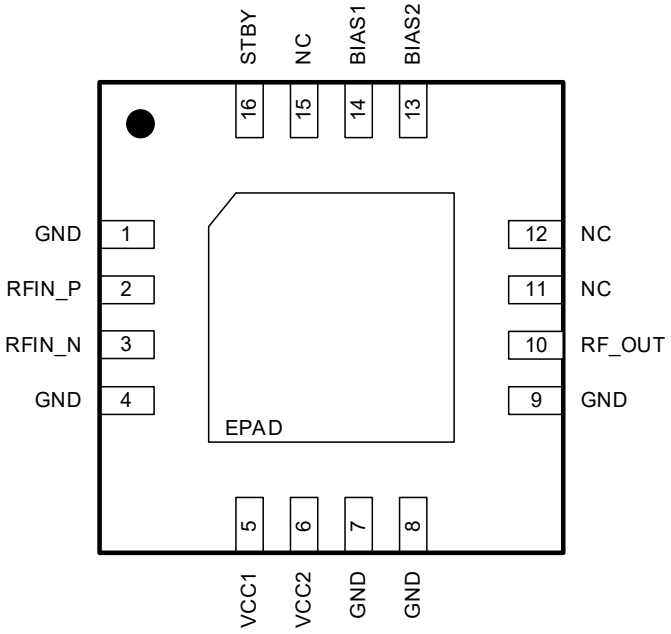


Figure 2. Pin Assignments – Top View

1.2 Pin Descriptions

Number	Name	Description
1, 4, 7, 8, 9	GND	Internally grounded. This pin must be grounded with a via as close to the pin as possible.
2	RFIN_P	RF input. Must use an external DC block.
3	RFIN_N	RF input. Must use an external DC block.
5	VCC1	Power supply. Pull up to VCC through inductor and use bypass capacitors as close to the pin as possible. In addition to supplying the device with a DC voltage, there is also an RF signal present.
6	VCC2	Power supply. Pull up to VCC through inductor and use bypass capacitors as close to the pin as possible. In addition to supplying the device with a DC voltage, there is also an RF signal present.
10	RF_OUT	RF output. Pull up to VCC through inductor. Must use an external DC block.
13	BIAS_2	Connect using a resistor to a common VCC and use a bypass capacitor. Place network as close to the pin as possible.
14	BIAS_1	Connect using a resistor to a common VCC and use a bypass capacitor. Place network as close to the pin as possible.
11, 12, 15	NC	No internal connection. These pins can be left unconnected or connected to ground (recommended). If grounded, use a via as close to the pin as possible. Note: Either pin 11 or pin 12 must be connected to ground to provide good isolation between pin 10 (RF_OUT) and pin 13 (BIAS_2).
16	STBY	Standby pin. With Logic LOW applied to this pin, the amplifier is powered off. With Logic HIGH applied to this pin (or if the pin is left unconnected), the part is in full operation mode. Pin is 1.8V logic compatible.

Number	Name	Description
	EPAD	Exposed Pad. Internally connected to ground. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the noted RF performance.

2. Specifications

2.1 Absolute Maximum Ratings

Stresses above those listed below can cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Parameter	Symbol	Minimum	Maximum	Unit
VCC to GND	V_{CC}	-0.3	+6.0	V
STBY	V_{CTL}	-0.3	Lower of (5.0, VCC + 0.25)	V
BIAS_1 to GND	V_{BIAS_1}		+6.0	V
BIAS_2 to GND	V_{BIAS_2}		+6.0	V
RFIN externally applied DC voltage	V_{RFIN}	-0.5	+0.5	V
RFOUT externally applied DC voltage	V_{RFOUT}	-0.5	+6.0	V
Maximum CW Input Power applied for 24 hours. VCC = 5V, T_{EPAD} = 115°C, input/output based on a 50Ω system. Standby = logic HIGH: ON state. [1]	$P_{MAX\_IN\_ON}$		4	dBm
Maximum CW Input Power applied for 24 hours. VCC = 5V, T_{EPAD} = 115°C, input/output based on a 50Ω system. Standby = logic LOW: OFF state. [1]	$P_{MAX\_IN\_OFF}$		10	dBm
Junction Temperature	T_{JMAX}		150	°C
Storage Temperature Range	T_{st}	-65	150	°C
Lead Temperature (soldering, 10s)			260	°C

1. Exposure to these maximum RF levels can result in significantly higher I_{CC} current draw because of overdriving the amplifier stages.

2.2 ESD Ratings

Parameter	Symbol	Rating	Unit
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}	1500	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)	V_{ESDCDM}	750	V

2.3 Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power Supply Voltage	V_{CC}		4.75	5	5.25	V
Operating Temperature Range	T_{EPAD}	Exposed paddle	-40		+115	°C
RF Frequency Range [1]	f_{RF}	2.6GHz Tuning Set	2.3		2.7	GHz
		3.6GHz Tuning Set	3.3		3.8	
		4.0GHz Tuning Set	3.8		4.2	
RFIN Port Impedance	Z_{RFI}	Differential		100		Ω
RFOUT Port Impedance	Z_{RFO}	Single-ended		50		Ω

1. Recommended frequency ranges for Evaluation Kit Bill of Materials (BOMs) defined in section 5.3.

2.4 Electrical Specifications

2.4.1. General

See Evaluation Board Schematic. Specifications apply when operated as a TX amplifier with tuning optimized for desired band of interest, V_{CC} = +5.0V, T_{EPAD} = +25°C, STBY = HIGH, Z_S = 100Ω differential, Z_L = 50Ω single-ended, Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Logic Input High	V_{IH}		***1.17*** [1]		V_{CC}	V
Logic Input Low	V_{IL}		-0.3		***0.63***	V
Logic Current	I_{IH}, I_{IL}	STBY pin. V_{STBY} = 1.8 V	***-250***		***+250***	µA
Quiescent Current [2]	I_{CC}	2.6GHz Tuning Set, R1 = 24Ω		147	***177***	mA
		3.6GHz Tuning Set, R1 = 51Ω		136		
Standby Current	I_{CC_STBY}	STBY = LOW		43		mA
Standby Settling Time [3]	t_{SETTLE_ON}	50% STBY control to RF output within 0.25dB and 1° of the on-state final value. V_{CC} = +5V, T_{EPAD} = -40°C to 115°C			1	µs
	t_{SETTLE_OFF}	50% STBY control to gain less than 5% of the on-state final gain value. V_{CC} = +5V, T_{EPAD} = -40°C to 115°C			1	

1. Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.
2. I_{CC} refers to the nominal small signal bias current.
3. Standby control signal has a rise/fall time of typically 5 to 10 ns and logic level of 0V to 1.8V.

2.4.2. 2.3GHz to 2.7GHz

See Evaluation Board Schematic and Evaluation Kit Bill of Material (BOM) – 2.3GHz to 2.7GHz. Typical specifications apply when operated as a TX amplifier with tuning optimized for the 2.3GHz to 2.7GHz band, V_{CC} = +5.0V, f_{RF} = 2.6GHz, T_{EPAD} = +25°C, Z_S = 100Ω differential, Z_L = 50Ω single-ended. Minimum and Maximum specifications apply across process and the recommended operating frequency, voltage, and full performance temperature ranges unless otherwise stated.

Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	f_{RF} = 2.6GHz T_{EPAD} = 25°C	33.5	35.5		dB
			31		39	
Gain Variation Over Temperature	G_{TEMP}	f_{RF} = 2.6GHz V_{CC} = 5V			-2.5/+2.0	dB
Gain Flatness	G_{FLAT}	Any 100MHz BW within f_{RF} = 2.3GHz to 2.7GHz			0.6	dB
STBY Mode Gain	G_{STBY}	STBY = logic LOW, $P_{IN} \leq$ -15dBm		-35		dB
Reverse Isolation	ISO_{REV}			53		dB
RF Input Return Loss	RL_{RFIN}	f_{RF} = 2.3GHz to 2.7GHz		19		dB
RF Output Return Loss	RL_{RFOUT}	f_{RF} = 2.3GHz to 2.7GHz		9		dB
Noise Figure	NF	T_{EPAD} = -40°C			3.9	dB
		T_{EPAD} = +115°C			6.1	
Output Third Order Intercept Point [1]	OIP3	P_{OUT} = 0dBm/tone, Δf = 1MHz		37		dBm
Output 1dB Compression Point	OP1dB		25.5	28		dBm
ACLR	ACLR	20MHz LTE Pout = 15dBm + 8.5dB PAR, 0.01% Probability		-42.5		dBc
		20MHz LTE Pout = 12dBm + 8.5dB PAR, 0.01% Probability		-49		
CMRR	CMRR		21			dB

1. OIP3 performance for input powers up to P1dB to 10dB and Δf = 100MHz.

2.4.3. 3.3GHz to 3.8GHz

See Evaluation Board Schematic and Evaluation Kit Bill of Material (BOM) – 3.3GHz to 3.8GHz. Typical specifications apply when operated as a TX amplifier with tuning optimized for the 3.3GHz to 3.8GHz band, V_{CC} = +5.0V, f_{RF} = 3.6GHz, T_{EPAD} = +25°C, Z_S = 100Ω differential, Z_L = 50Ω single-ended. Minimum and Maximum specifications apply across process and the recommended operating frequency, voltage, and full performance temperature ranges unless otherwise stated.

Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	f_{RF} = 3.6GHz T_{EPAD} = 25°C		35		dB
			30.5		38.5	
Gain Variation Over Temperature	G_{TEMP}	f_{RF} = 3.6GHz V_{CC} = 5V			-2.5/+2.0	dB
Gain Flatness	G_{FLAT}	Any 100MHz BW within f_{RF} = 3.3GHz to 3.8GHz			0.5	dB
STBY Mode Gain	G_{STBY}	STBY = logic LOW, $P_{IN} \leq$ -15dBm		-33		dB
Reverse Isolation	ISO_{REV}			54		dB
RF Input Return Loss	RL_{RFIN}	f_{RF} = 3.3GHz to 3.8GHz		17		dB
RF Output Return Loss	RL_{RFOUT}	f_{RF} = 3.3GHz to 3.8GHz		10		dB
Noise Figure	NF	T_{EPAD} = -40°C			3.6	dB
		T_{EPAD} = +115°C			5.9	
Output Third Order Intercept Point [1]	OIP3	P_{OUT} = 0dBm/tone, Δf = 1MHz		32		dBm
Output 1dB Compression Point	OP1dB		25.5	28		dBm
ACLR	ACLR	20MHz LTE Pout = 15dBm + 8.5dB PAR, 0.01% Probability		-42		dBc
		20MHz LTE Pout = 12dBm + 8.5dB PAR, 0.01% Probability		-47		
CMRR	CMRR		21			dB

1. OIP3 performance for input powers up to P1dB to 10dB and Δf = 100MHz.

2.5 Thermal Characteristics

Parameter	Symbol	Value	Unit
Junction to Ambient Thermal Resistance	θ_{JA}	63.5	°C/W
Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	θ_{JC_BOT}	5.9	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL1	

3. Typical Operating Conditions

Unless otherwise stated the typical operating graphs were measured under the following conditions:

- V_{CC} = 5.0V
- STBY = HIGH
- T_{EPAD} = +25°C
- f_{RF} = 2.6GHz
- f_{RF} = 3.6GHz
- Z_S = 100Ω differential, Z_L = 50Ω single-ended
- Pout = 0dBm/tone and 1MHz tone spacing for OIP3

3.1 Typical Performance Graphs

3.1.1. 2.3GHz to 2.7GHz

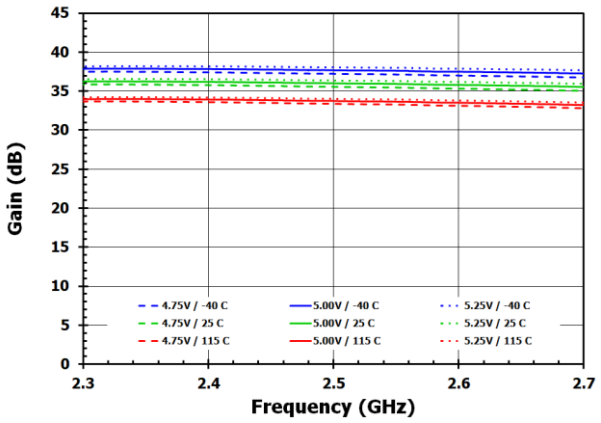


Figure 3. Gain

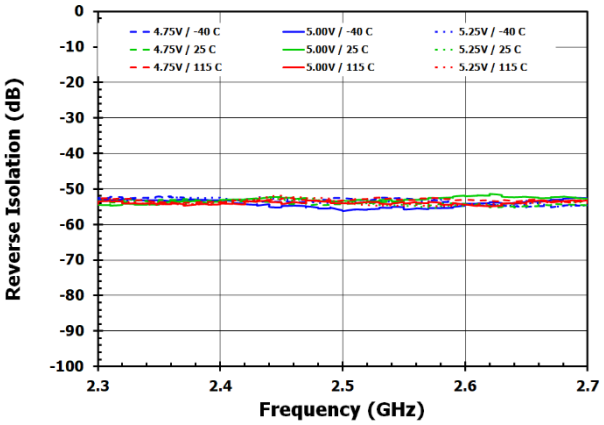


Figure 4. Reverse Isolation

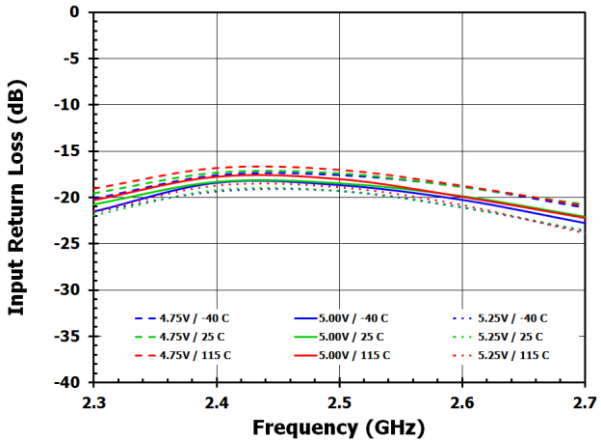


Figure 5. Input Return Loss

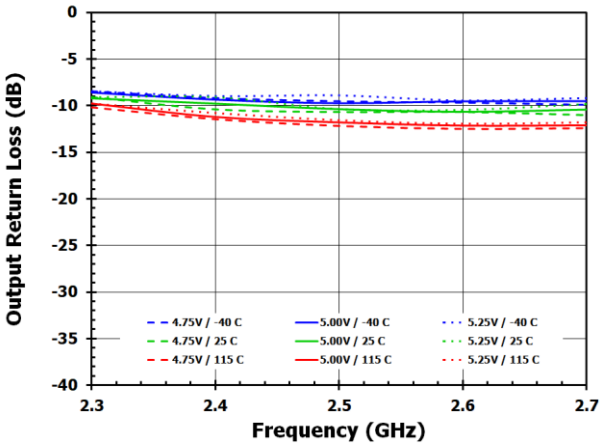


Figure 6. Output Return Loss

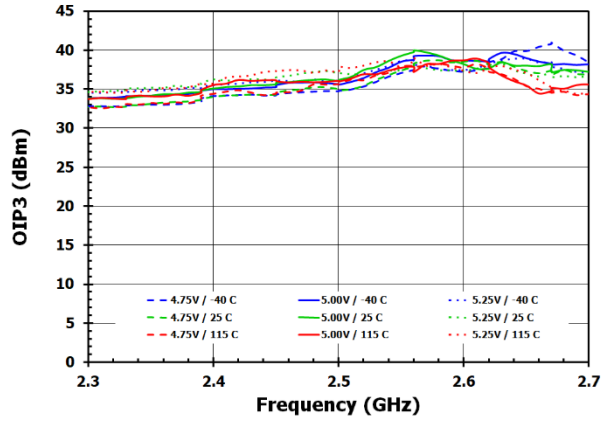


Figure 7. OIP3

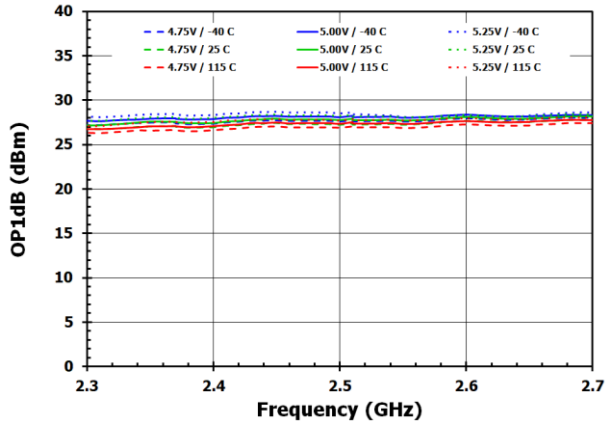


Figure 8. OP1dB

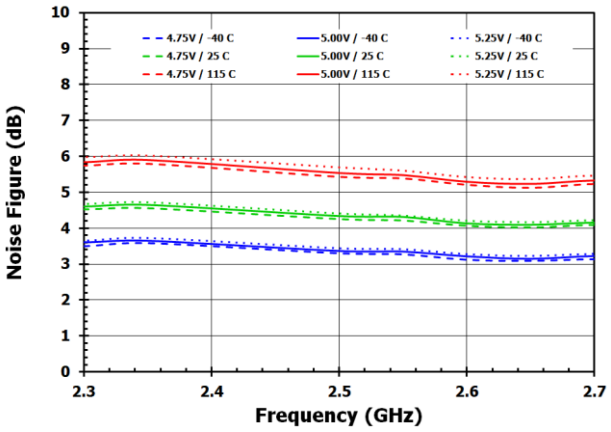


Figure 9. Noise Figure

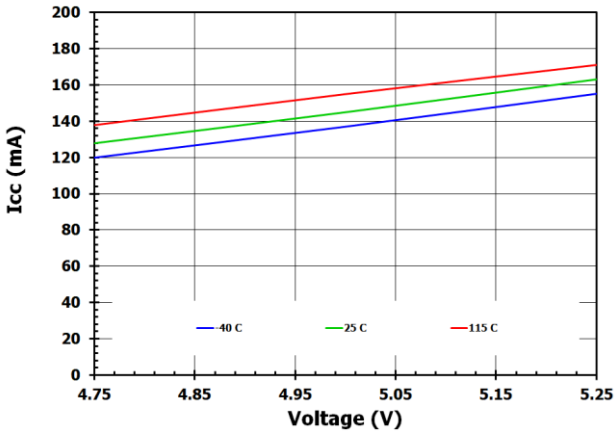


Figure 10. Quiescent Current

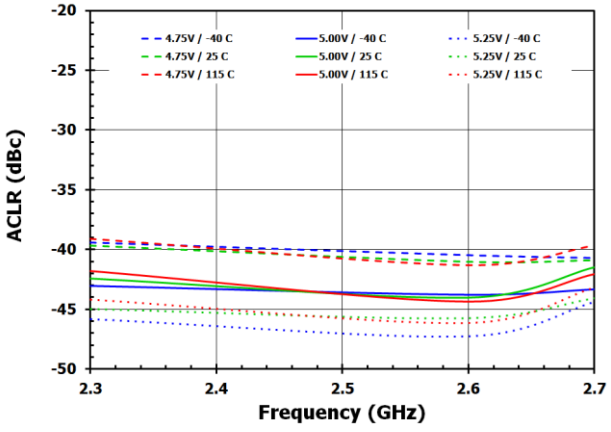


Figure 11. ACLR, 20MHz LTE
Pout = 15dBm + 8.5dB PAR, 0.01% Probability

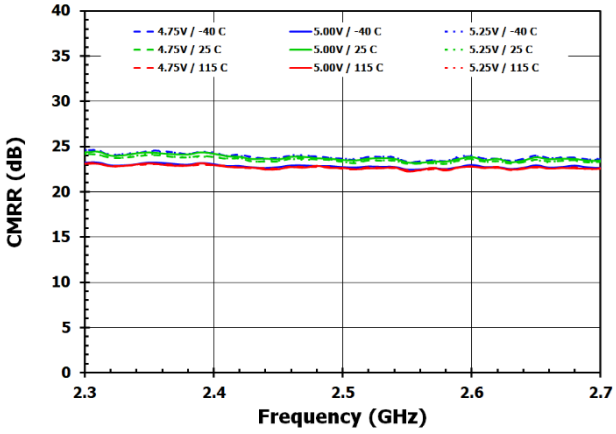


Figure 12. CMRR

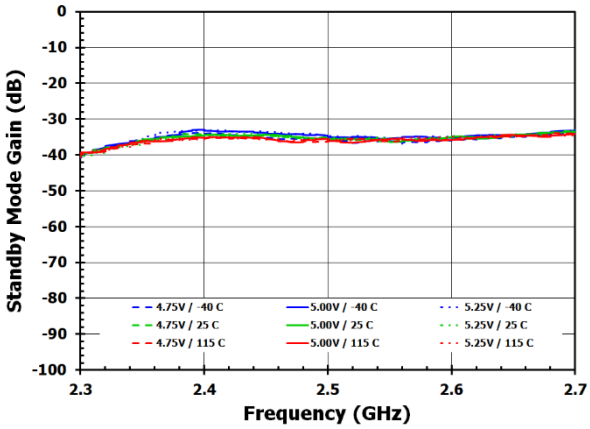


Figure 13. Standby Mode Gain

3.2 Typical Performance Graphs

3.2.1. 3.3GHz to 3.8GHz

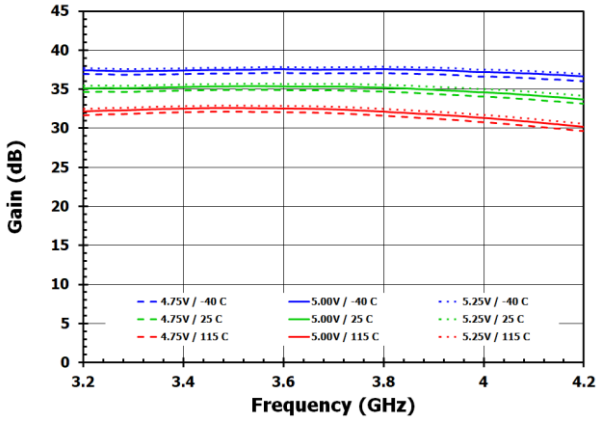


Figure 14. Gain

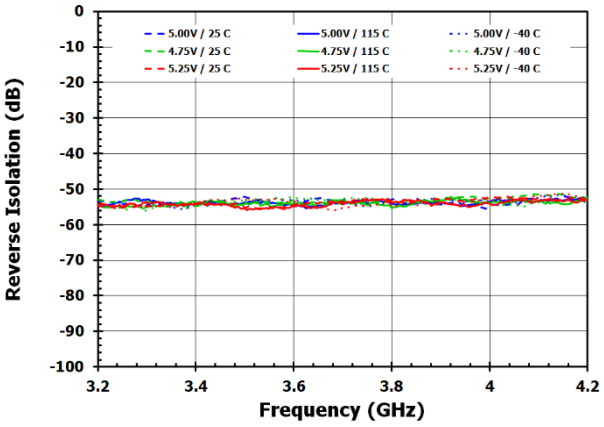


Figure 15. Reverse Isolation

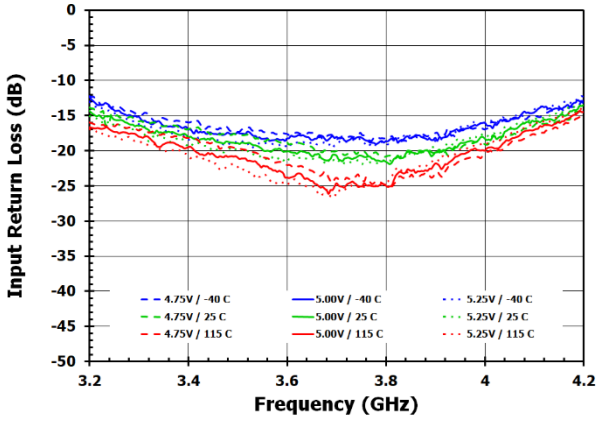


Figure 16. Input Return Loss

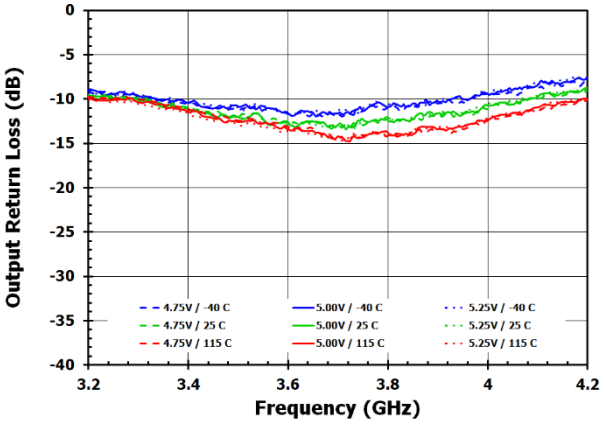


Figure 17. Output Return Loss

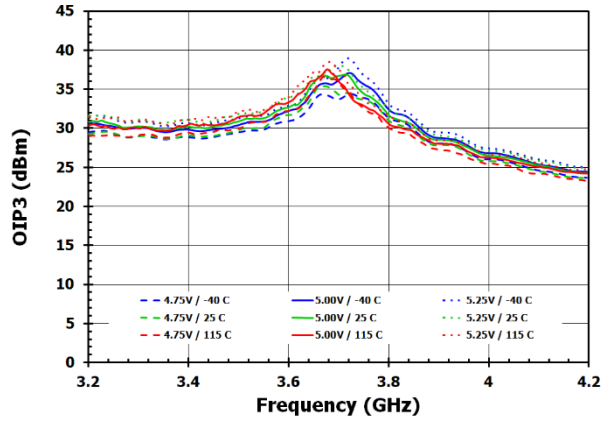


Figure 18. OIP3

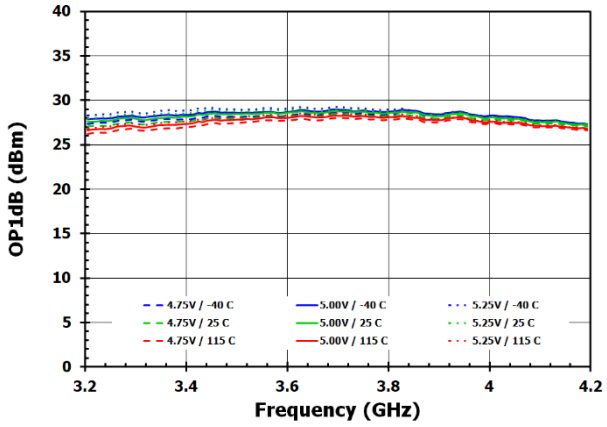


Figure 19. OP1dB

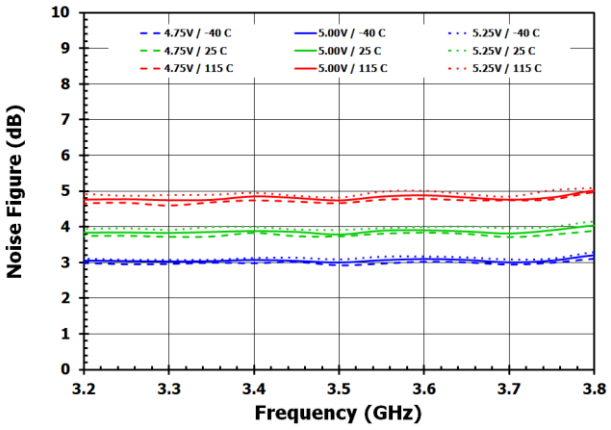


Figure 20. Noise Figure

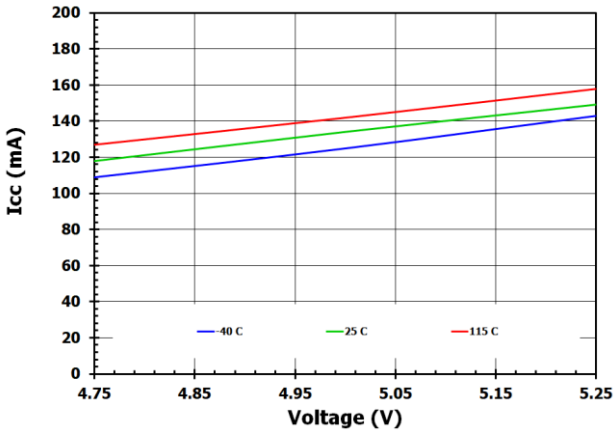


Figure 21. Quiescent Current

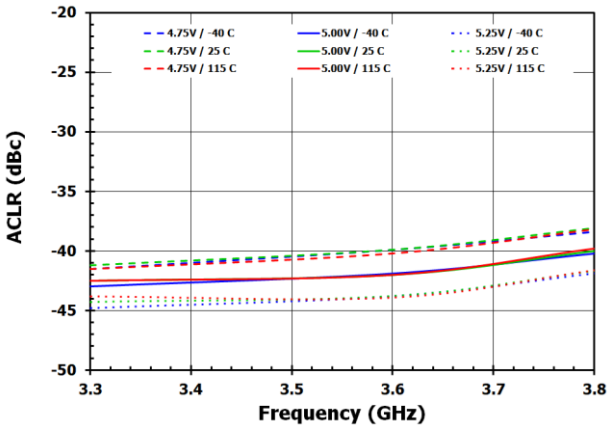


Figure 22. ACLR, 20MHz LTE
Pout = 15dBm + 8.5dB PAR, 0.01% Probability

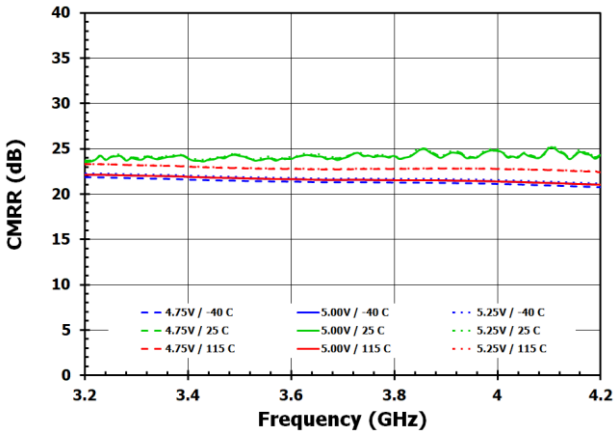


Figure 23. CMRR

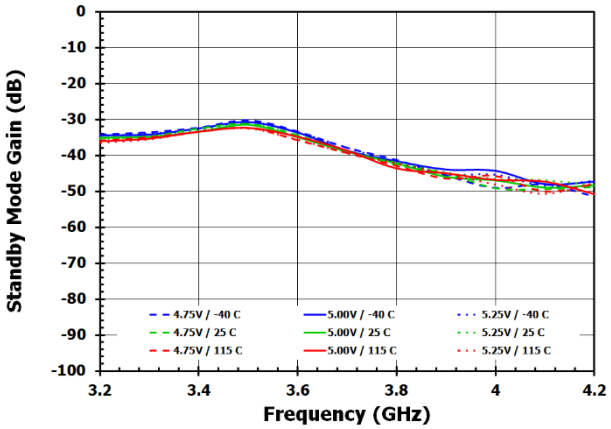


Figure 24. Standby Mode Gain

4. Functional Description

4.1 Standby

The F1427 can be turned off for low current consumption. This is done by applying a logic voltage to Pin 16 using Table 1.

Table 1. Standby Truth Table

STBY	Condition
Logic HIGH / NC	Full operation
Logic LOW	Amplifier OFF

5. Evaluation Board

5.1 Evaluation Board Images

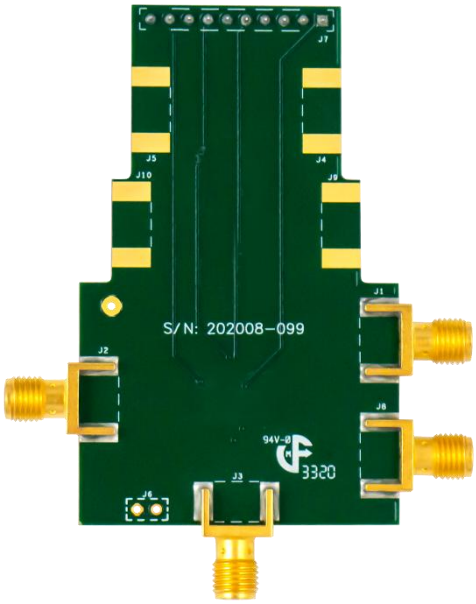


Figure 25. Evaluation Board – Front

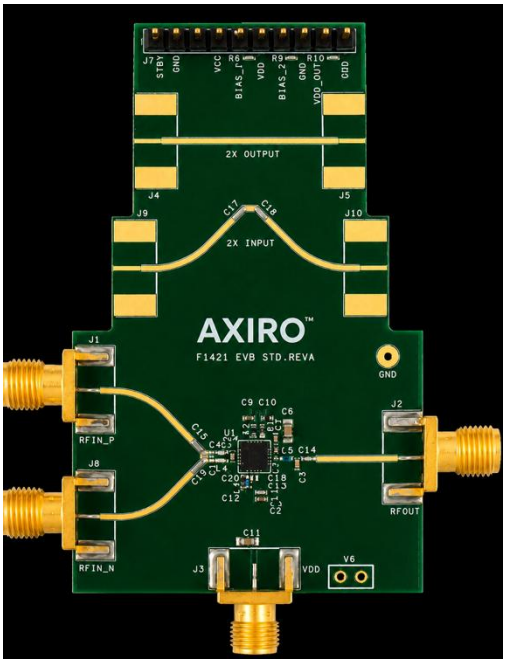


Figure 26. Evaluation Board – Back

5.2 Evaluation Board Schematic

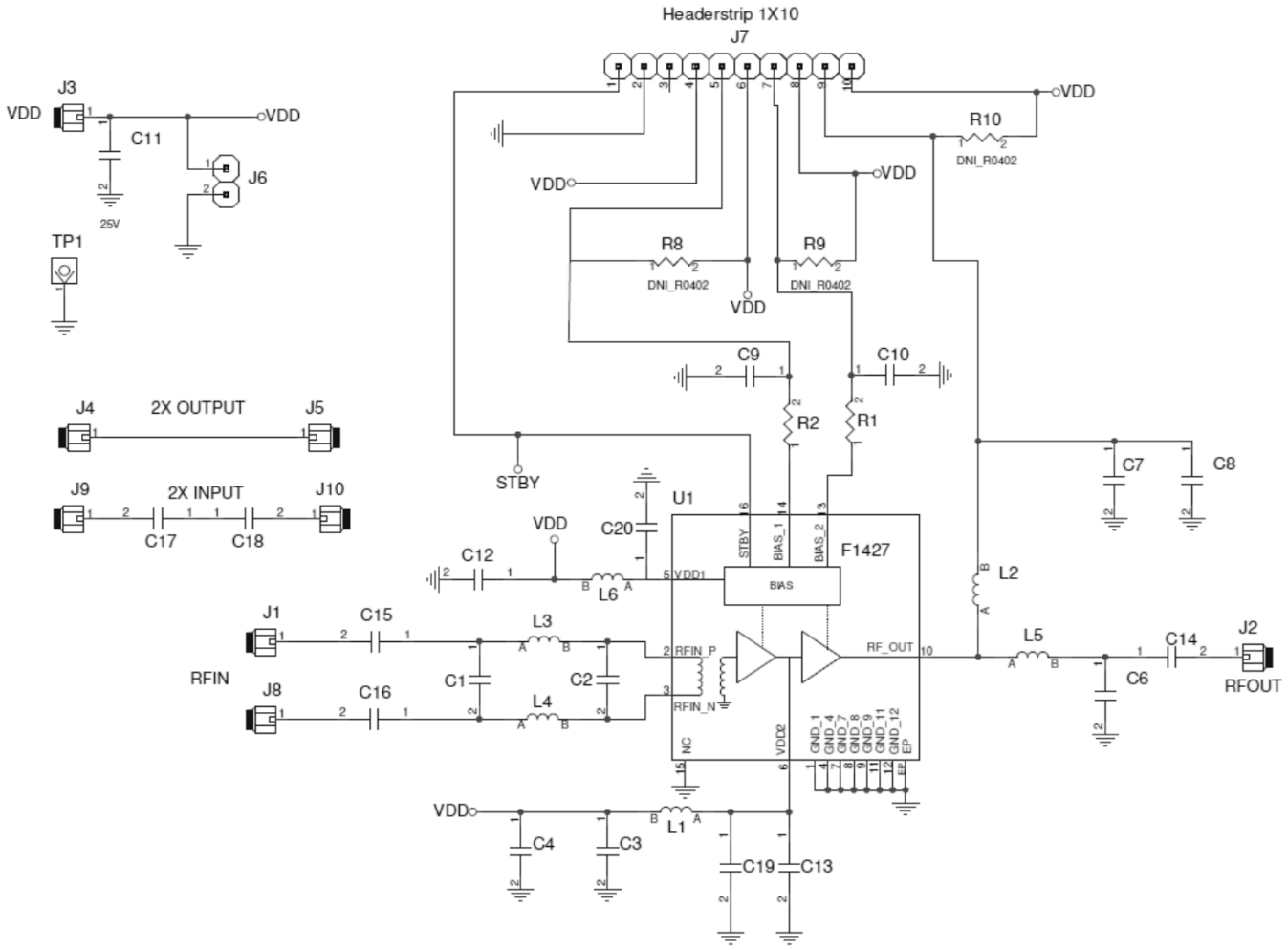


Figure 27. Evaluation Board Schematic

5.3 Bill of Materials

Table 2. Evaluation Kit Bill of Material (BOM) – 2.3GHz to 2.7GHz

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C15,C16,C17,C18, R2, R8, R9, R10,L5	9	0Ω ±1% 0.1W Resistor (0402)	ERJ-2GE0R00X	Panasonic
R1	1	24Ω ±1% 0.1W Resistor (0402)	ERJ2RKF24R0	Panasonic
C1, C13, C19, C20	4	DNI		Murata
C2	1	0.4pF ±0.1pF, 50V, C0G Ceramic Capacitor (0402)	GJM1555C1HR40BB01	Murata
C3, C7	2	10pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GJM1555C1H100JB01	Murata
C4	1	10nF ±10%, 25V, C0G Ceramic Capacitor (0402)	GRM155R71E103K	Murata
C6	1	1.1pF ±0.1pF, 50V, C0G Ceramic Capacitor (0402)	GJM1555C1H1R1BB01	Murata
C8	1	560pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H561JA01	Murata
C9, C10	2	33pF ±5%, 25V, C0G Ceramic Capacitor (0402)	GRM1555C1E330J	Murata
C11	1	1µF ±10%, 25V, C0G Ceramic Capacitor (0603)	GRM188R61E105K	Murata
C12	1	39pF ±5%, 25V, C0G Ceramic Capacitor (0201)	GRM0335C1E390JD01B	Murata
C14	1	3.3pF ±0.1pF, 50V, C0G Ceramic Capacitor (0402)	GJM1555C1H3R3BB01	Murata
L1	1	0.6nH ±0.1nH, 600mA, Inductor (0201)	LQP03TN0N6B02	Murata
L2	1	3.9nH ±0.1nH, 750mA, Inductor (0402)	LQG15HS3N9B02D	Murata
L3, L4	2	2.0pF ±0.1pF, 50V, C0G Ceramic Capacitor (0402)	GJM1555C1H2R0BB01	Murata
L6	1	0.7nH ±0.1nH, 800mA, Inductor (0201)	LQP03TN0N7B02D	Panasonic
J1, J2, J3, J8	4	Edge Launch SMA (0.375-inch pitch ground, tab, 50Ω)	142-0701-851	Emerson Johnson
J7	1	CONN HEADER VERT 1x10	0022284103	Molex
J4,J5,J9,J10	4	DNI	142_0701_851	Molex
U1	1	F1427 Amplifier	F1427	Axiro

Table 3. Evaluation Kit Bill of Material (BOM) – 3.3GHz to 3.8GHz

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C15,C16,C17,C18, R2, R8, R9, R10, L1, L6	10	0Ω ±1% 0.1W Resistor (0402)	ERJ-2GE0R00X	Panasonic
R1	1	51Ω ±1% 0.1W Resistor (0402)	ERJ2RKF51R0	Panasonic
C1, C12, C13	3	DNI		Murata
C2	1	0.2pF ±0.1pF, 50V, C0G Ceramic Capacitor (0402)	GJM1555C1HR20BB01	Murata
C3,C7,C9,C10	4	33pF ±5%, 25V, C0G Ceramic Capacitor (0402)	GRM1555C1E330J	Murata
C4	1	1µF ±15%, 25V, C0G Ceramic Capacitor (0402)	GRM155R61E105KE11	Murata
C6	1	0.7pF ±0.1pF, 50V, C0G Ceramic Capacitor (0402)	GJM1555C1HR70BB01	Murata
C8	1	3300pF ±5%, 50V, C0G Ceramic Capacitor (0603)	GRM1885C1H332JA01	Murata
C11	1	1µF ±10%, 25V, C0G Ceramic Capacitor (0603)	GRM188R61E105K	Murata
C14	1	1.9pF ±0.1pF, 50V, C0G Ceramic Capacitor (0402)	GJM1555C1H1R9BB01	Murata
C19	1	4.3pF ±0.1pF, 50V, C0G Ceramic Capacitor (0201)	GJM0335C1H4R3BB01	Murata
C20	1	12pF ±0.1pF, 50V, C0G Ceramic Capacitor (0201)	GJM0335C1H120GB01	Murata
L2	1	3.9nH ±0.1nH, 750mA,, Inductor (0402)	LQW15AN3N9B00	Murata
L3, L4	2	1.3pF ±0.1pF, 50V, C0G Ceramic Capacitor (0402)	GJM1555C1H1R3BB01	Murata
L5	1	7pF ±0.1pF, 50V, C0G Ceramic Capacitor (0402)	GJM155C1H7R0BB01	Murata
J1, J2, J3, J8	4	Edge Launch SMA (0.375-inch pitch ground, tab, 50Ω)	142-0701-851	Emerson Johnson
J7	1	CONN HEADER VERT 1x10	0022284103	Molex
J4,J5,J9,J10	4	DNI	142_0701_851	Molex
U1	1	F1427 Amplifier	F1427	Axiro

6. Application Notes

RF Input DC blocking capacitors are not necessary if the DC offset on each input is equal.

6.1 Power Supplies

Use a common V_{CC} power supply for all pins requiring DC power. Bypass all supply pins with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change, or transients should have a slew rate smaller than 1V/20µs. In addition, keep all control pins at 0V (±0.3V) while the supply voltage ramps or while it returns to zero.

7. Package Outline Drawings

The package outline drawings are accessible from the Axiro website (see package links in "Ordering Information"). The package information is the most current data available and is subject to change without revision of this document.

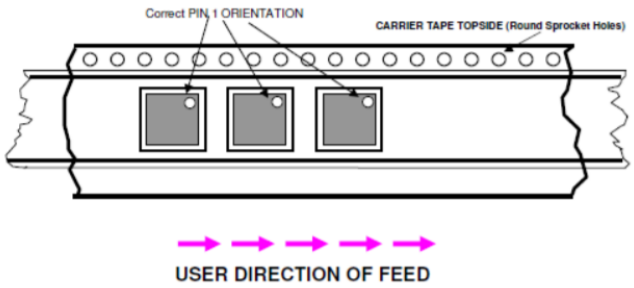
8. Marking Diagram

Top Marking Illustration	Marking	Representation
	$	Factory Code
	Y	Last Digit of the Year
	WW	Work Week
	***	Lot Sequential Code

9. Ordering Information

Part Number	Package Description	MSL Rating	Carrier Type	Temp. Range (°C)
RA81F1427STGNM#BD0	3.0 × 3.0 mm 16-VFQFPN	1	Tray	-40 to +115
RA81F1427STGNM#KD0	3.0 × 3.0mm 16-VFQFPN	1	Tape and Reel	-40 to +115
RTKA81F1427ST260RU	Evaluation Board for 2.3GHz to 2.7GHz Band			
RTKA81F1427ST360RU	Evaluation Board for 3.3GHz to 3.8GHz Band			

Table 4. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
KD0	Quadrant 2 (EIA-481-E)	

10. Revision History

Revision	Date	Description
2.00	Jun 24, 2026	Updated document branding and layout to Axiro Semiconductor standard. No changes to device functionality or specifications.