

F1476

High Linearity RF Driver Amplifier 3000MHz to 5000MHz

Description

The F1476 is a high linearity RF Driver Amplifier designed to operate within the 3000MHz to 5000MHz frequency range. Using a 5V power supply, the F1476 provides 18dB typical gain and 27.5dBm typical OP1dB with a quiescent current consumption of 200mA.

The F1476 is packaged in a 4mm × 4mm, 20-VFQFPN package, with matched 50Ω input and output impedances for ease of integration into the signal path.

Advantages

- High linearity
- Compact 4mm × 4mm 20-VFQFPN package
- Robust ESD Performance
 - 1kV HBM ESD rating
 - 500V CDM ESD rating

Features

- Frequency range: 3000MHz to 5000MHz
- 18dB typical gain at 4000MHz
- +27.5dBm typical OP1dB at 4000MHz
- ACLR < -55dBc at 4000MHz
- 50Ω Single-ended input and output impedances
- 5V power supply
- 200mA typical quiescent supply current
- 1.8V logic compatible standby mode for power savings
- Operating temperature (T_{EPAD}) range: -40°C to +115°C
- 4mm × 4 mm 20-VFQFPN package

Applications

- 5G Sub-6GHz AAS/Massive MIMO
- FDD or TDD systems
- General purpose RF

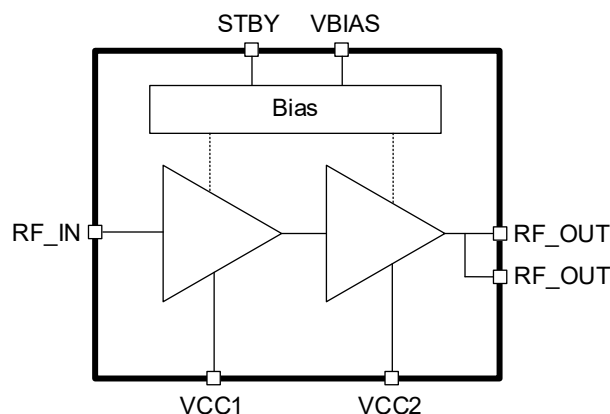


Figure 1. Block Diagram

Contents

1. Pin Information	Error! Bookmark not defined.
1.1 Pin Assignments.....	Error! Bookmark not defined.
1.2 Pin Descriptions.....	Error! Bookmark not defined.
2. Specifications	Error! Bookmark not defined.
2.1 Absolute Maximum Ratings.....	5
2.2 Recommended Operating Conditions.....	Error! Bookmark not defined.
2.3 Thermal Specifications.....	Error! Bookmark not defined.
2.4 Electrical Specifications.....	Error! Bookmark not defined.
2.4.1. Electrical Characteristics – General.....	Error! Bookmark not defined.
2.4.2. Electrical Characteristics – 3300MHz to 3800MHz.....	Error! Bookmark not defined.
2.4.3. Electrical Characteristics – 3700MHz to 4000MHz.....	Error! Bookmark not defined.
2.4.4. Electrical Characteristics – 4700MHz to 5000MHz.....	Error! Bookmark not defined.
3. Typical Operating Conditions	Error! Bookmark not defined.
4. Typical Performance Graphs	Error! Bookmark not defined.
4.1 3300MHz to 3800MHz.....	10
4.2 3700MHz to 4000MHz.....	12
4.3 4700MHz to 5000MHz.....	14
5. Functional Information	Error! Bookmark not defined.
6. Evaluation Board Information	Error! Bookmark not defined.
6.1 Evaluation Board Picture.....	Error! Bookmark not defined.
6.2 Application Circuit.....	Error! Bookmark not defined.
6.3 Bill-of-Materials (BOM)	Error! Bookmark not defined.
6.3.1. 3300MHz to 3800MHz	17
6.3.2. 3700MHz to 4000MHz	18
6.3.3. 4700MHz to 5000MHz	19
7. Package Outline Drawings	Error! Bookmark not defined.
8. Marking Diagram	Error! Bookmark not defined.
9. Ordering Information	Error! Bookmark not defined.
10. Revision History	Error! Bookmark not defined.

Figures

Figure 1. Block Diagram.....	1
Figure 2. Pin Assignments – Top View.....	4
Figure 3. Gain 3.3 - 3.8GHz	10
Figure 4. Reverse Isolation 3.3 - 3.8GHz	10
Figure 5. Input Return Loss 3.3 - 3.8GHz.....	10
Figure 6. Output Return Loss 3.3 - 3.8GHz.....	10
Figure 7. Standby Mode Gain 3.3 - 3.8GHz	10

Figure 8. Noise Figure 3.3 - 3.8GHz.....	10
Figure 9. Stability K-Factor 3.3 - 3.8GHz.....	11
Figure 10. OP1dB 3.3 - 3.8GHz	11
Figure 11. OIP3 3.3 - 3.8GHz $\Delta f = 20\text{MHz}$, Pout/Tone = +5dBm.....	11
Figure 12. ACLR 3.3 - 3.8GHz LTE20MHz, Pout = +15dBm	11
Figure 13. Gain 3.7 - 4.0GHz	12
Figure 14. Reverse Isolation 3.7 - 4.0GHz	12
Figure 15. Input Return Loss 3.7 - 4.0GHz.....	12
Figure 16. Output Return Loss 3.7 - 4.0GHz	12
Figure 17. Standby Mode Gain 3.7 - 4.0GHz	12
Figure 18. Noise Figure 3.7 - 4.0GHz.....	12
Figure 19. Stability K-Factor 3.7 - 4.0GHz.....	13
Figure 20. OP1dB 3.7 - 4.0GHz.....	13
Figure 21. OIP3 3.7 - 4.0GHz $\Delta f = 20\text{MHz}$, Pout/Tone = +5dBm.....	13
Figure 22. ACLR 3.7 - 4.0GHz LTE20MHz, Pout = +15dBm	13
Figure 23. Gain 4.7 - 5.0GHz	14
Figure 24. Reverse Isolation 4.7 - 5.0GHz	14
Figure 25. Input Return Loss 4.7 - 5.0GHz.....	14
Figure 26. Output Return Loss 4.7 - 5.0GHz.....	14
Figure 27. Standby Mode Gain 4.7 - 5.0GHz	14
Figure 28. Noise Figure 4.7 - 5.0GHz.....	14
Figure 29. Stability K-Factor 4.7 - 5.0GHz.....	15
Figure 30. OP1dB 4.7 - 5.0GHz	15
Figure 31. OIP3 4.7 - 5.0GHz $\Delta f = 20\text{MHz}$, Pout/Tone = +5dBm.....	15
Figure 32. ACLR 4.7 - 5.0GHz LTE20MHz, Pout = +15dBm	15
Figure 33. Evaluation Board – Top View	16
Figure 34. Evaluation Board – Bottom View.....	16
Figure 35. Evaluation Board Schematic.....	17

Pin Assignments

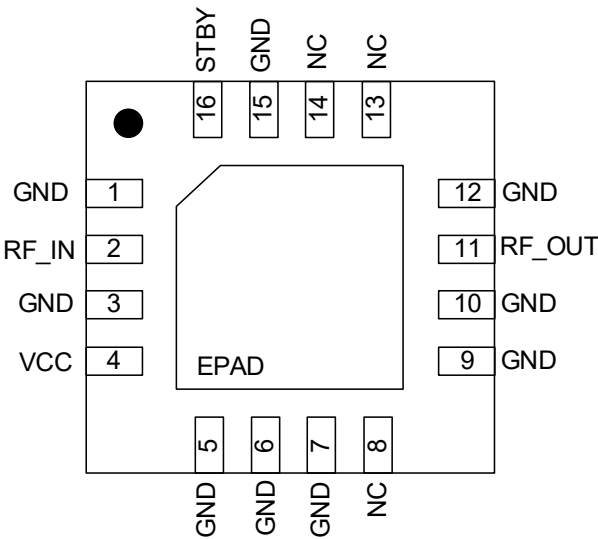


Figure 2. Pin Assignments – Top View

Pin Descriptions

Pin Number	Pin Name	Description
1, 5, 8, 9, 10, 15, 17, 19	NC	No internal connection. These pins can remain unconnected or be connected to ground (recommended). Use a via as close to the pin as possible if grounded.
2, 4, 7, 11, 14	GND	Internally grounded. This pin must be grounded with vias as close to the pin as possible.
3	RF_IN	RF input internally matched to 50Ω. Must use an external DC block.
6	VCC1	Connect pin directly to VCC.
12, 13	RF_OUT	RF output. Pull up to VCC through inductor. Must use an external DC block.
16	VCC2	Connect pin directly to VCC. Axiro recommends placing a decoupling capacitor as close to this pin as possible.
18	VBIAS	Connect pin to VCC through a biasing resistor. Axiro recommends placing a decoupling capacitor as close to this pin as possible.
20	STBY	Standby pin. With Logic LOW applied to this pin the amplifier is powered off. With Logic HIGH applied to this pin (or if the pin is left unconnected), the part is in full operation mode.
-	EPAD	Exposed Pad. Internally connected to the ground. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the noted RF performance.

Absolute Maximum Ratings

Stresses above those listed can cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Parameter	Symbol	Minimum	Maximum	Unit
V _{CC} to GND	V _{CC}	-0.3	6.0	V
V _{BIAS} to GND	V _{DD}	-0.3	6.0	V
STBY	V _{STBY}	-0.3	5.0	V
RFIN Externally Applied DC Voltage	V _{RFIN}	-	2.5	V
RFOUT Externally Applied DC Voltage	V _{RFOUT}	-	6.0	V
Maximum CW Input Power applied for 24 hours. V _{CC} = 5V, T _{EPAD} = 115°C, 50Ω system. Standby = logic HIGH: ON state. [1]	P _{MAX_IN_ON}	-	15	dBm
Maximum CW Input Power applied for 24 hours. V _{CC} = 5V, T _{EPAD} = 115°C, 50Ω system. Standby = logic LOW: OFF state. [1]	P _{MAX_IN_OFF}	-	15	dBm
Junction Temperature	T _{JMAX}	-	175	°C
Storage Temperature Range	T _{st}	-65	150	°C
Lead Temperature (soldering, 10s)	-	-	260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V _{ESDHBM}	-	1000	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)	V _{ESDCDM}	-	500	V

1. Exposure to these maximum RF levels can result in significantly higher ICC current draw because of overdriving the amplifier stages.

Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power Supply Voltage	V _{DD}	-	4.75	5	5.25	V
Operating Temperature Range [1]	T _{EPAD_OP}	Exposed paddle	-40	-	+115	°C
RF Frequency Range	f _{RF}	-	3000	-	5000	MHz
RFIN Port Impedance	Z _{RFI}	Single-ended	-	50	-	Ω
RFOUT Port Impedance	Z _{RFO}	Single-ended	-	50	-	Ω

1. Electrical specifications are confirmed within this temperature range unless otherwise specified.

Thermal Specifications

Parameter	Symbol	Value	Unit
Junction to Ambient Thermal Resistance.	θ_{JA}	51.4	°C/W
Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	θ_{JC-BOT}	27	°C/W
Moisture Sensitivity Rating (Per J-STD-020)	-	MSL1	-

Electrical Characteristics

Specifications apply when operated as a TX amplifier with $V_{CC} = +5.0V$, $V_{BIAS} = +5.0V$, $T_{EPAD} = +25^{\circ}C$, $STBY = HIGH$, $Z_S = Z_L = 50\Omega$, Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Logic Input High	V_{IH}	-	0.99^[1]	-	V_{CC}	V
Logic Input Low	V_{IL}	-	-0.3	-	0.78	V
Logic Current	I_{IH}, I_{IL}	STBY pin. VSTBY = 1.8V	-150	-	150	μA
Quiescent Current ^[2]	I_{CCQ}	3.3GHz to 3.8GHz BOM	-	242	287	mA
		3.7GHz to 4.0GHz BOM		195	240	mA
		4.7GHz to 5.0GHz BOM		190	235	mA
Standby Current	I_{CC_STBY}	STBY = LOW	-	-	22	mA
Standby Enable/Disable Settling Time	t_{SETTLE}	Settling time for disable to enable. 50% TX_EN control to RF output within 0.25dB and 1° of the on-state final value. $T_{EPAD} = -40^{\circ}C$ to $115^{\circ}C$, $V_{CC} = +4.75V$ to $5.25V$	-	-	1	μs
		Settling time for enable to disable. Gain shall be <5% of the gain in enable state.	-	-	1	

1. Specifications in the minimum/maximum columns that are shown in **bold italics** are confirmed by test.
2. I_{CCQ} refers to the nominal small signal bias current.

Electrical Characteristics (3000MHz – 3800MHz)

Typical specifications apply when operated as an amplifier with tuning optimized for 3300MHz to 3800MHz band, $V_{CC} = +5.0V$, $V_{BIAS} = +5.0V$, $f_{RF} = 3600MHz$, $T_{EPAD} = +25^{\circ}C$, $STBY = HIGH$, $Z_S = Z_L = 50\Omega$. Minimum and Maximum specifications apply across process, recommended operating voltage, full performance temperature, and tuned frequency range unless otherwise stated. Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	-	15.9	18	-	dB
Gain Variation Over Process	G_{PROC}	-	-	-	0.9	dB
Gain Variation Over Temperature	G_{TEMP}	-	-	-	2.5	dB
Gain Flatness	G_{FLAT}	Every 100MHz	-	-	0.45	dB
		Every 250MHz	-	-	0.8	dB
		Every 500MHz	-	-	0.8	dB
STBY Mode Gain	G_{STBY}	STBY = logic LOW, $P_{IN} \leq -10dBm$	-	-24	-	dB
RF Input Return Loss	RL_{RFIN}	-	7.8	12.5	-	dB
RF Output Return Loss	RL_{RFOUT}	-	6.7	10.5	-	dB
Reverse Isolation	ISO_{REV}	-	-	-45	-	dB
Noise Figure	NF	-	-	5.3	6.7	dB
Output Third Order Intercept Point	OIP3	$P_{out} = +5dBm/tones$, $\Delta f = 20MHz$.	35.8	44.1	-	dBm
Output 1dB Compression Point	OP1dB	-	26	28	-	dBm
ACLR	ACLR	LTE 20MHz signal, $P_{out} = 15dBm$, 9dB PAR, CCDF = 0.01%.	-	-57	-50	dBc
Stability K-Factor	K_{FACT}	$f_{RF} = Up\ to\ 20GHz$	1	-	-	

Electrical Characteristics (3700MHz – 4000MHz)

Typical specifications apply when operated as an amplifier with tuning optimized for 3700MHz to 4000MHz band, $V_{CC} = +5.0V$, $V_{BIAS} = +5.0V$, $f_{RF} = 3900MHz$, $T_{EPAD} = +25^{\circ}C$, $STBY = HIGH$, $Z_S = Z_L = 50\Omega$. Minimum and Maximum specifications apply across process, recommended operating voltage, full performance temperature, and tuned frequency range unless otherwise stated. Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	-	15.5	18	-	dB
Gain Variation Over Process	G_{PROC}	-	-	-	0.62	dB
Gain Variation Over Temperature	G_{TEMP}	-	-	-	3.4	dB
Gain Flatness	G_{FLAT}	Every 100MHz	-	-	0.6	dB
		Every 300MHz	-	-	1.1	dB
STBY Mode Gain	G_{STBY}	STBY = logic LOW, $P_{IN} \leq -10dBm$	-	-25	-	dB
RF Input Return Loss	RL_{RFIN}	-	7.0	23	-	dB
RF Output Return Loss	RL_{RFOUT}	-	7.5	11	-	dB
Reverse Isolation	ISO_{REV}	-	-	-44	-	dB
Noise Figure	NF	-	-	5.6	6.7	dB
Output Third Order Intercept Point	OIP3	$P_{out} = +5dBm/tones$, $\Delta f = 20MHz$.	36.5	41.8	-	dBm
Output 1dB Compression Point	OP1dB	-	26.8	28.8	-	dBm
ACLR	ACLR	LTE 20MHz signal, $P_{out} = 15dBm$, 9dB PAR, CCDF = 0.01%.	-	-58	-52	dBc
Stability K-Factor	K_{FACT}	$f_{RF} = Up\ to\ 20GHz$	1	-	-	-

Electrical Characteristics (4700MHz – 5000MHz)

Typical specifications apply when operated as an amplifier with tuning optimized for 4700MHz to 5000MHz band, $V_{CC} = +5.0V$, $V_{BIAS} = +5.0V$, $f_{RF} = 4900MHz$, $T_{EPAD} = +25^{\circ}C$, $STBY = HIGH$, $Z_S = Z_L = 50\Omega$. Minimum and Maximum specifications apply across process, recommended operating voltage, full performance temperature, and tuned frequency range unless otherwise stated. Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	-	14.7	17	-	dB
Gain Variation Over Process	G_{PROC}	-	-	-	0.55	dB
Gain Variation Over Temperature	G_{TEMP}	-	-	-	3.4	dB
Gain Flatness	G_{FLAT}	Every 100MHz	-	-	0.5	dB
		Every 300MHz	-	-	1.3	dB
STBY Mode Gain	G_{STBY}	STBY = logic LOW, $P_{IN} \leq -10dBm$	-	-30	-	dB
RF Input Return Loss	RL_{RFIN}	-	11	27.5	-	dB
RF Output Return Loss	RL_{RFOUT}	-	9.1	12.2	-	dB
Reverse Isolation	ISO_{REV}	-	-	-40	-	dB
Noise Figure	NF	-	-	4.3	5.6	dB
Output Third Order Intercept Point	OIP3	$P_{out} = +5dBm/tones$, $\Delta f = 20MHz$.	26.8	30.5	-	dBm
Output 1dB Compression Point	OP1dB	-	25.1	27.5	-	dBm
ACLR	ACLR	LTE 20MHz signal, $P_{out} = 15dBm$, 9dB PAR, CCDF = 0.01%.	-	-53.4	-48	dBc
Stability K-Factor	K_{FACT}	$f_{RF} = Up\ to\ 20GHz$	1	-	-	-

Typical Operating Conditions

Unless otherwise noted, the following conditions apply for the TOC graphs on the following pages:

- $V_{CC} = 5.0V$
- $Z_L = Z_S = 50\Omega$ Single-ended
- $T_{EP} = +25^{\circ}C$
- All temperatures are referenced to the exposed paddle
- ACLR measurements used with LTE signal, 20MHz, PAR = 9dB at 0.01% probability
- Evaluation Kit traces and connector losses are de-embedded

Typical Performance Graphs

1.1 3300MHz to 3800MHz

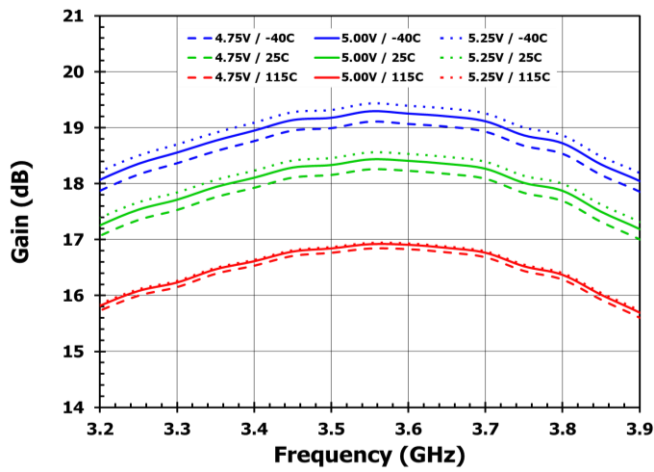


Figure 3. Gain 3.3 - 3.8GHz

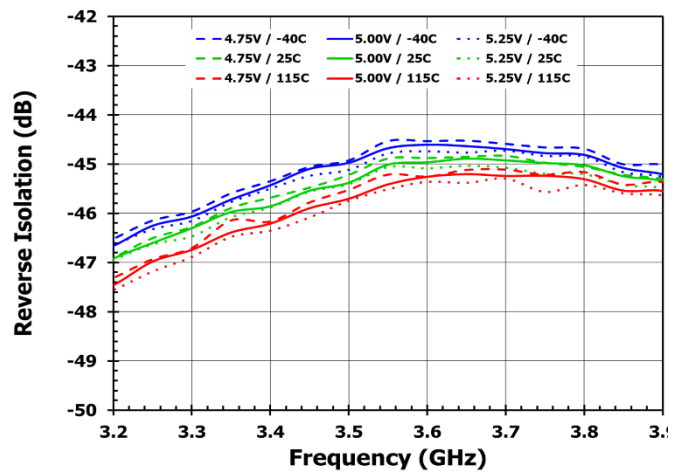


Figure 4. Reverse Isolation 3.3 - 3.8GHz

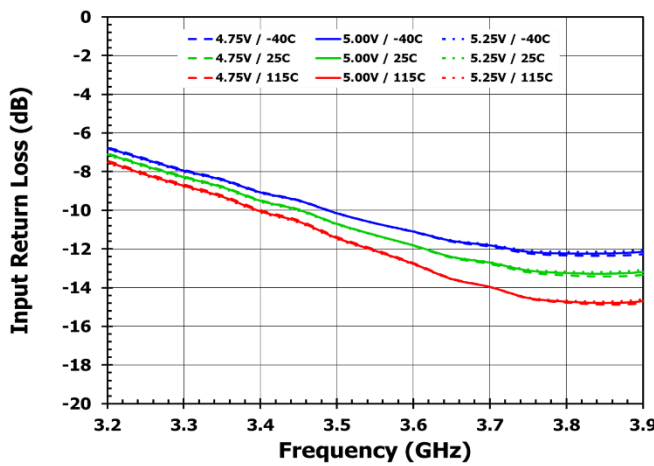


Figure 5. Input Return Loss 3.3 - 3.8GHz

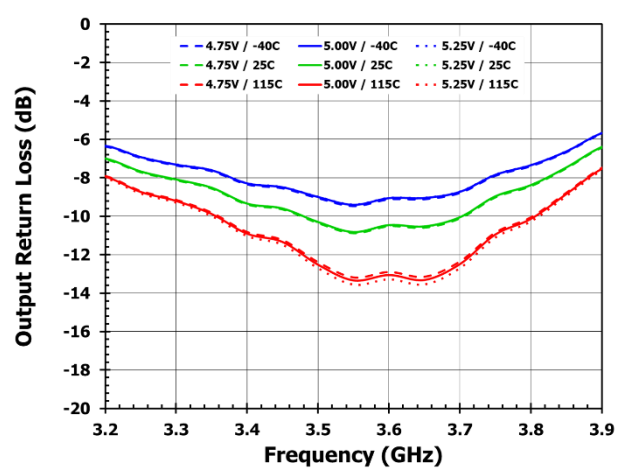


Figure 6. Output Return Loss 3.3 - 3.8GHz

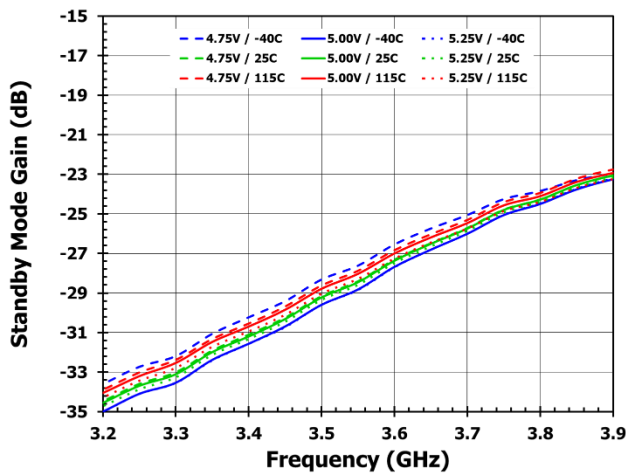


Figure 7. Standby Mode Gain 3.3 - 3.8GHz

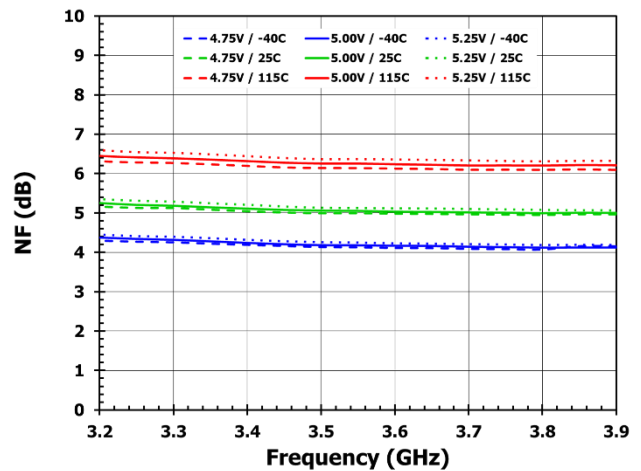


Figure 8. Noise Figure 3.3 - 3.8GHz

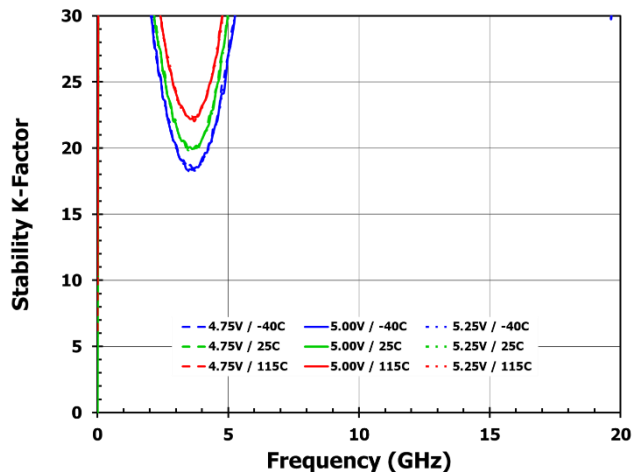


Figure 9. Stability K-Factor 3.3 - 3.8GHz

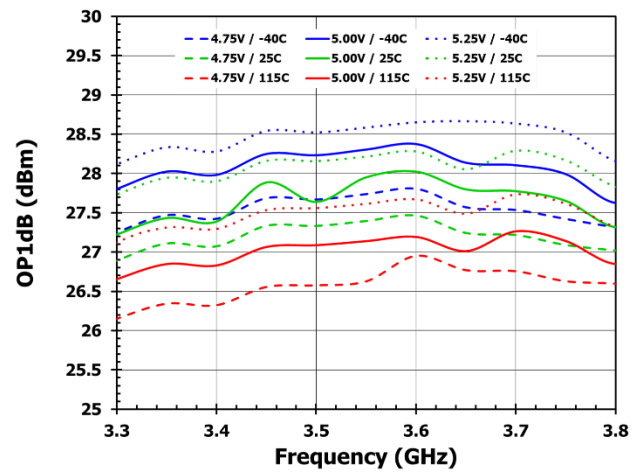


Figure 10. OP1dB 3.3 - 3.8GHz

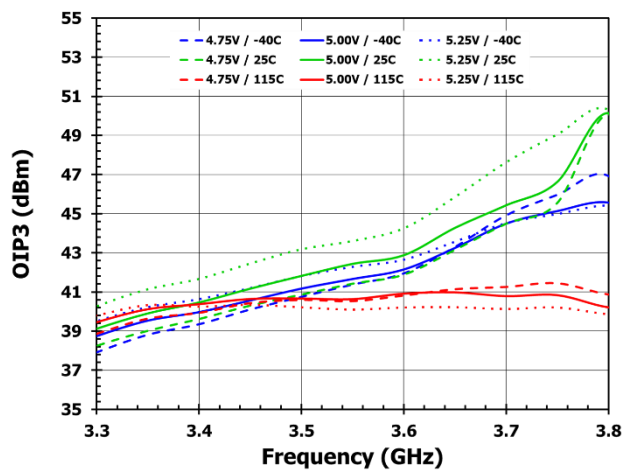


Figure 11. OIP3 3.3 - 3.8GHz $\Delta f = 20\text{MHz}$, $P_{\text{out}}/\text{Tone} = +5\text{dBm}$

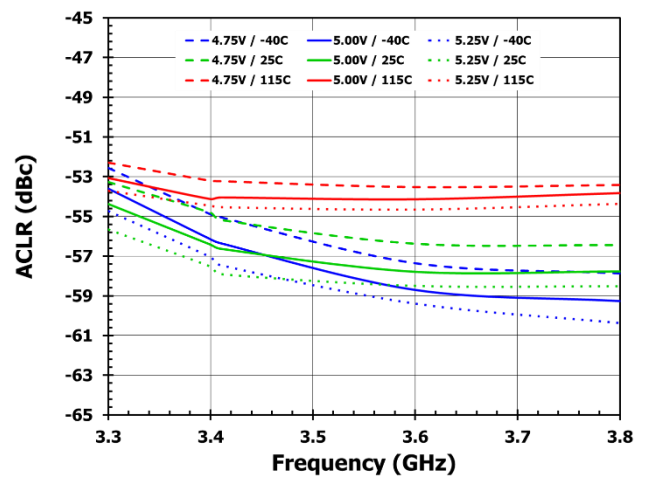


Figure 12. ACLR 3.3 - 3.8GHz LTE20MHz, $P_{\text{out}} = +15\text{dBm}$

1.2 3700MHz to 4000MHz

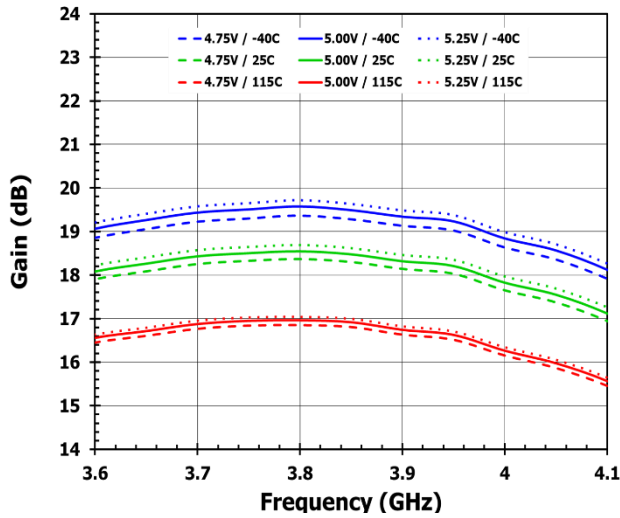


Figure 13. Gain 3.7 - 4.0GHz

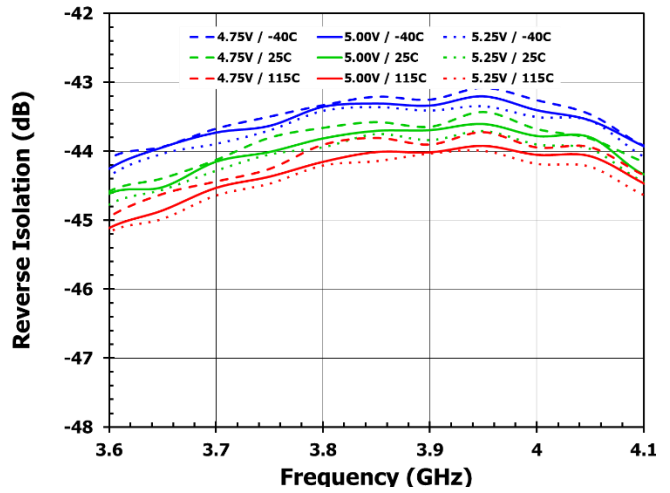


Figure 14. Reverse Isolation 3.7 - 4.0GHz

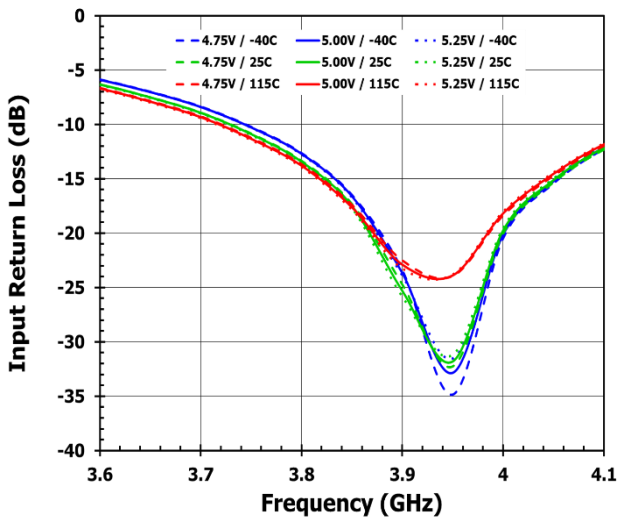


Figure 15. Input Return Loss 3.7 - 4.0GHz

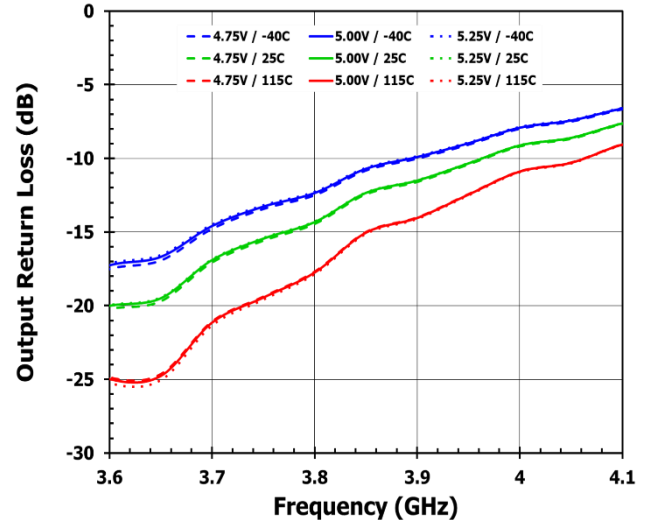


Figure 16. Output Return Loss 3.7 - 4.0GHz

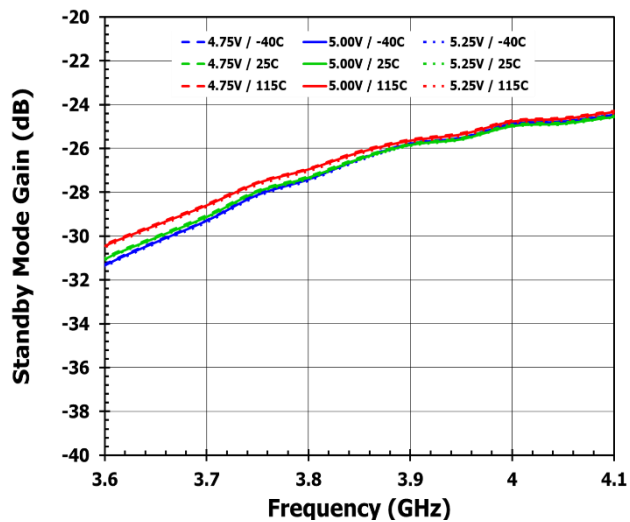


Figure 17. Standby Mode Gain 3.7 - 4.0GHz

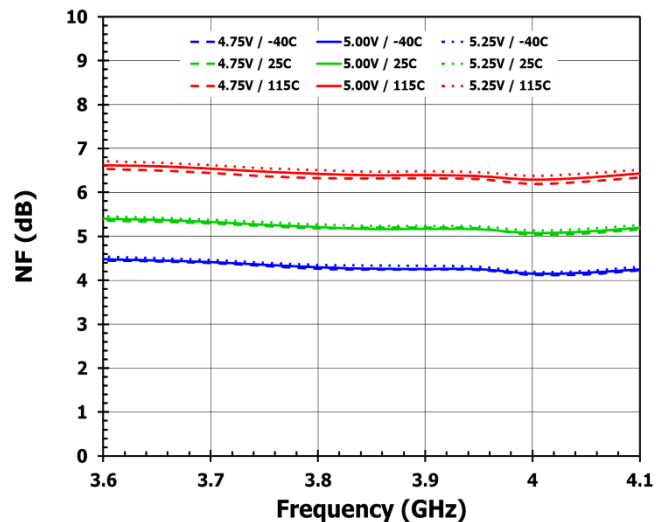


Figure 18. Noise Figure 3.7 - 4.0GHz

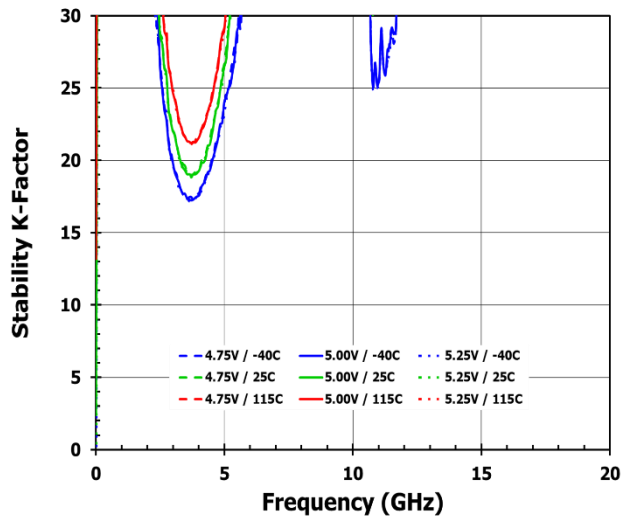


Figure 19. Stability K-Factor 3.7 - 4.0GHz

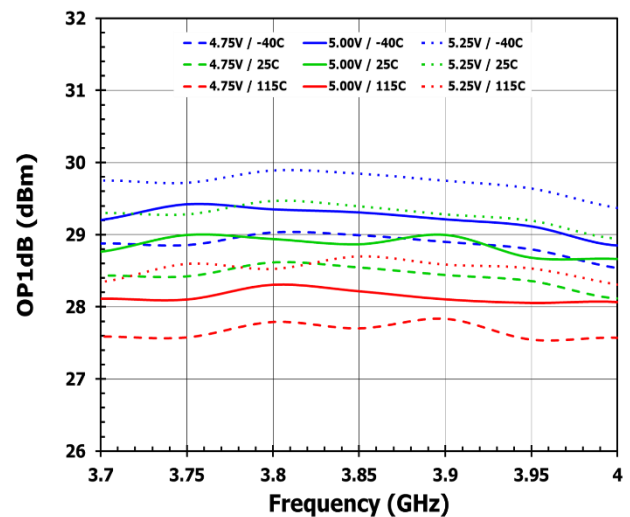


Figure 20. OP1dB 3.7 – 4.0GHz

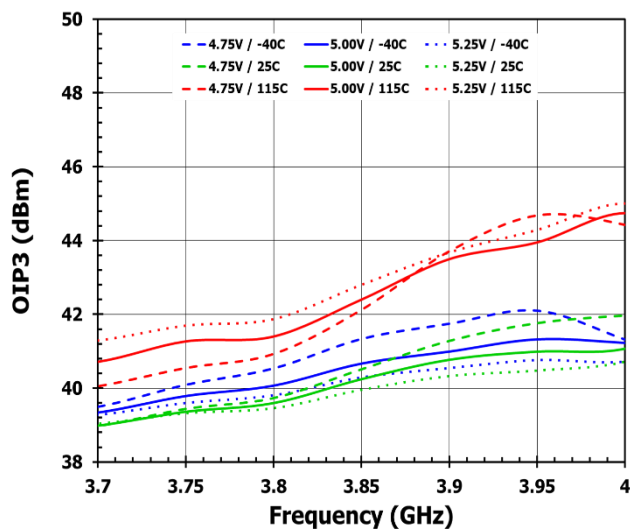


Figure 21. OIP3 3.7 - 4.0GHz $\Delta f = 20\text{MHz}$, $P_{\text{out}}/\text{Tone} = +5\text{dBm}$

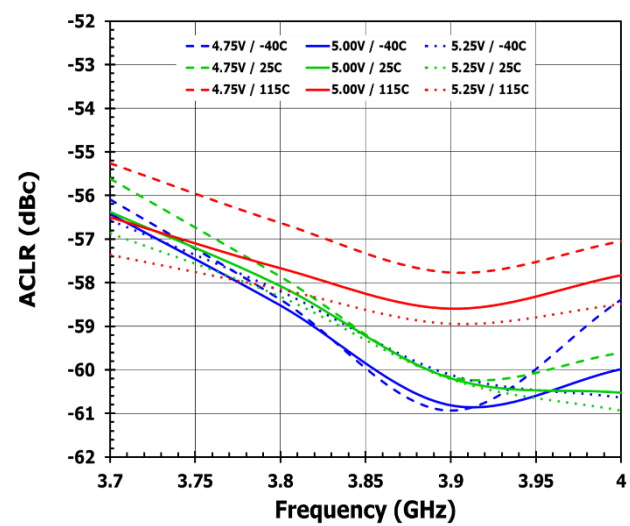


Figure 22. ACLR 3.7 - 4.0GHz LTE20MHz, $P_{\text{out}} = +15\text{dBm}$

1.3 4700MHz to 5000MHz

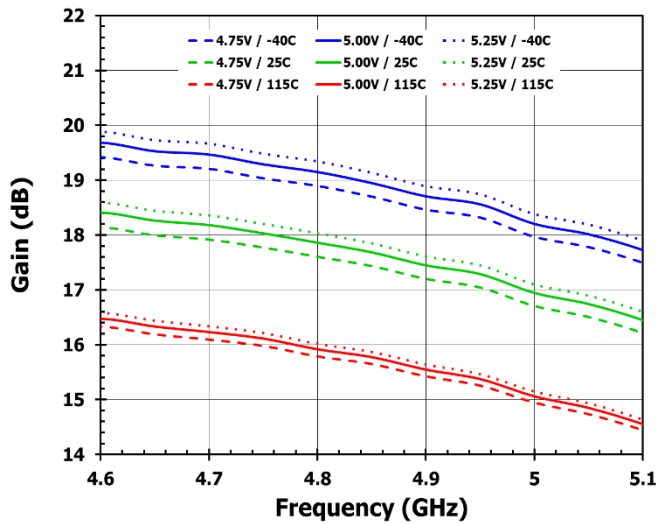


Figure 23. Gain 4.7 - 5.0GHz

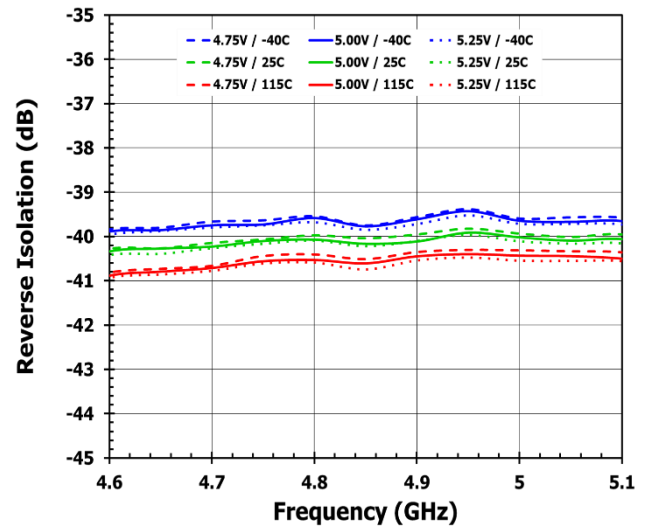


Figure 24. Reverse Isolation 4.7 - 5.0GHz

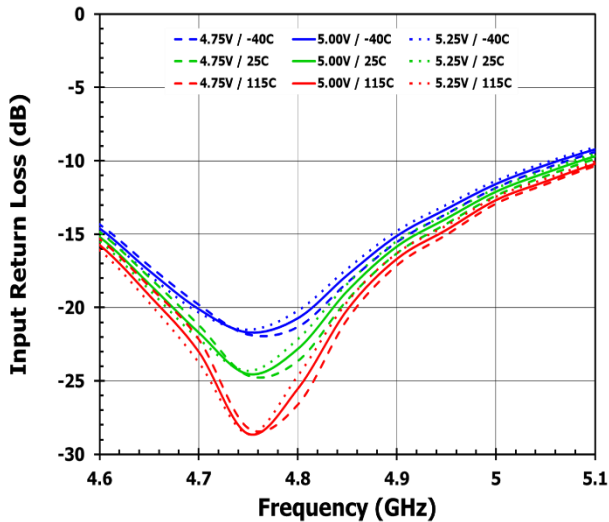


Figure 25. Input Return Loss 4.7 - 5.0GHz

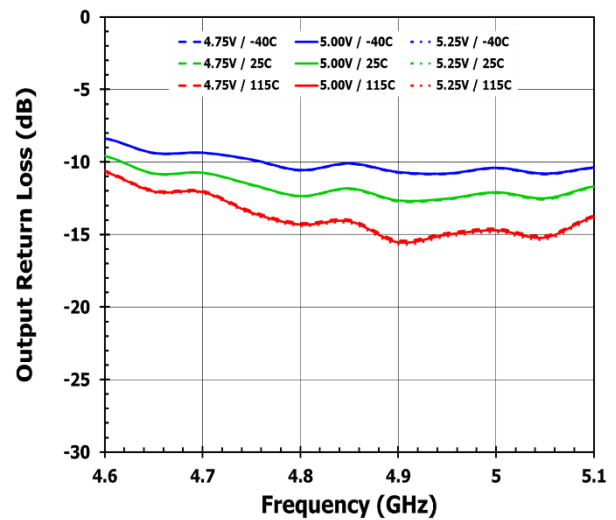


Figure 26. Output Return Loss 4.7 - 5.0GHz

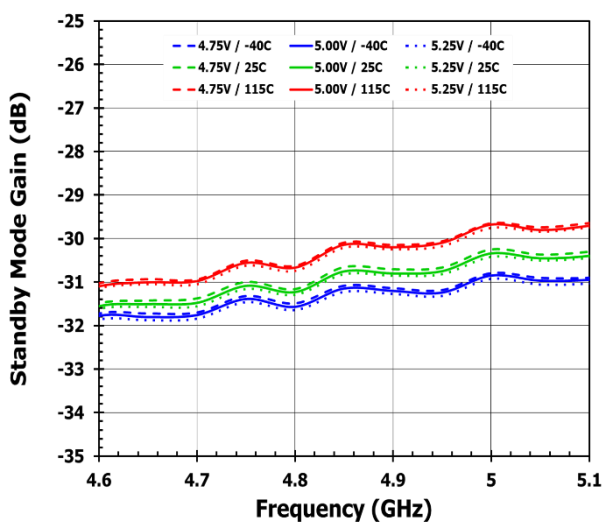


Figure 27. Standby Mode Gain 4.7 - 5.0GHz

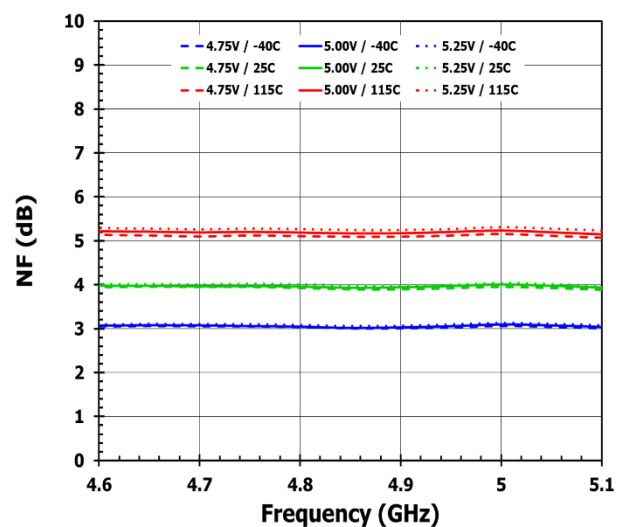


Figure 28. Noise Figure 4.7 - 5.0GHz

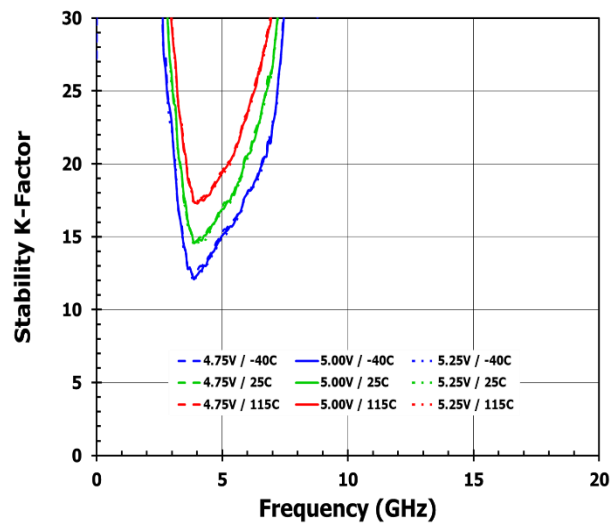


Figure 29. Stability K-Factor 4.7 - 5.0GHz

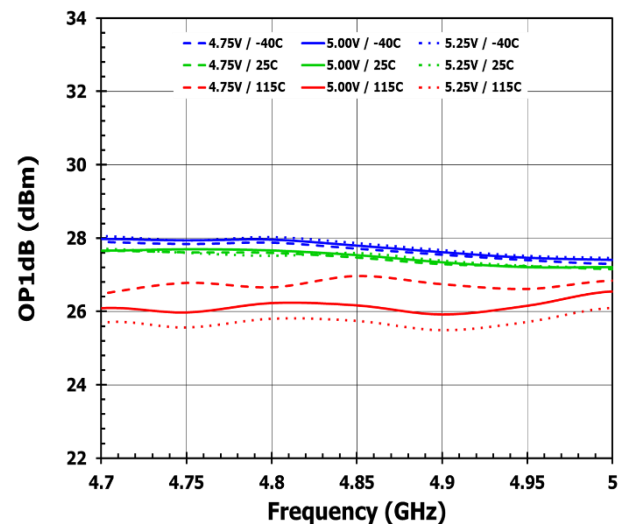


Figure 30. OP1dB 4.7 - 5.0GHz

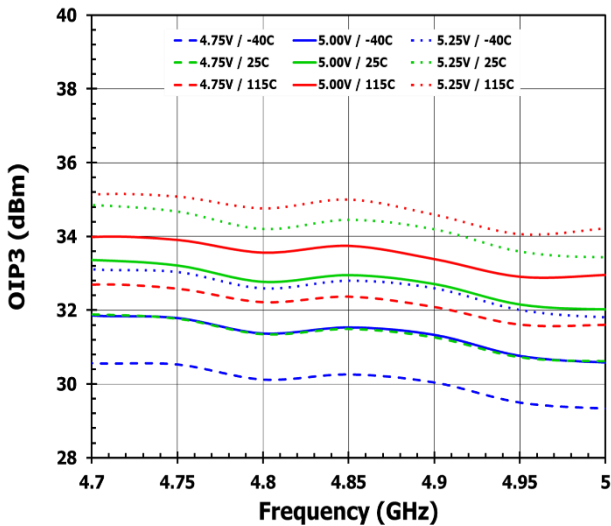


Figure 31. OIP3 4.7 - 5.0GHz $\Delta f = 20\text{MHz}$, $P_{\text{out}}/\text{Tone} = +5\text{dBm}$

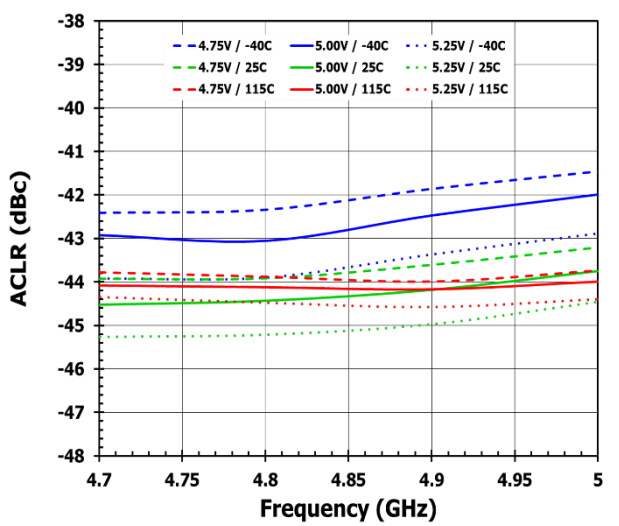


Figure 32. ACLR 4.7 - 5.0GHz LTE20MHz, $P_{\text{out}} = +15\text{dBm}$

Functional Information

The F1476 includes a STBY feature.

Table 1. STBY Truth Table

STBY	State
Logic HIGH or NC	Full Operation
Logic LOW	Amplifier OFF

Evaluation Board Information

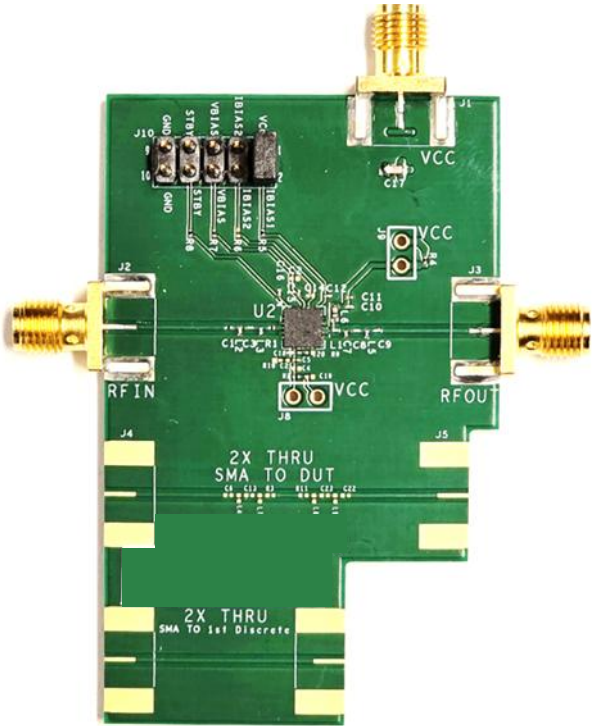


Figure 33. Evaluation Board – Top View

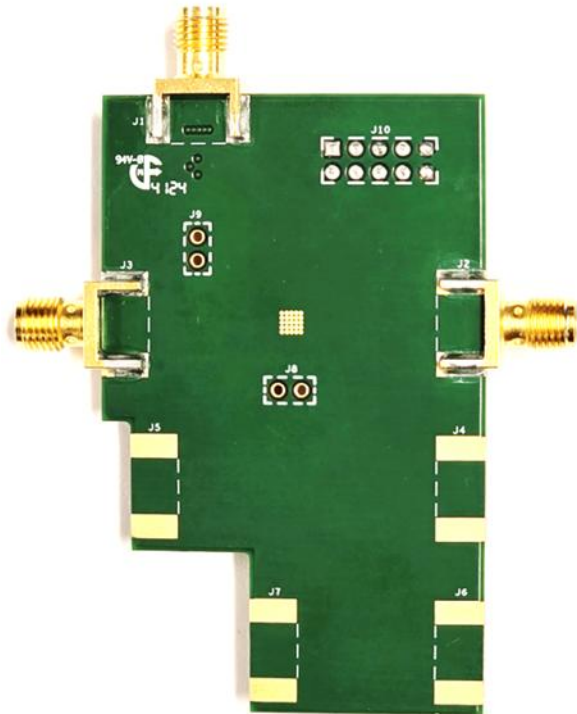


Figure 34. Evaluation Board – Bottom View

The schematic diagram illustrates the internal circuitry of the F147X EVB board. Key components include:

- Central IC:** F147108 (QFN20) with pins connected to VCC, GND, and various signal lines.
- Power Supply:** VCC and GND rails with decoupling capacitors (C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19).
- Resistors:** R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19.
- Inductors:** L1, L2.
- Connectors:** J1, J2, J3, J4.
- Header:** H1 (Headering 142) with pins connected to VCC and GND.

A note at the bottom right of the schematic states: "F147X_EVB_REV0".

Figure 35. Evaluation Board Schematic

Bill of Materials (BOM)

1.3.1. 3300MHz to 3800MHz

Part Reference	Qty	Description	Manufacturer Part No.	Manufacturer
R2, R4, R8, R5, C6, C13, R3, R11, C23, C22	10	0 Ohm, Chip Resistor, 1/10W (0201)	ERJ1GN0R00C	Panasonic
R1	1	6.04 Ohm, Chip Resistor, 1/20W (0201)	CRCW02016R04FXED	Vishay Dale
R7	1	160 Ohm, Chip Resistor, 1/20W (0201)	ERJ1GNF1600C	Panasonic
C1, L1	2	27pF, High-Q MLCC, 25V (0201)	GJM0335C1E270GB01	Murata
L3	1	0.6pF, High-Q MLCC, 50V (0201)	GJM0335C1HR60WB01	Murata
L5	1	1.9nH High-Q Inductor 450mA (0201)	LQP03TG1N9B02	Murata
L6	1	4.3nH High-Q Inductor 750mA (0402)	LQW15AN4N3B00	Murata
C3, C8	2	1.9pF, High-Q MLCC, 50V (0201)	GJM0335C1H1R9BB01	Murata
C7	1	1.7pF, High-Q MLCC, 50V (0201)	GJM0335C1H1R7BB01	Murata
C9	1	20pF, High-Q MLCC, 25V (0201)	GJM0335C1E200GB01	Murata

C10, C18	2	1000pF, MLCC 50V (0201)	GRM0335C1H102JE01	Murata
C11, C5	2	0.1uF, MLCC 25V (0201)	GRM033C81E104ME14	Murata
C12, C15, C16	3	100pF, MLCC 50V (0201)	GRM0335C1H101JA01	Murata
C17	1	4.7uF, MLCC 25V (0603)	GRM188C81E475KE11	Murata
C2, C14, C19, R6, C4, L2, L4, L7	8	DNP	-	-
J1, J2, J3, J4, J5, J6, J7	7	SMA Jack Str 50 Ohm Edge Mount, Fits 0.062" board	172-0701-801	Cinch Connectivity
J10	1	Vertical Header Strip 2x5, Male, 0.1" Pitch	-	Any Vendor
J8, J9	2	DNP	-	-
U2	1	F1476 Driver Amplifier	RA81F1476STG	Axiro Semiconductor

1.3.2. 3700MHz to 4000MHz

Part Reference	Qty	Description	Manufacturer Part No.	Manufacturer
R2, R3, R4, R8, R5, C1, C6, C13, R11, C23, C22	11	0 Ohm, Chip Resistor, 1/10W (0201)	ERJ1GN0R00C	Panasonic
R1	1	4.7 Ohm, Chip Resistor, 1/20W (0201)	CRCW02014R70FXED	Vishay Dale
R7	1	270 Ohm, Chip Resistor, 1/20W (0201)	ERJ1GNF2700C	Panasonic
L1	1	5.6pF, High-Q MLCC 50V (0201)	GJM0335C1H5R6BB01	Murata
L2	1	1pF, High-Q MLCC 50V (0201)	GJM0335C1H1R0BB01	Murata
L3	1	6.2nH, High-Q Inductor, 200mA (0201)	LQP03TG6N2H02	Murata
L5	1	2.3nH, High-Q Inductor, 450mA (0201)	LQP03TG2N3B02	Murata
L6	1	4.3nH, High-Q Inductor, 750mA (0402)	LQG15HS4N3B02	Murata
C3, C7	2	1.4pF, High-Q MLCC 50V (0201)	GJM0335C1H1R4BB01	Murata
C8	1	1pF, High-Q MLCC 50V (0201)	GJM0335C1H1R0BB01	Murata
C9	1	33pF, High-Q MLCC 25V (0201)	GJM0335C1E330G0B01	Murata
C10, C18	2	1000pF, MLCC 50V (0201)	GRM0335C1H102JE01	Murata
C11, C5	2	0.1uF, MLCC 25V (0201)	GRM033C81E104ME14	Murata
C12, C15, C16	3	100pF, MLCC 50V (0201)	GRM0335C1H101JA01	Murata
C17	1	4.7uF, MLCC 25V (0603)	GRM188C81E475KE11	Murata
C2, C14, C19, R6, C4, L4, L7	7	DNP	-	-
J1, J2, J3, J4, J5, J6, J7	7	SMA Jack Str 50 Ohm Edge Mount, Fits 0.062" board	172-0701-801	Cinch Connectivity
J10	1	Vertical Header Strip 2x5, Male, 0.1" Pitch	-	Any Vendor

J8, J9	2	DNP	-	-
U2	1	F1476 Driver Amplifier	RA81F1476STG	Axiro Semiconductor

1.3.3. 4700MHz to 5000MHz

Part Reference	Qty	Description	Manufacturer Part No.	Manufacturer
R1, R2, R3, R4, R8, R5, C1, C6, C13, R11, C23, C22	12	0 Ohm, Chip Resistor, 1/10W (0201)	ERJ1GN0R00C	Panasonic
R7	1	270 Ohm, Chip Resistor, 1/20W (0201)	ERJ1GNF2700C	Panasonic
L1	1	2.8pF, High-Q MLCC 50V (0201)	GJM0335C1H2R8BB01	Murata
L2	1	4.3nH, High-Q Inductor, 300mA (0201)	LQP03TG4N3H02	Murata
L3	1	0.2pF, High-Q MLCC 50V (0201)	GJM0335C1HR20WB01	Murata
L5	1	6.2nH, High-Q Inductor, 200mA (0201)	LQP03TG6N2H02	Murata
L6	1	3.3nH, High-Q Inductor, 800mA (0402)	LQG15HS3N3B02	Murata
C3	1	0.3pF, High-Q MLCC 50V (0201)	GJM0335C1HR30WB01	Murata
C7	1	0.5pF, High-Q MLCC 50V (0201)	GJM0335C1HR50WB01	Murata
C8	1	1.2pF, High-Q MLCC 50V (0201)	GJM0335C1H1R2BB01	Murata
C9	1	30pF, High-Q MLCC 25V (0201)	GJM0335C1E300GB01	Murata
C10, C18	1	1000pF, MLCC 50V (0201)	GRM0335C1H102JE01	Murata
C11, C5	1	0.1uF, MLCC 25V (0201)	GRM033C81E104ME14	Murata
C12, C15, C16	3	100pF, MLCC 50V (0201)	GRM0335C1H101JA01	Murata
C17	1	4.7uF, MLCC 25V (0603)	GRM188C81E475KE11	Murata
C2, C14, C19, R6, C4, L4, L7	8	DNP	-	-
J1, J2, J3, J4, J5, J6, J7	7	SMA Jack Str 50 Ohm Edge Mount, Fits 0.062" board	172-0701-801	Cinch Connectivity
J10	1	Vertical Header Strip 2x5, Male, 0.1" Pitch	-	Any Vendor
J8, J9	2	DNP	-	-
U2	1	F1476 Driver Amplifier	RA81F1476STG	Axiro Semiconductor

Package Outline Drawings

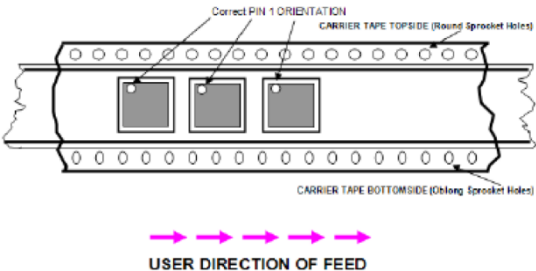
The package outline drawings are accessible from the Axiro website. The package information is the most current data available and is subject to change without revision of this document.

Marking Diagram

Top Marking Illustration	Marking	Representation
	RA81F1476STG	Manufacturer Part Number
	\$	Assembly Site Mark Code
	Y	Last Digit of the Year
	WW	Work Week
	***	Lot Sequential Code

Ordering Information

Part Number	Package Description	MSL Rating	Carrier Type	Temperature Range
RA81F1476STG NK#HD0	4.00 × 4.00 mm 20-VFQFPN	MSL1	Tape and Reel	-40°C to +115°C
RA81F1476STG NK#BD0	4.00 × 4.00 mm 20-VFQFPN	MSL1	Tray	
RTKA81F14763P600RU	Evaluation Board 3300MHz to 3800MHz tune			
RTKA81F14764P000RU	Evaluation Board 3700MHz to 4000MHz tune			
RTKA81F14764P600RU	Evaluation Board 4700MHz to 5000MHz tune			

Part Number Suffix	Pin 1 Orientation	Illustration
HD0	Quadrant 1(EIA-481-C)	

Revision History

Revision	Date	Description
2.00	Aug 4, 2026	▪ Updated document branding and layout to Axiro Semiconductor standard. No changes to device functionality or specifications.