F14292

1.7GHz to 2.7GHz 100Ω DIFF-In 50Ω SE-Out High-Gain, High-Linearity Driver Amplifier

The F14292 is a high-gain, high-linearity RF amplifier designed to operate within the 1.7GHz to 2.7GHz frequency range. Using a single 5V power supply, the F14292 provides 40dB of gain and 31dBm OP1dB at 2.6GHz.

The F14292 is packaged in a 4.0 × 4.0 mm, 24-VFQFPN package, with a differential 100Ω input and single-ended 50Ω output impedances for ease of integration into the signal path.

Applications

- 5G sub-6GHz massive MIMO
- Wireless infrastructure base stations
- FDD or TDD systems
- Point-to-point infrastructure
- Public safety infrastructure
- Military handhelds
- Repeaters and DAS
- General purpose RF

Features

- Frequency range: 1.7GHz to 2.7GHz
- 40dB typical gain at 2.6GHz
- 39dBm typical OIP3 at 2.6GHz
- 31dBm typical OP1dB at 2.6GHz
- 100Ω differential input and 50Ω singled-ended output impedances
- 5V power supply
- 305mA quiescent current consumption
- 1.8V logic compatible Standby Mode for power savings
- Operating temperature (T_{EPAD}) range: -40°C to +115°C
- 4.0 × 4.0 mm 24-VFQFPN package

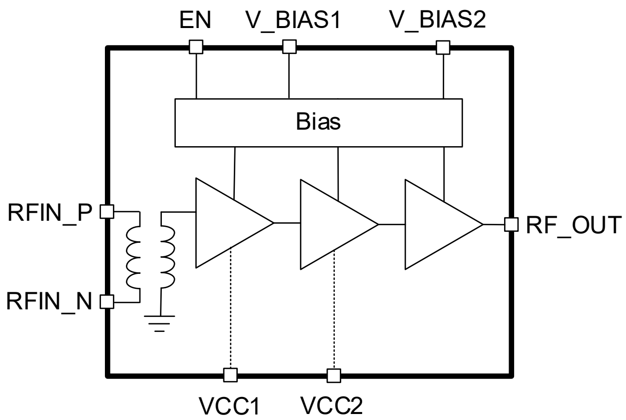

Figure 1. Block Diagram

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1. Pin Information

1.1 Pin Assignments

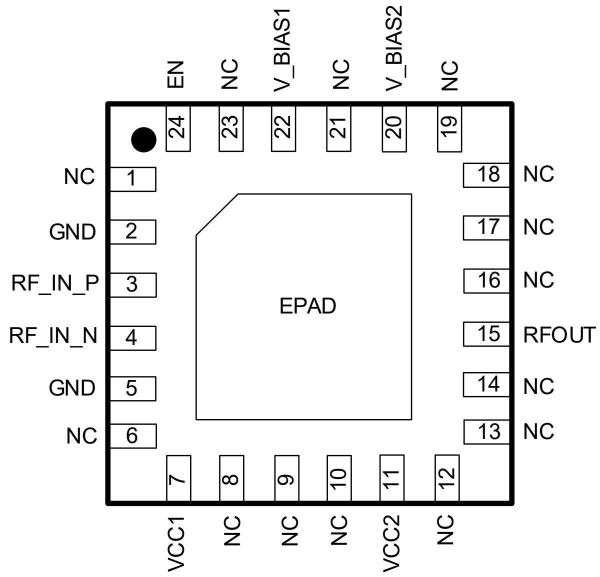


Figure 2. Pin Assignments – Top View

1.2 Pin Descriptions

Number	Name	Description
2, 5	GND	Internally grounded. This pin must be grounded with a via as close to the pin as possible.
1, 6, 8, 9, 10, 12, 13, 14, 16, 17, 18, 19, 21, 23	NC	Not connected inside the device. Recommend being grounded on the PCB board.
3	RFIN_P	RF input.
4	RFIN_N	RF input.
7	VCC1	Power supply. Use bypass capacitors as close to the pin as possible.
11	VCC2	Power supply. Use bypass capacitors as close to the pin as possible.
15	RF_OUT	RF output. Pull up to V_{CC} through inductor. Must use an external DC block.
20	V_BIAS2	Connect using a resistor to a common V_{CC} and use a bypass capacitor. Place network as close to the pin as possible. Proper VCC bypass capacitance is required for settling time performance. Please see application note below.
22	V_BIAS1	Connect using a resistor to a common ground and use a bypass capacitor. Place network as close to the pin as possible.
24	EN	Standby pin. With Logic LOW or no connect (NC) applied to this pin, the amplifier is powered off. With Logic HIGH applied to this pin, the part is in full operation mode. If standby functionality is not required, it is recommended that this pin be tied to logic HIGH.

Number	Name	Description
-	EPAD	Exposed Pad. Internally connected to ground. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the noted RF performance.

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Symbol	Minimum	Maximum	Unit
V_{CC1} to GND	V_{CC1}	-0.3	+6.0	V
V_{CC2} to GND	V_{CC2}	-0.3	+6.0	V
V_{BIAS1} to GND	V_{BIAS1}	-0.3	+6.0	V
V_{BIAS2} to GND	V_{BIAS2}	-0.3	+6.0	V
EN	V_{EN}	-0.3	5.25	V
RFIN externally applied DC voltage	V_{RFIN}	-0.5	+0.5	V
RFOUT externally applied DC voltage	V_{RFOUT}	-0.5	+8	V
Maximum CW Input Power applied for 24 hours. V_{CC} = 5V, Standby = logic HIGH: ON state.[1]	$P_{MAX\_IN\_ON}$	-	6	dBm
Junction Temperature	T_{JMAX}	-	175	°C
Storage Temperature Range	T_{st}	-65	150	°C
Lead Temperature (soldering, 10s)	-	-	260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}	-	1000	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)	V_{ESDCDM}	-	500	V

1. Exposure to these maximum RF levels can result in significantly higher I_{CC} current draw because of overdriving the amplifier stages.

2.2 Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power Supply Voltage	V_{CC}	-	4.75	5	5.25	V
Operating Temperature Range	T_{EPAD}	Exposed paddle	-40	-	+115	°C
RF Frequency Range	f_{RF}	-	1.7	-	2.7	GHz
RFIN Port Impedance	Z_{RFI}	Differential	-	100	-	Ω
RFOUT Port Impedance	Z_{RFO}	Single-ended	-	50	-	Ω

2.3 Electrical Specifications

2.3.1 General

Specifications apply when operated as a TX amplifier with tuning optimized for desired band of interest, $V_{CC} = V_{CC1} = V_{CC2} = V_{BIAS1} = V_{BIAS2} = +5.0V$, $T_{EPAD} = +25°C$, $Z_S = 100\Omega$ differential, $Z_L = 50\Omega$ single-ended, Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Logic Input High	V_{IH}	-	***1.17*** [1]	-	V_{CC}	V
Logic Input Low	V_{IL}	-	-0.3	-	***0.63***	V
Logic Current High	I_{IH}	EN pin. $V_{EN} = 5.25V$ ($V_{CC} = 5V$)	-	120	-	µA
Logic Current Low	I_{IL}	EN pin. $V_{EN} = -0.3V$ ($V_{CC} = 5V$)	-	-25	-	µA
Quiescent Current [2]	I_{CC}	-	-	305	-	mA
Power Dissipation	P_{DISS}	$V_{CC} = 4.75V$ to $5.25V$ $T_{EPAD} = -40°C$ to $+115°C$ Pout = 18dBm, 10% Pulsed CW	-	-	1975	mW
Standby Current	I_{CC_EN}	$V_{EN} = 0V$	-	8	-	mA
Standby Settling Time [3]	t_{SETTLE}	50% STBY control to RF output within 0.1dB and 1° of the on-state final value	-	-	1	µs
		50% STBY control to gain less than 5% of the on-state final gain value	-	-	1	

1. Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.
2. I_{CC} refers to the nominal small signal bias current.
3. Standby control signal has a rise/fall time of typically 5–10 ns and logic level of 0V to 1.8V.

2.3.2 2.3GHz to 2.7GHz

Specifications apply when operated as a TX amplifier with tuning optimized for the 2.3GHz to 2.7GHz band, $V_{CC} = V_{CC1} = V_{CC2} = V_{BIAS1} = V_{BIAS2}$ =+5.0V, f_{RF} = 2.6GHz, T_{EPAD} = +25°C, Z_S = 100Ω differential, Z_L = 50Ω single-ended, Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G1	f_{RF} = 2.6GHz V_{CC} = 5V T_{EPAD} = +25°C	***38*** [1]	40	-	dB
	G2	f_{RF} = 2.3GHz to 2.7GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	35.5	-	43	dB
Gain Flatness Max minus min gain within the frequency window	G_{FLAT-1}	f_{RF} = 2.3GHz to 2.7GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	-	0.55	-	dB
	G_{FLAT-2}	f_{RF} = 2.2GHz to 2.8GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	-	0.75	-	dB
Phase Ripple Deviation Largest phase deviation from linear phase within the frequency window. Linear phase based on frequency window center.	$Phase_{ripple1}$	f_{RF} = 2.3GHz to 2.7GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	-	2	-	Deg
	$Phase_{ripple2}$	f_{RF} = 2.2GHz to 2.8GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	-	3.5	-	Deg
STBY Mode Gain	G_{STBY}	EN pin. V_{EN} = 0V, P_{IN} ≤ +5dBm	-	-	-40	dB
Reverse Isolation	ISO_{REV}	f_{RF} = 2.3GHz to 2.7GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	50	-	-	dB
RF Input Return Loss	RL_{RFIN}	f_{RF} = 2.3GHz to 2.7GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	10	-	-	dB
RF Output Return Loss	RL_{RFOUT}	f_{RF} = 2.2GHz to 2.8GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	10	-	-	dB
Noise Figure	NF	f_{RF} = 2.3GHz to 2.7GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = +115°C	-	-	6.6	dB
Noise Figure at Cold	NF_{COLD}	f_{RF} = 2.3GHz to 2.7GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C	-	-	4.1	dB

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Output Third Order Intercept Point	$OIP3_1$	Δf = 1MHz Pout = OP1dB -10dBm f_{RF} = 2.3GHz to 2.7GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	35	38	-	dBm
	$OIP3_2$	Δf = 100MHz Pout = OP1dB -10dBm f_{RF} = 2.3GHz to 2.7GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	32	34	-	dBm
Output 1dB Compression Point Pulsed CW 10% Duty Cycle	OP1dB	f_{RF} = 2.3GHz to 2.7GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	29	31	-	dBm
ACLR	ACLR	20MHz E-TM1.1 signal Pout = 18dBm f_{RF} = 2.3GHz to 2.7GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	-	-	-45	dBc
CMRR	CMRR	f_{RF} = 2.3GHz to 2.7GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	25	-	-	dB
Stability	K_{factor}	f_{RF} = 10MHz to 20GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	1	-	-	-

1. Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.

2.3.3 1.7GHz to 2.2GHz

Specifications apply when operated as a TX amplifier with tuning optimized for the 1.7GHz to 2.2GHz band, $V_{CC} = V_{CC1} = V_{CC2} = V_{BIAS1} = V_{BIAS2}$ =+5.0V, f_{RF} = 2.0GHz, T_{EPAD} = +25°C, Z_S = 100Ω differential, Z_L = 50Ω single-ended, Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G1	f_{RF} = 2.0GHz V_{CC} = 5V T_{EPAD} = +25°C	38.5	40.5	-	dB
	G2	f_{RF} = 1.7GHz to 2.2GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	35.5	-	45	dB
Gain Flatness Max minus min gain within the frequency window	G_{FLAT-1}	f_{RF} = 1.7GHz to 2.2GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	-	2.5	-	dB
	G_{FLAT-2}	f_{RF} = 1.6GHz to 2.3GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	-	6.0	-	dB
Phase Ripple Deviation Largest phase deviation from linear phase within the frequency window. Linear phase based on frequency window center.	$Phase_{ripple1}$	f_{RF} = 1.7GHz to 2.2GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	-	12	-	Deg
	$Phase_{ripple2}$	f_{RF} = 1.6GHz to 2.3GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	-	12	-	Deg
STBY Mode Gain	G_{STBY}	EN pin. V_{EN} = 0V, P_{IN} ≤ +5dBm	-	-	-40	dB
Reverse Isolation	ISO_{REV}	f_{RF} = 1.7GHz to 2.2GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	50	-	-	dB
RF Input Return Loss	RL_{RFIN}	f_{RF} = 1.7GHz to 2.2GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = +115°C	10	-	-	dB
RF Output Return Loss	RL_{RFOUT}	f_{RF} = 1.7GHz to 2.2GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = +115°C	10	-	-	dB
Noise Figure	NF	f_{RF} = 1.8GHz to 2.2GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = +115°C	-	-	7.4	dB
Noise Figure at Cold	NF_{COLD}	f_{RF} = 1.8GHz to 2.2GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C	-	-	5.0	dB

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Output Third Order Intercept Point	$OIP3_1$	Δf = 1MHz Pout = OP1dB -10dBm f_{RF} = 1.8GHz to 2.2GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	36	41	-	dBm
	$OIP3_2$	Δf = 100MHz Pout = OP1dB -10dBm f_{RF} = 1.8GHz to 2.2GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	34	39	-	dBm
Output 1dB Compression Point Pulsed CW 10% Duty Cycle	OP1dB	f_{RF} = 1.8GHz to 2.2GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	27	30	-	dBm
ACLR	ACLR	20MHz E-TM1.1 signal Pout = 18dBm f_{RF} = 1.8GHz to 2.2GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	-	-	-45	dBc
CMRR	CMRR	f_{RF} = 1.7GHz to 2.2GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	25	-	-	dB
Stability	K_{factor}	f_{RF} = 10MHz to 20GHz V_{CC} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	1	-	-	-

2. Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.

2.4 Thermal Specifications

Parameter	Symbol	Condition	Typical Value	Unit
Thermal Resistance	θ_{JA}	Junction to ambient	57.8	°C/W
	θ_{JC}	Junction to case (case is defined as the exposed paddle)	16.2	
Moisture Sensitivity Rating (Per J-STD-020)			MSL1	-

3. Typical Performance Graphs

Unless otherwise stated the typical operating graphs were measured under the following conditions:

- V_{CC} = 5.0V
- V_{EN} = High
- T_{EPAD} = +25°C
- Z_S = 100Ω differential, Z_L = 50Ω single-ended
- Pout = 23dBm/tone and 1MHz/100MHz tone spacing for OIP3

3.1 2300MHz to 2700MHz Performance

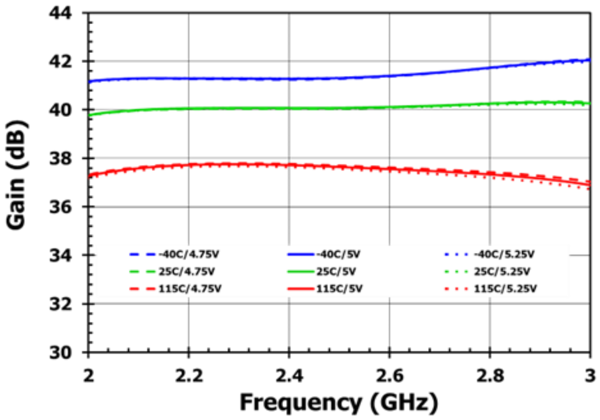


Figure 3. Gain

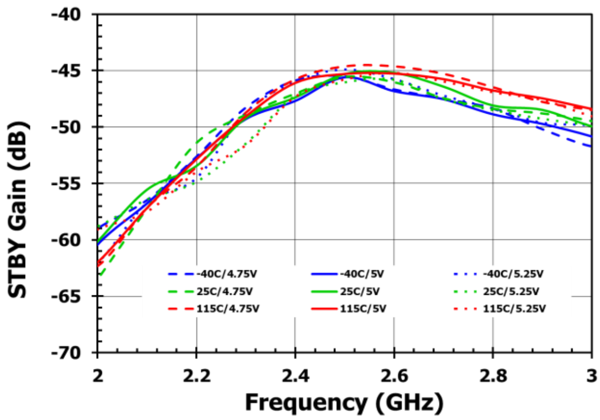


Figure 4. Standby Mode Gain

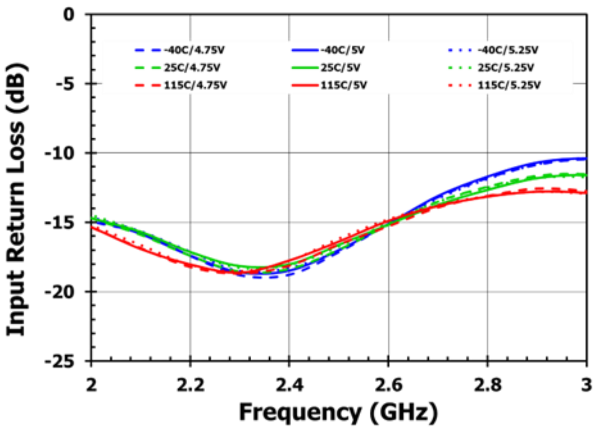


Figure 5. Input Return Loss

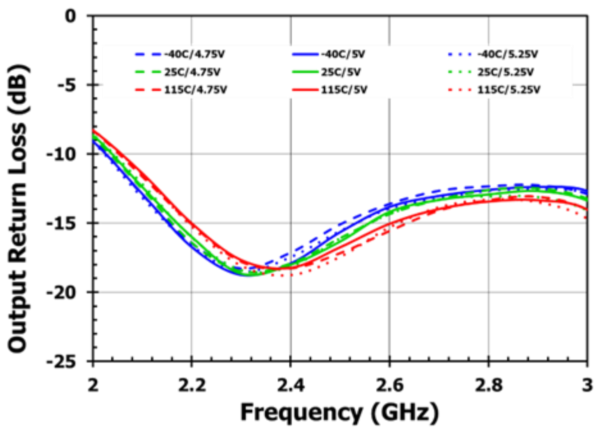


Figure 6. Output Return Loss

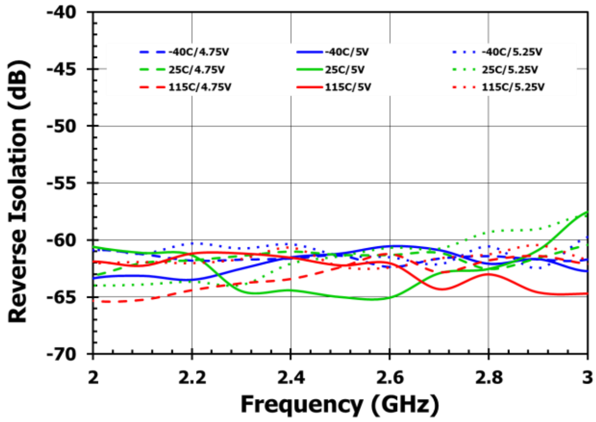


Figure 7. Reverse Isolation

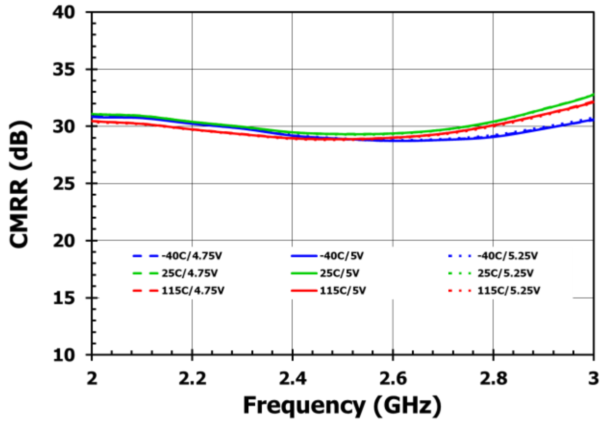


Figure 8. CMRR

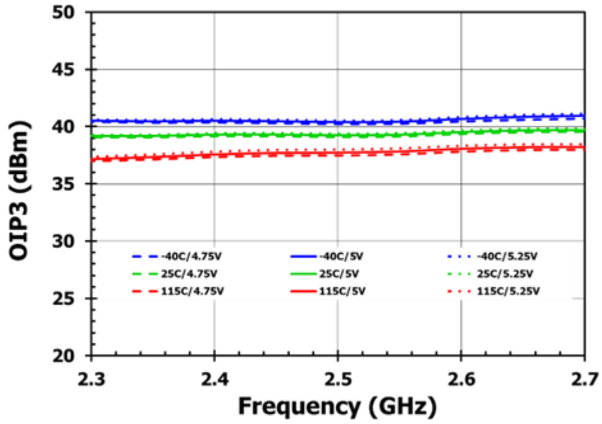


Figure 9. OIP3 (1MHz Tone Spacing)

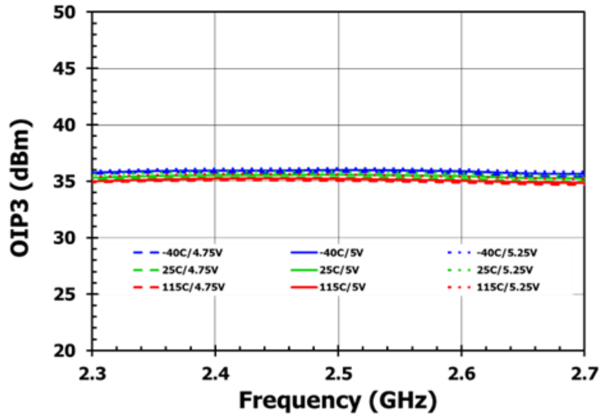


Figure 10. OIP3 (100MHz Tone Spacing)

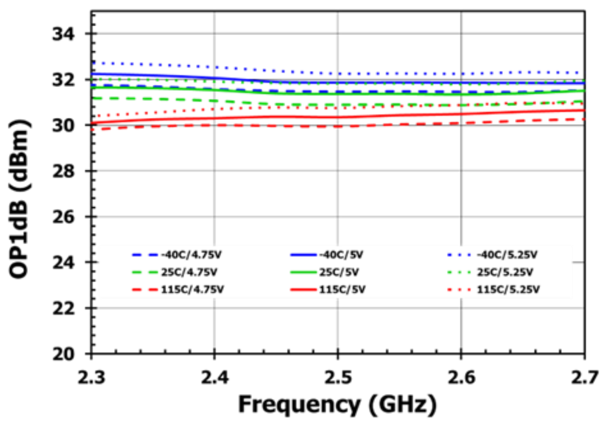


Figure 11. OP1dB

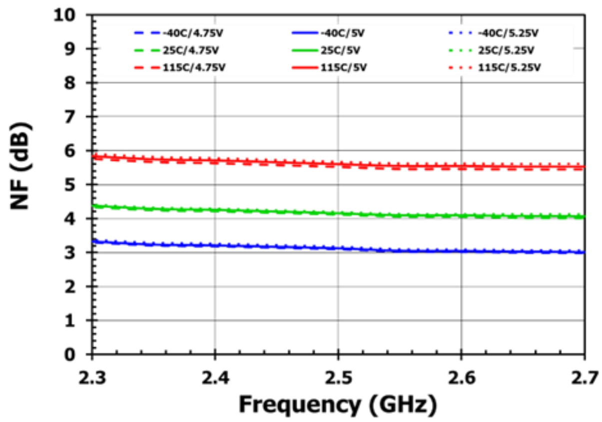


Figure 12. Noise Figure

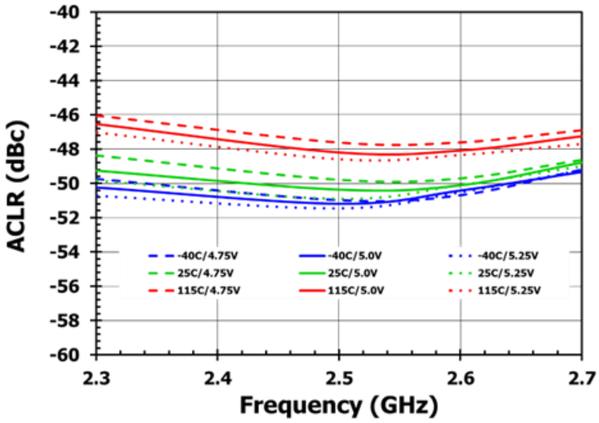


Figure 13. ACLR

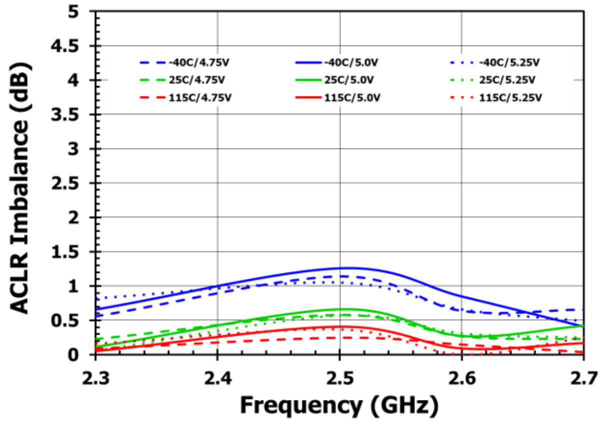


Figure 14. ACLR Imbalance

3.2 1800MHz to 2200MHz Performance

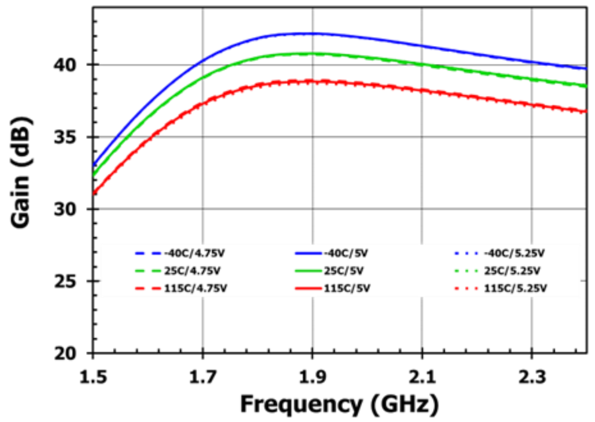


Figure 15. Gain

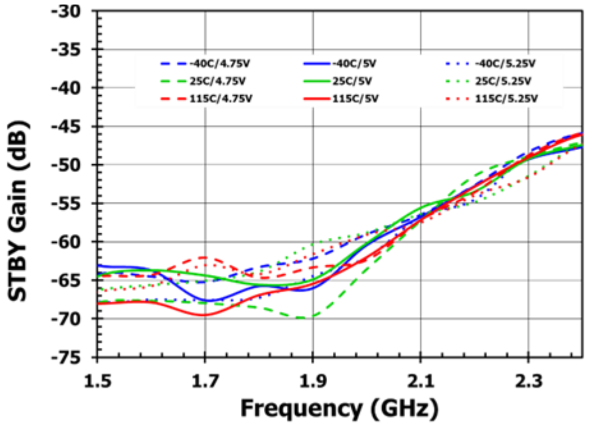


Figure 16. Standby Mode Gain

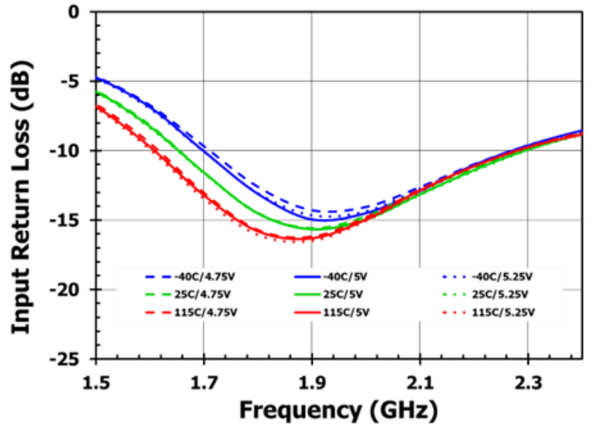


Figure 17. Input Return Loss

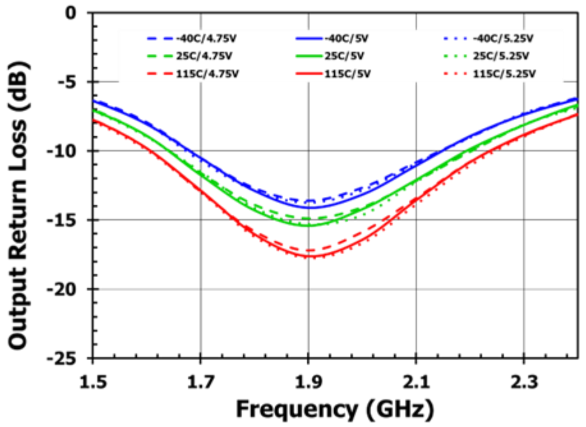


Figure 18. Output Return Loss

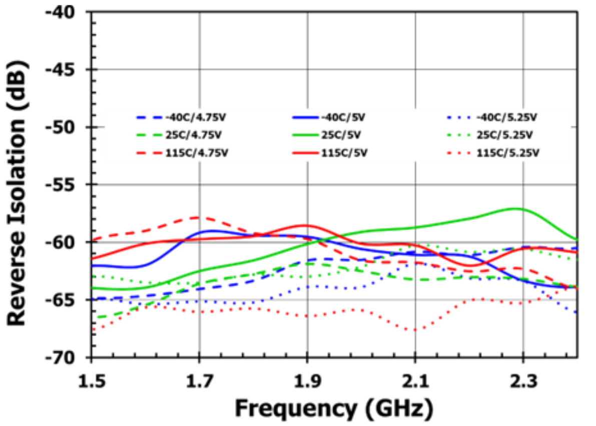


Figure 19. Reverse Isolation

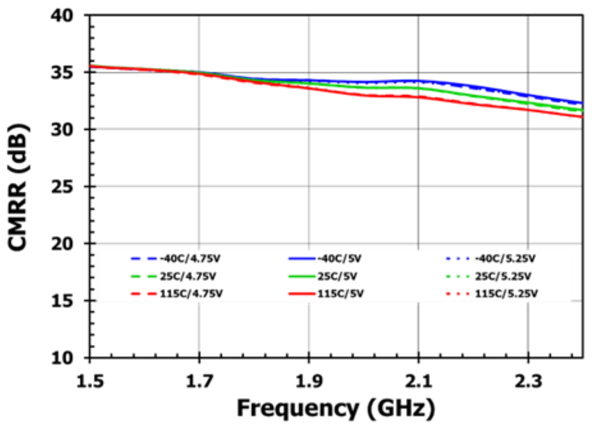


Figure 20. CMRR

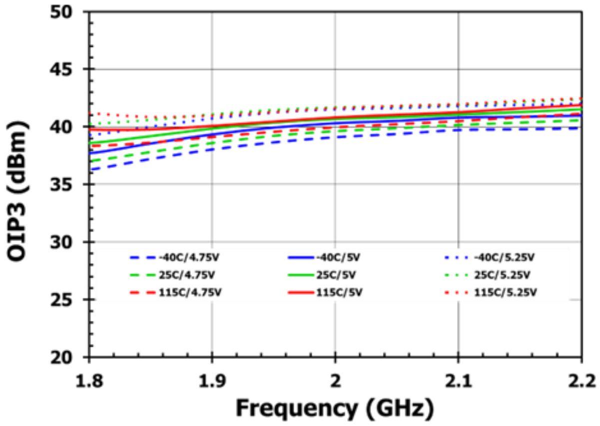


Figure 21. OIP3 (1MHz Tone Spacing)

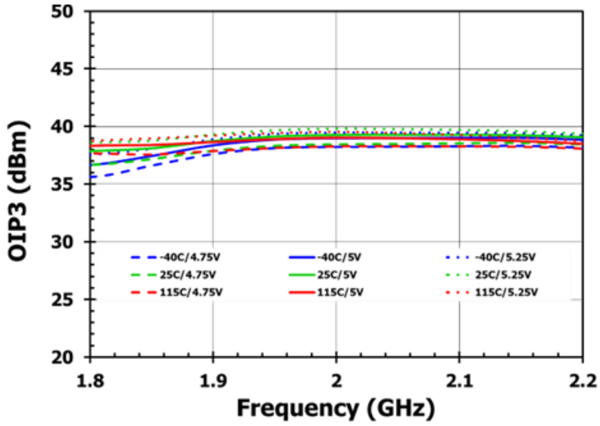


Figure 22. OIP3 (100MHz Tone Spacing)

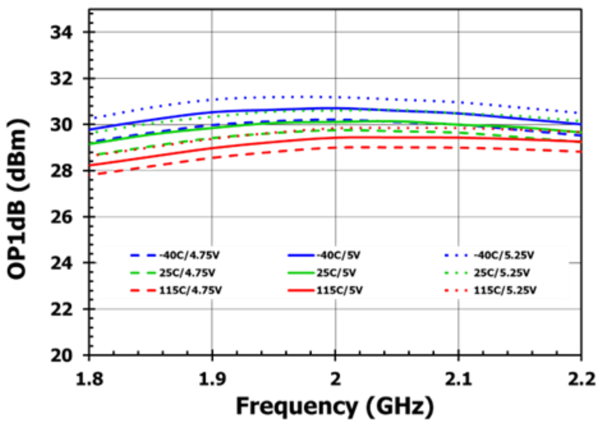


Figure 23. OP1dB

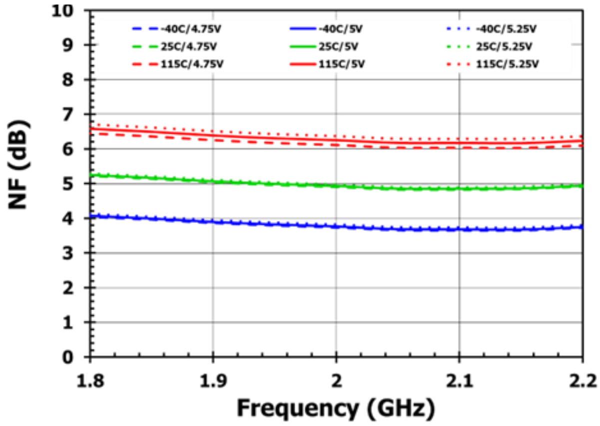


Figure 24. Noise Figure

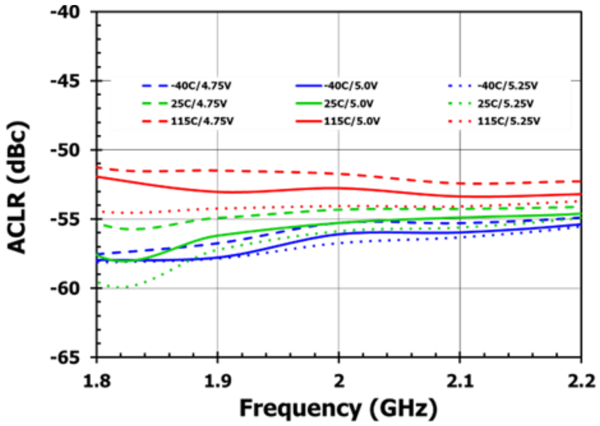


Figure 25. ACLR (LTE 20MHz)

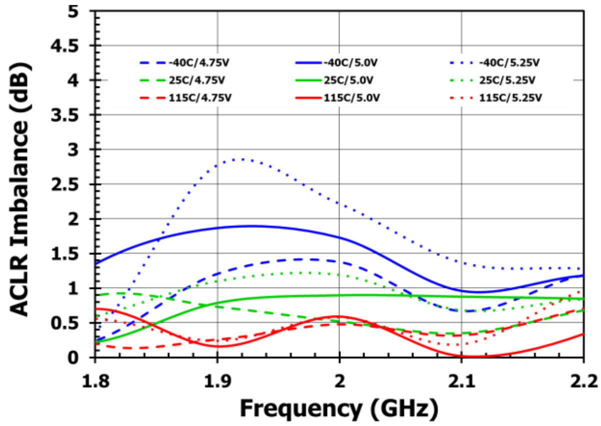


Figure 26. ACLR Imbalance

4. Functional Description

4.1 ENABLE

The F14292 can be turned off for low current consumption. This is done by applying a logic voltage to the EN pin (pin 24) using Table 1.

Table 1. ENABLE Truth Table

EN	Condition
Logic HIGH	Full operation
Logic LOW / NC	Amplifier OFF

5. Evaluation Board (EVB) Information

5.1 Evaluation Board (Front)

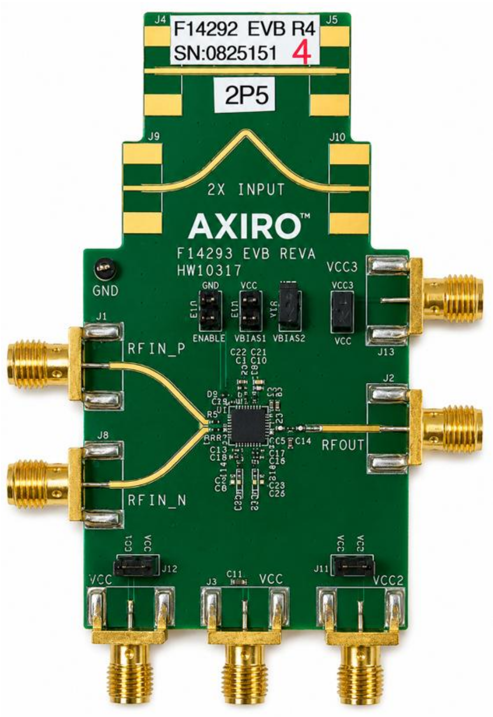


Figure 27. Evaluation Board (Front)

5.2 Evaluation Board (Back)

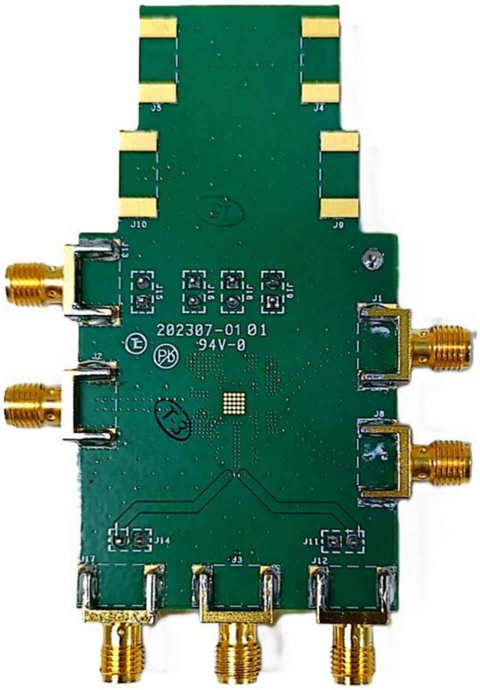


Figure 28. Evaluation Board (Back)

5.3 Evaluation Board Schematic

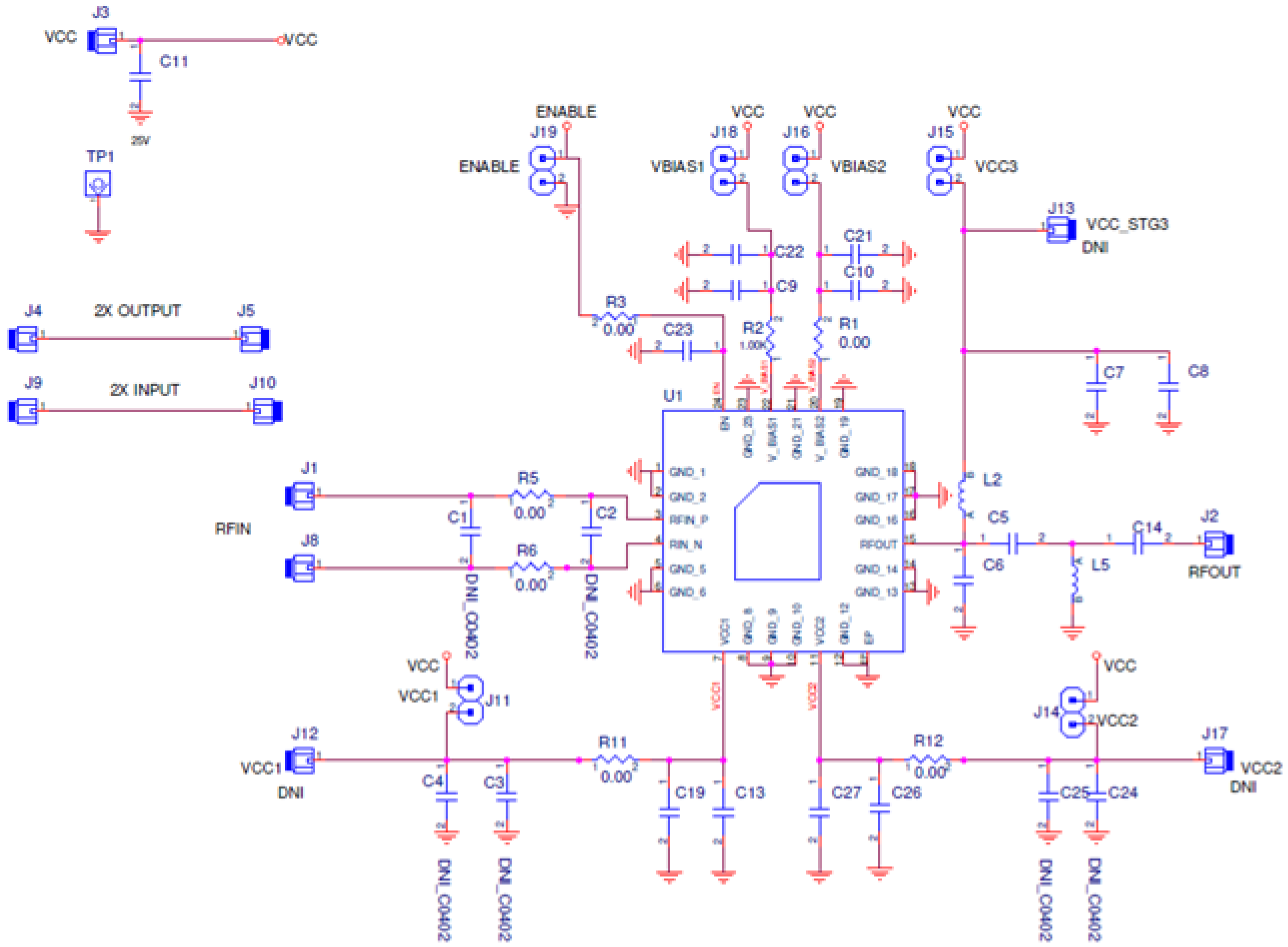


Figure 29. Evaluation Board Circuit Schematic

5.4 Bill of Materials

Table 2. Evaluation Board Bill of Material (BOM) – 2.3GHz to 2.7GHz

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C1, C2, C3, C4, C23, C24, C25	7	DNI	-	-
C5	1	1.7pF ± 0.1pF, 50V, C0G Surface Mount Capacitor (0402)	GJM1555C1H1R7BB01D	Murata Electronics
C6	1	2.7pF ± 0.1pF, 50V, C0G Surface Mount Capacitor (0402)	GJM1555C1H2R7BB01D	Murata Electronics
C7	1	33pF ± 2%, 50V, C0G Surface Mount Capacitor (0402)	GJM1555C1H330GB01D	Murata Electronics
C8, C19, C27	3	0.1uF ± 10%, 50V, X7R Surface Mount Capacitor (0402)	GRM155R71H104KE14D	Murata Electronics
C9	1	0Ω Surface Mount Resistor (0402)	ERJ-2GE0R00X	Panasonic
C10, C22	2	1000pF ± 5%, 25V, C0G Surface Mount Capacitor (0402)	GRM1555C1E102JA01D	Murata Electronics
C11	1	47uF ± 20%, 6.3V, X5R Surface Mount Capacitor (0603)	GRM188R60J476ME15D	Murata Electronics
C13	1	2.0pF ± 0.1pF, 50V, C0G Surface Mount Capacitor (0402)	GJM1555C1H2R0BB01D	Murata Electronics
C14	1	6.6pF ± 0.1pF, 50V, C0G Surface Mount Capacitor (0402)	GJM1555C1H6R6BB01D	Murata Electronics
C21	1	10uF ± 20%, 6.3V, X5R Surface Mount Capacitor (0402)	GRM155R60J106ME44D	Murata Electronics
C26	1	1uF ± 20%, 6.3V, X7R Surface Mount Capacitor (0402)	GRM155R70J105MA12D	Murata Electronics
J1, J2, J3, J4, J5, J8, J9, J10, J12, J13, J17	11	SMA Connector Jack, Female 50 Ohms Board Edge	142_0701_851	Cinch
J11, J14, J15, J16	4	Header 1x2	22-28-4023	Molex
J18, J19	2	DNI	-	-
L2	1	8.2nH Surface Mount Inductor (0402)	LQG15HS8N2G02D	Murata Electronics
L5	1	2.0nH Surface Mount Inductor (0402)	LQG15HS2N0B02D	Murata Electronics
R1, R2, R3, R5, R6, R11, R12	7	0Ω Surface Mount Resistor (0402)	ERJ-2GE0R00X	Panasonic
TP1	1	Test Point Loop	5001	Keystone
U1	1	1.7GHz to 2.7GHz 100Ω DIFF-In 50Ω SE-Out High-Gain, High-Linearity Driver Amplifier	F14292	Axiro

Table 3. Evaluation Board Bill of Material (BOM) – 1.7GHz to 2.2GHz

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C1, C4, C19, C23, C24, C25	6	DNI	-	-
C2	1	0.6pF ± 0.1pF, 50V, C0G Surface Mount Capacitor (0402)	GJM1555C1HR60BB01D	Murata Electronics
C3	1	0.1uF ± 10%, 50V, X7R Surface Mount Capacitor (0402)	GRM155R71H104KE14D	Murata Electronics
C5	1	1.0nH Surface Mount Inductor (0402)	LQG15HS1N0B02D	Murata Electronics
C6	1	3.3pF ± 0.1pF, 50V, C0G Surface Mount Capacitor (0402)	GJM1555C1H3R3BB01D	Murata Electronics
C7	1	33pF ± 2%, 50V, C0G Surface Mount Capacitor (0402)	GJM1555C1H330GB01D	Murata Electronics
C8, C27	2	0.1uF ± 10%, 50V, X7R Surface Mount Capacitor (0402)	GRM155R71H104KE14D	Murata Electronics
C9	1	0Ω Surface Mount Resistor (0402)	ERJ-2GE0R00X	Panasonic
C10, C22	2	1000pF ± 5%, 25V, C0G Surface Mount Capacitor (0402)	GRM1555C1E102JA01D	Murata Electronics
C11	1	47uF ± 20%, 6.3V, X5R Surface Mount Capacitor (0603)	GRM188R60J476ME15D	Murata Electronics
C13	1	DNI	-	-
C14	1	10pF ± 5%, 50V, C0G Surface Mount Capacitor (0402)	GJM1555C1H100JB01D	Murata Electronics
C21	1	10uF ± 20%, 6.3V, X5R Surface Mount Capacitor (0402)	GRM155R60J106ME44D	Murata Electronics
C26	1	1uF ± 20%, 6.3V, X7R Surface Mount Capacitor (0402)	GRM155R70J105MA12D	Murata Electronics
J1, J2, J3, J4, J5, J8, J9, J10, J12, J13, J17	11	SMA Connector Jack, Female 50 Ohms Board Edge	142_0701_851	Cinch
J11, J14, J15, J16	4	Header 1x2	22-28-4023	Molex
J18, J19	2	DNI	-	-
L2	1	3.9nH Surface Mount Inductor (0402)	LQH15HS3N9B02D	Murata Electronics
L5	1	2.2pF ± 0.1pF, 50V, C0G Surface Mount Capacitor (0402)	GJM1555C1H2R2BB01D	Murata Electronics
R1, R2, R3, R5, R6, R12	6	0Ω Surface Mount Resistor (0402)	ERJ-2GE0R00X	Panasonic
R11	1	47nH Surface Mount Inductor (0402)	LQG15HS47NG02D	Murata Electronics
TP1	1	Test Point Loop	5001	Keystone
U1	1	1.7GHz to 2.7GHz 100Ω DIFF-In 50Ω SE-Out High-Gain, High-Linearity Driver Amplifier	F14292	Axiro

6. Application Information

6.1 Application Circuit Schematic

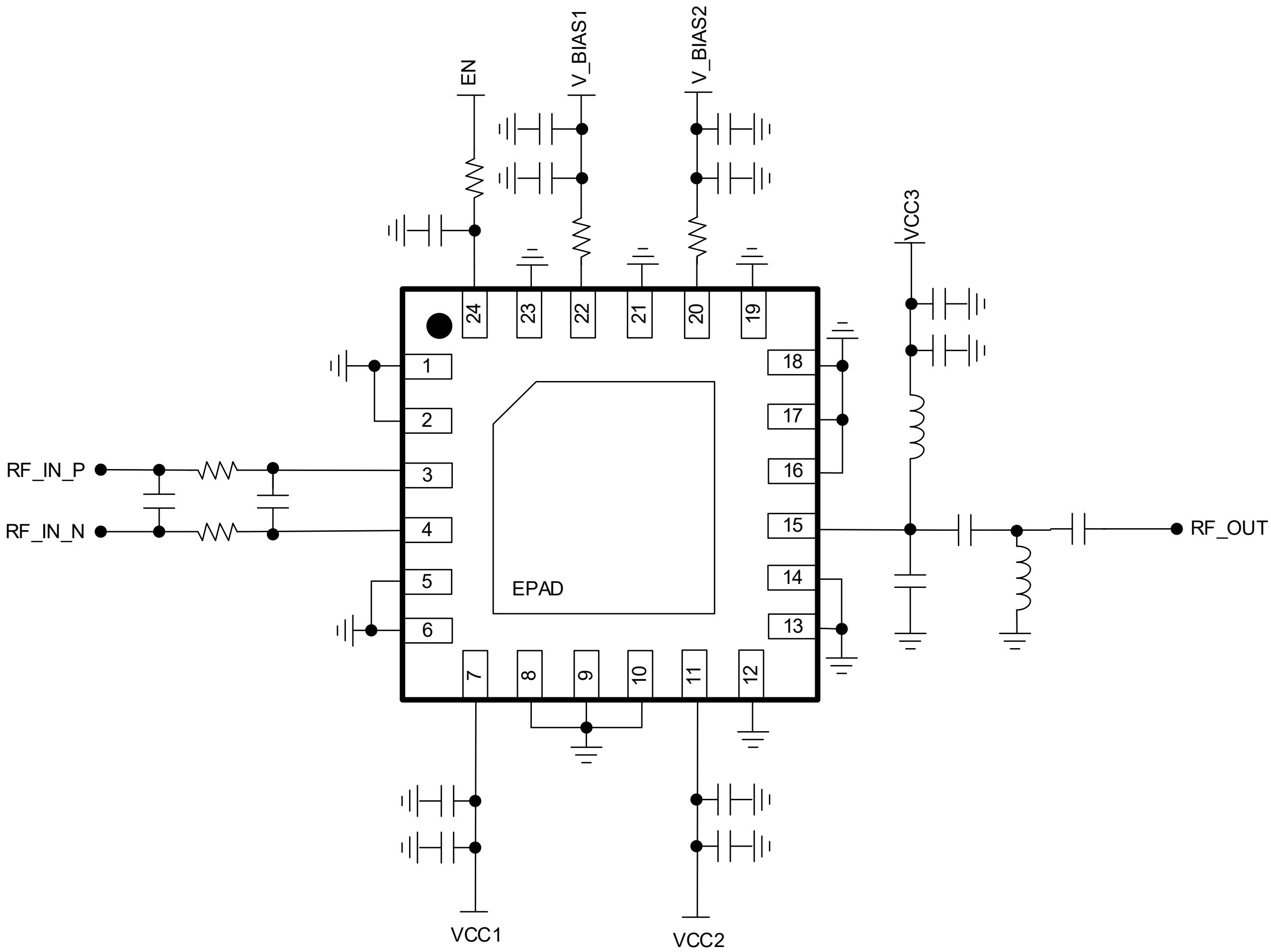


Figure 30. Application Circuit Schematic

6.2 Settling Time

Proper voltage supply bypass capacitance is required to achieve the settling time performance. Ensure that sufficient bypass capacitance is provided on the VCC supply (Ex. 47uF for C11) and specifically that C10 and C21 on pin VBIAS2 (Pin 20) is as close to the device as possible and of sufficient capacitance (Ex. 10uF for C21)

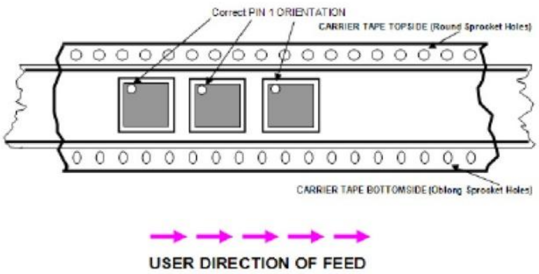
7. Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without revision of this document.

8. Ordering Information

Part Number	Package Description	MSL Rating	Carrier Type	Temperature Range
RRF14292-B00	4.0 × 4.0 mm 24-VFQFPN	1	Tray	-40°C to +115°C
RRF14292-H00	4.0 × 4.0 mm 24-VFQFPN	1	Reel	-40°C to +115°C
RTKRF14292-2P0	Evaluation Board (1.7-2.2GHz)			
RTKRF14292-2P5	Evaluation Board (2.3-2.7GHz)			

Table 4. Pin 1 Orientation in Tape and Reel Packaging

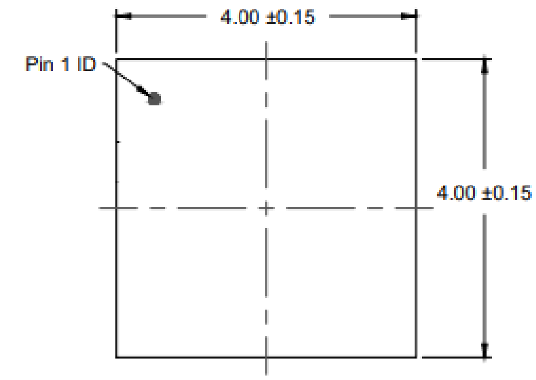
Part Number Suffix	Pin 1 Orientation	Illustration
H00	Quadrant 1 (EIA-481-C)	

9. Revision History

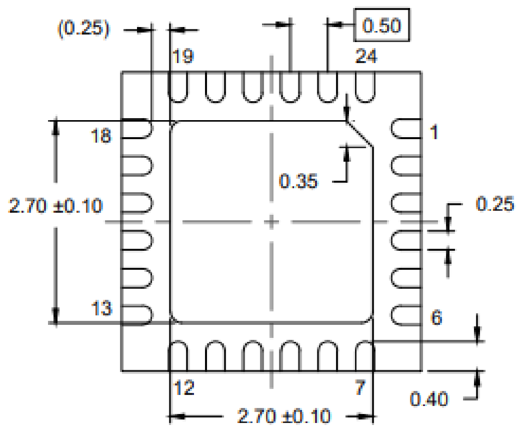
Revision	Date	Description
2.00	Jun 25, 2026	Updated document branding and layout to Axiro Semiconductor standard. No changes to device functionality or specifications.

Package Outline Drawing

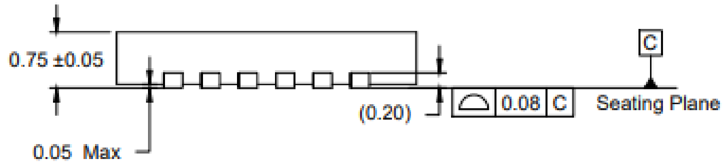
Package Code:NBG24P3
24-VFQFPN 4.0 x 4.0 x 0.75 mm Body, 0.50 mm Pitch
PSC-4313-03, Revision: 02, Date Created: Jul 20, 2023



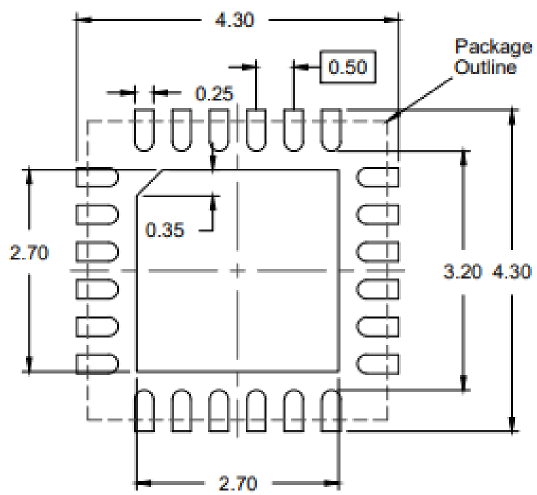
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.