AX110

Automotive Applications Processor

Overview

The AX110 processor is a high-performance automotive applications processor designed to help OEMs and Tier 1s build next-generation eCockpit systems with advanced compute, graphics, AI, multimedia, and functional safety in a single device.

It combines a powerful heterogeneous processing architecture with 6x ARM Cortex-A55 CPUs in the primary application cluster, 1x additional ARM Cortex-A55 CPU in a secondary cluster, an IMG PowerVR 9XM GPU, and a dedicated AI accelerator to support the growing performance demands of intelligent cockpit platforms, rich human-machine interfaces, and immersive in-vehicle user experiences.

To enable flexible and cost-effective system integration, AX110 also incorporates a broad range of high-speed and automotive interfaces, including PCIe 3.0, USB 3.0, Gigabit Ethernet TSN, CAN-FD, MIPI CSI, MIPI DSI, LVDS, eMMC, SD/SDIO, QuadSPI/OctalSPI, SPI, UART, and I^2C.

For safety-critical functions, AX110 integrates a dedicated on-chip safety island based on Cortex-R5F cores operating in dual-core lock-step mode, along with a separate RTC and system control domain for low-power operation, reset and power management, and secure storage.

With its multi-domain architecture, high-performance application processing, rich multimedia support, and integrated safety capability, AX110 provides a scalable and practical foundation for modern digital cockpit designs.

Target Applications

AX110 processor is targeted for the following applications:

- eCockpit
- Virtual Cluster
- Infotainment

Key Features

AX110 processor consists of three independent functional domains:

- Applications Processing Domain
- Highly Reliable Safety Domain
- Low Power RTC and Safety Control Domain

Applications Processing Domain

CPU1

- 6x ARM Cortex-A55 CPU, 2.0GHz
- 32KB/32KB L1 I/D-Cache per core
- 128KB L2 Cache per core
- 1MB L3 Cache

CPU2

- ARM Cortex-A55 CPU, 1.4GHz
- 32KB/32KB L1 I/D-Cache
- 128KB L2 Cache

Secure Processor

- ARM Cortex-R5 in DCLS mode
- 32KB/32KB L1 I/D-Cache
- 128KB TCM

Multi-Purpose Processor

- ARM Cortex-R5 in DCLS mode
- 32KB/32KB L1 I/D-Cache
- 128KB TCM

AI Accelerator

- High efficiency accelerator for AI
- Support TensorFlow/Caffe framework

ADC

- 12-bit SAR ADC, 5M Samples/s
- 4 Analog Input Channels

Audio Interface

- 4x SPDIF
- 6x single-channel I2S/TDM
- 2x multi-channel I2S

Camera Interface

- 2x 4-lane MIPI-CSI Interface, support 4 virtual channels
- 1x 8-bit Parallel CSI Interface

Display Interface

- 2x 4-lane MIPI-DSI Interface
- 4x LVDS Display Interface

GPU Core

- IMG PowerVR 9XM GPU

Internal Memory

- 768K System RAM

DRAM Interfaces

- 32-bit DRAM Interface, 4267MT/s
- Support LPDDR4/LPDDR4x
- Support DDR4
- Optional In-line ECC

VPU Cores

- H.264 Video Encoder/Decoder
- H.265/VP8/VP9 Video Decoder

High-Speed Interfaces

- 2x USB3.0
- 2x PCIe3.0 RC/EP Dual Role

Storage Interface

- 2x eMMC5.1
- 2x SD3.0/SDIO
- 1x QuadSPI/OctalSPI

Peripherals

- 1x Giga-bit Ethernet TSN
- 4x SPI
- 8x UART
- 12x I2C
- GPIO
- PWM
- Watchdog
- Timer

Highly Reliable Safety Domain

Safety CPU Core

- ARM Cortex-R5F 800MHz in DCLS mode
- 32KB/32KB L1 I/D-Cache
- 128KB TCM

Storage Interface

- 1x QuadSPI/OctalSPI

Audio Interface

- 2x Single-Channel I2S/TDM

Internal Memory

- 256KB System RAM
- 128KB ROM
- All memory with ECC enabled

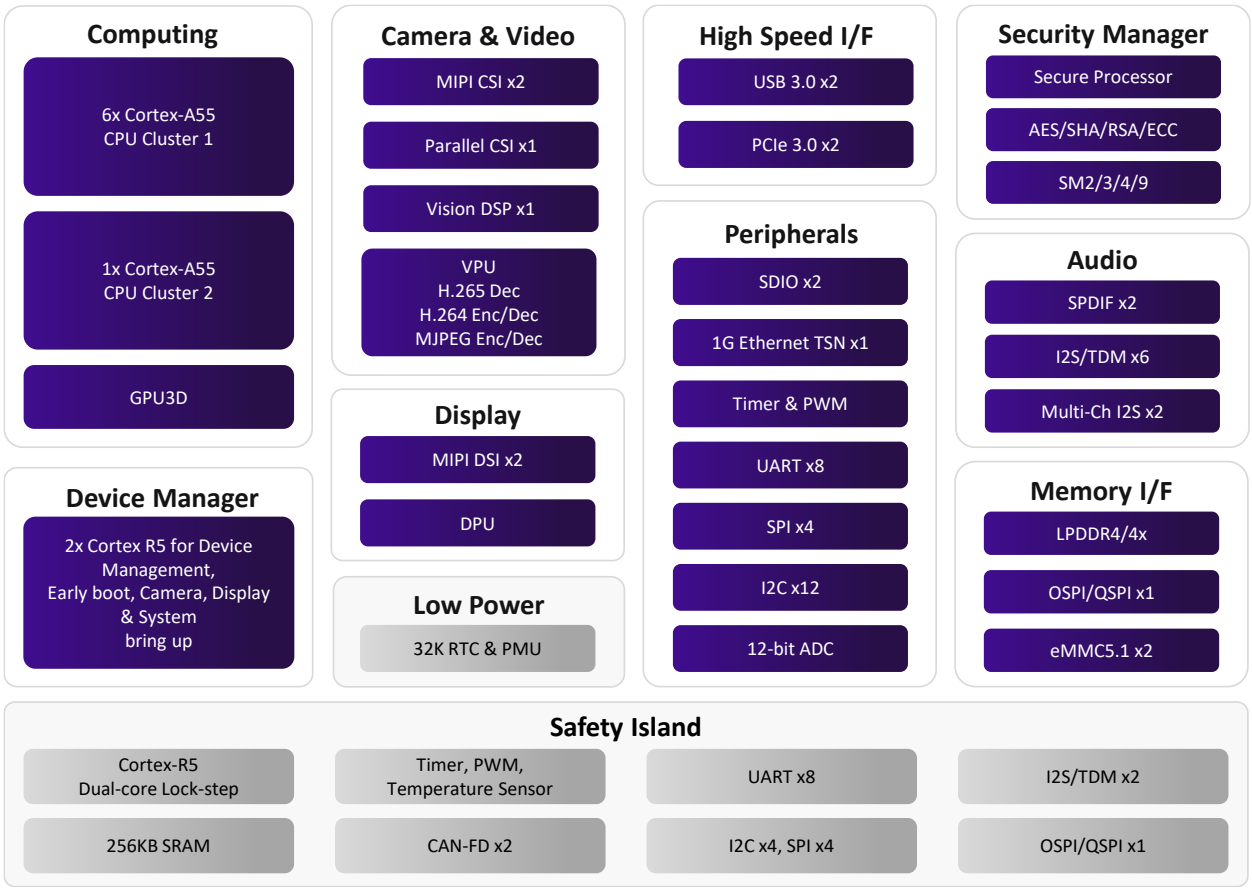
Peripherals

- 2x CAN-FD
- 4x SPI
- 8x UART
- 4x I2C
- GPIO
- PWM
- Temperature Sensor
- Watchdog
- Timer

Low Power RTC and System Control Domain

- 32KHz Oscillator
- Real-Time Clock
- System Power and Reset Control
- 2048-bit Secure Storage Register

Block Diagram



AX110 Block Diagram

Ordering Information

The following table provides detailed specifications for the AX110 Processor.

Part Number	Features	Package	Temperature	Notes
P112A21	6x A55 2.0GHz, 1x A55 1.4GHz, 3x R5, 2x GPU, VPU, PCIe	21x21 FCBGA	-40 ~ 125°C T_j	AEC-Q100 Grade 2 (-40 ~ 105°C) HBM ESD Level 2 CDM ESD Level C1